FSCM0765R

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Low startup current (max 40uA)
- Low power consumption under 1 W at 240VAC & 0.4W load
- Precise Fixed Operating Frequency (66kHz)
- Frequency Modulation for low EMI
- Pulse by Pulse Current Limiting (Adjustable)
- Over Voltage Protection (OVP)
- Over Load Protection (OLP)
- Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under Voltage Lock Out (UVLO) with hysteresis
- Built-in Soft Start (15ms)

Application

- SMPS for VCR, SVR, STB, DVD & DVCD
- Adaptor
- SMPS for LCD Monitor

Description

The FSCM0765R is an integrated Pulse Width Modulator (PWM) and Sense FET specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high voltage power switching regulator which combine an avalanche rugged Sense FET with a current mode PWM control block. The PWM controller includes integrated fixed frequency oscillator, under voltage lockout, leading edge blanking (LEB), optimized gate driver, internal soft start, temperature compensated precise current sources for a loop compensation and self protection circuitry. Compared with discrete MOSFET and PWM controller solution, it can reduce total cost, component count, size and weight simultaneously increasing efficiency, productivity, and system reliability. This device is a basic platform well suited for cost effective designs of flyback converters.

Table 1. Maximum Output Power

OUTPUT POWER TABLE				
PRODUCT	230VAC ±15%(3)		85-265VAC	
	Adapter(1)	Open Frame(2)	Adapter(1)	Open Frame(2)
FSCM0565RD	50W	65W	40W	50W
FSCM0765RD	65W	70W	50W	60W
FSCM0565RC	70W	85W	60W	70W
FSCM0765RC	85W	95W	70W	85W

Notes:

1. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.
2. Maximum practical continuous power in an open frame design at 50°C ambient.
3. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

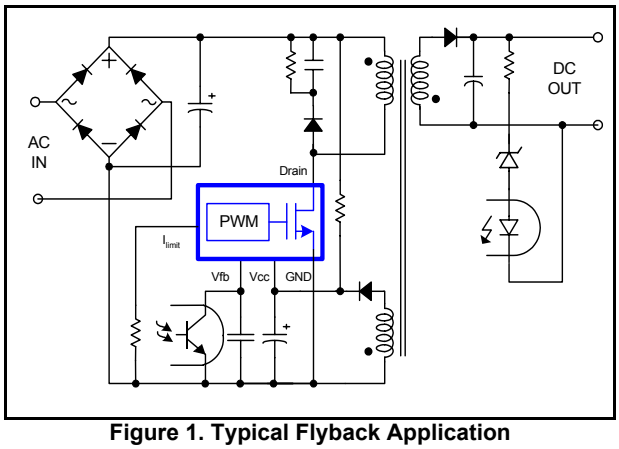


Figure 1. Typical Flyback Application

Internal Block Diagram

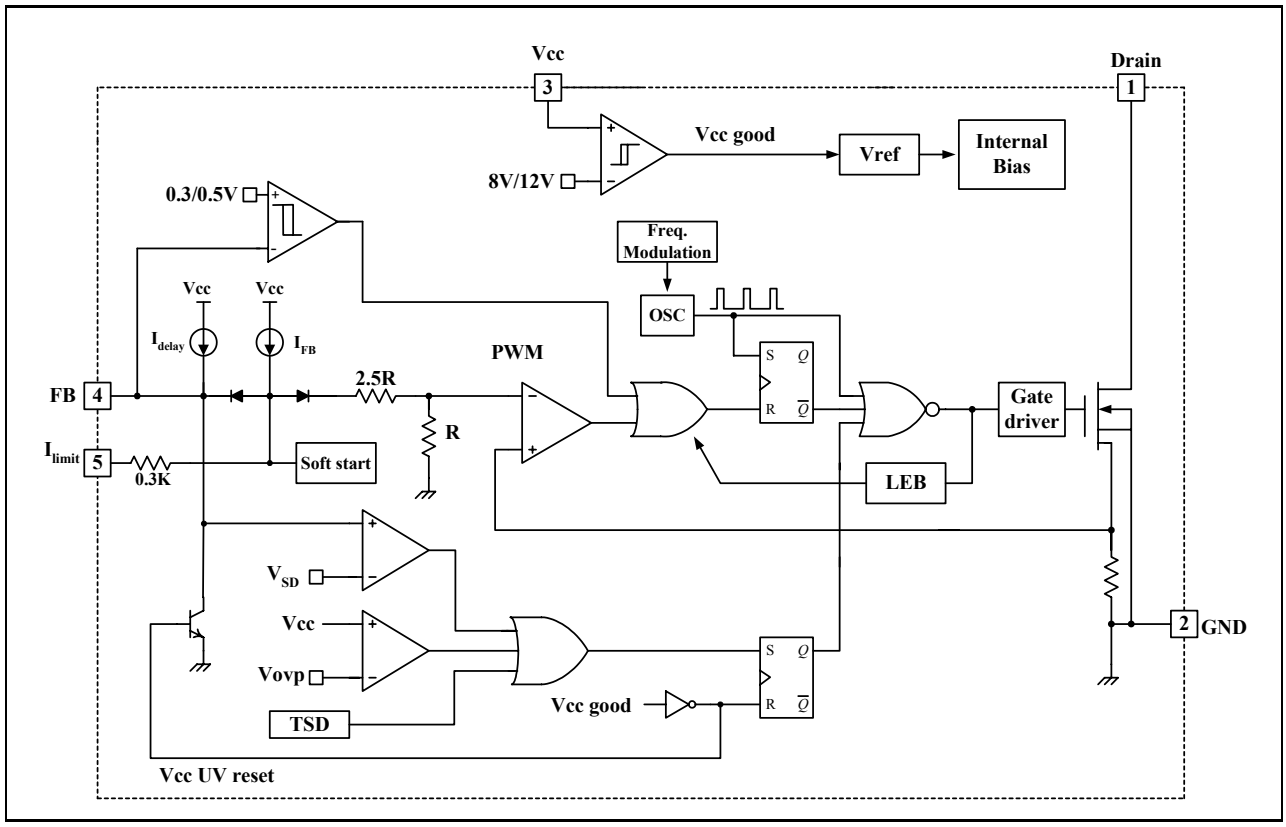


Figure 2. Functional Block Diagram of FSCM0765R

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	Drain	This pin is the high voltage power SenseFET drain. It is designed to drive the transformer directly.
2	GND	This pin is the control ground and the SenseFET source.
3	Vcc	This pin is the positive supply voltage input. Initially, During start up, the power is supplied through the startup resistor from DC link. When Vcc reaches 12V, the power is supplied from auxiliary transformer winding.
4	Feedback (FB)	This pin is internally connected to the inverting input of the PWM comparator. The collector of an optocoupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6.0V, the over load protection is activated resulting in shutdown of the FPS.
5	I_limit	This pin is for the pulse by pulse current limit level programming. By using a resistor to GND on this pin, the current limit level can be changed. If this pin is left floating, the typical current limit will be 3.0A.

Pin Configuration

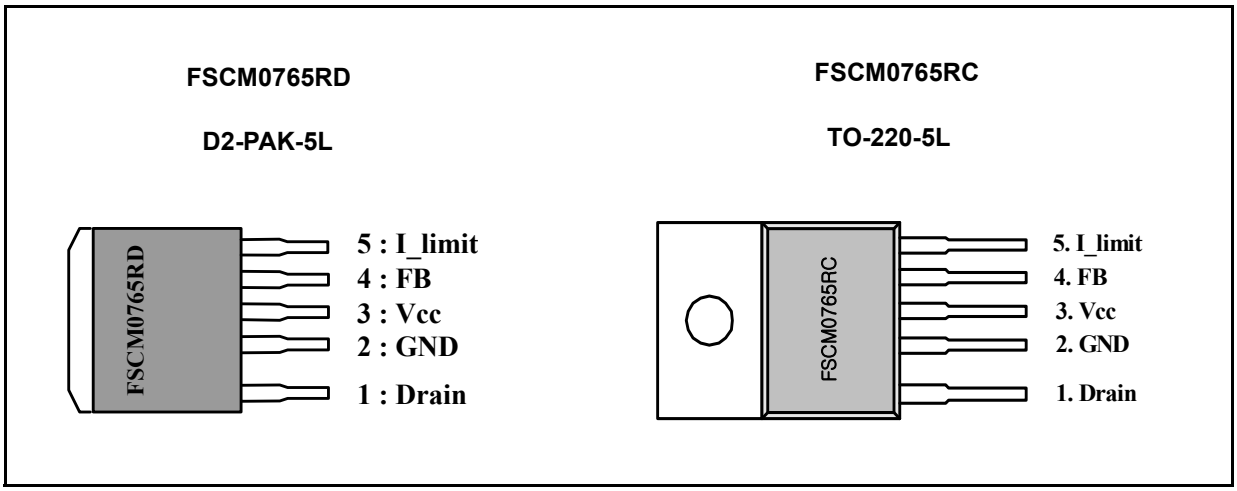


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source (GND) Voltage (1)	V_{DSS}	650	V
Drain-Gate Voltage (R_{GS}=1MΩ)	V_{DGR}	650	V
Gate-Source (GND) Voltage	V_{GS}	±30	V
Drain Current Pulsed (2)	I_{DM}	28	A_{DC}
Single Pulsed Avalanch Energy (3)	E_{AS}	570	mJ
Avalanch Current (4)	I_{AS}	17	A
Continuous Drain Current (TO-220)			
@ Tc = 25°C	I_D	7	A_{DC}
@ T_C=100°C	I_D	4.5	A_{DC}
Continuous Drain Current (D2-PAK)			
@ Tc = 25°C	I_D	4	A_{DC}
@ T_C=100°C	I_D	2.6	A_{DC}
Supply Voltage	V_{CC}	20	V
Analog Input Voltage Range	V_{FB}	-0.3 to V_{CC}	V
Total Power Dissipation (D2-PAK)	P_D	83	W
	Derating	0.664	W/°C
Total Power Dissipation (TO-220)	P_D	145	W
	Derating	1.163	W/°C
Operating Junction Temperature	T_J	Internally limited	°C
Operating Ambient Temperature	T_A	-25 to +85	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
ESD Capability, HBM Model (All pins excepts for Vstr and Vfb)	-	2.0 (Vcc-Vfb=1.0kV)	kV
ESD Capability, Machine Model (All pins excepts for Vstr and Vfb)	-	300 (Vcc-Vfb=100V)	V

Notes:

1. T_j = 25°C to 150°C
2. Repetitive rating: Pulse width limited by maximum junction temperature
3. L = 30mH, V_{DD} = 50V, R_G = 25Ω, starting T_j = 25°C
4. L = 13uH, starting T_j = 25°C

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET SECTION						
Drain source breakdown voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	650	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} = Max, Rating V_{GS} = 0V	-	-	500	μA
Static drain source on resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 2.3A	-	1.4	1.6	Ω
Output capacitance	C_{OSS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz	-	100	-	pF
Turn on delay time	$T_{D(ON)}$	V_{DD}= 325V, I_D= 5A (MOSFET switching time is essentially independent of operating temperature)	-	25	-	ns
Rise time	T_R		-	60	-	
Turn off delay time	$T_{D(OFF)}$		-	115	-	
Fall time	T_F		-	65	-	
CONTROL SECTION						
Initial frequency	F_{OSC}	V_{CC}=14V, V_{FB}=5V	60	66	72	kHz
Modulated frequency range	ΔF_{mod}	-	-	±3	-	kHz
Frequency modulation cycle	T_{mod}	-	-	4	-	ms
Voltage stability	F_{STABLE}	10V≤V_{CC}≤17V	0	1	3	%
Temperature stability	ΔF_{OSC}	−25°C≤Ta≤+85°C	-	±5	±10	%
Maximum duty cycle	D_{MAX}	-	75	80	85	%
Minimum duty cycle	D_{MIN}	-	-	-	0	%
Start threshold voltage	V_{START}	V_{FB}=GND	11	12	13	V
Stop threshold voltage	V_{STOP}	V_{FB}=GND	7	8	9	V
Feedback source current	I_{FB}	V_{FB}=GND	0.7	0.9	1.1	mA
Soft-start time	T_{SS}	-	10	15	20	ms
Leading Edge Blanking time	T_{LEB}	-	-	300	-	ns
BURST MODE SECTION						
Burst Mode Voltages	V_{BH}	Vcc=14V	0.4	0.5	0.6	V
	V_{BL}	Vcc=14V	0.24	0.3	0.36	V

PROTECTION SECTION						
Peak current limit	I_{LIM}	V_{CC}=14V, V_{FB}=5V	2.64	3	3.36	A
Over voltage protection	V_{OVP}	-	18	19	20	V
Thermal shutdown temperature	T_{SD}		130	145	160	°C
Shutdown delay current	I_{DELAY}	V_{FB}=4V	3.5	5.3	7	μA
Shutdown feedback voltage	V_{SD}	V_{FB}≥5.5V	5.5	6	6.5	V
TOTAL DEVICE SECTION						
Startup current	I_{start}		-	20	40	μA
Operating supply current	$I_{OP(MIN)}$	V_{CC}=10V, V_{FB}=0V	-	2.5	5	mA
	$I_{OP(MAX)}$	V_{CC}=20V, V_{FB}=0V				

Notes:

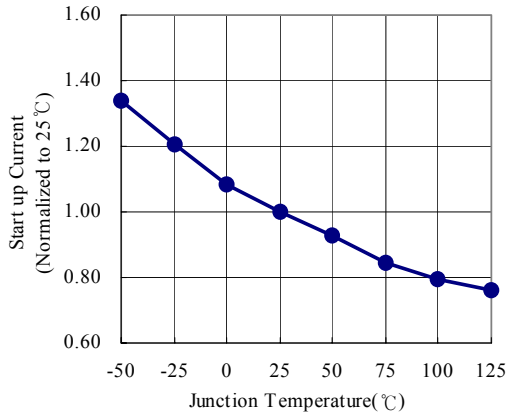
1. Pulse test : Pulse width ≤ 300μS, duty ≤ 2%
2. These parameters, although guaranteed at the design, are not tested in mass production.
3. These parameters, although guaranteed, are tested in EDS (wafer test) process.
4. These parameters indicate the inductor current.
5. This parameter is the current flowing into the control IC.

Comparison Between FSDM07652R and FSCM0765R

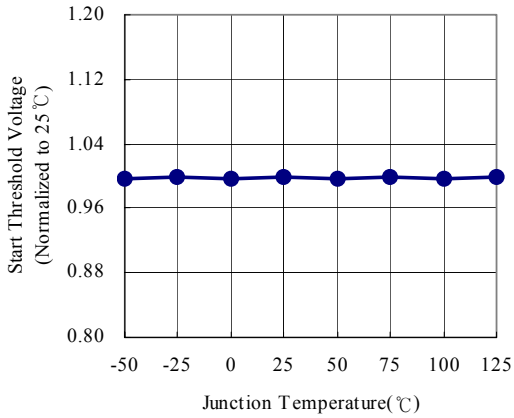
Function	FSDM07652R	FSCM0765R
Frequency modulation	N.A.	Available • Modulated frequency range (DF_{mod}) = ±3kHz • Frequency modulation cycle (T_{mod}) = 4ms
Pulse-by-pulse current limit	• Internally fixed (2.5A)	• Programmable using external resistor (3.0A max)
Internal Startup Circuit	• Available	• N.A. (Requires startup resistor) • Startup current : 40uA (max)

Typical Performance Characteristics

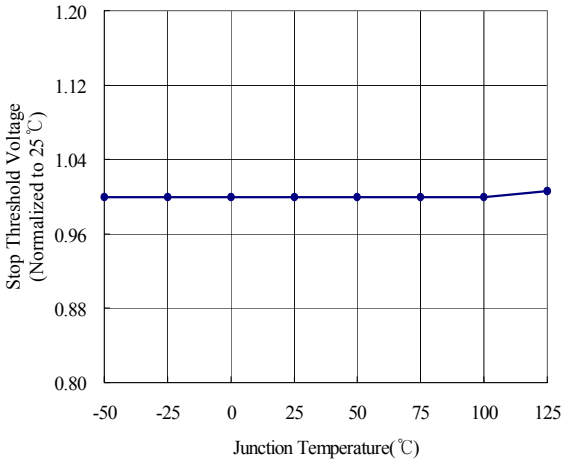
(These Characteristic Graphs are Normalized at Ta= 25°C)



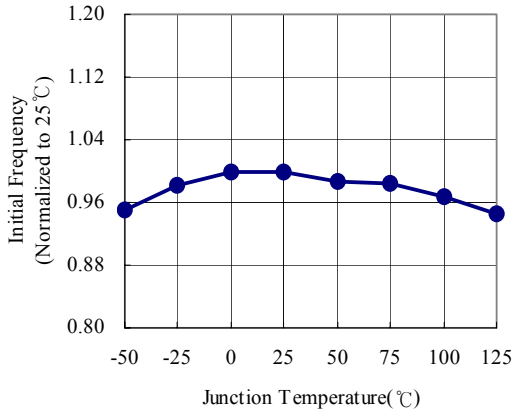
Startup Current vs. Temp



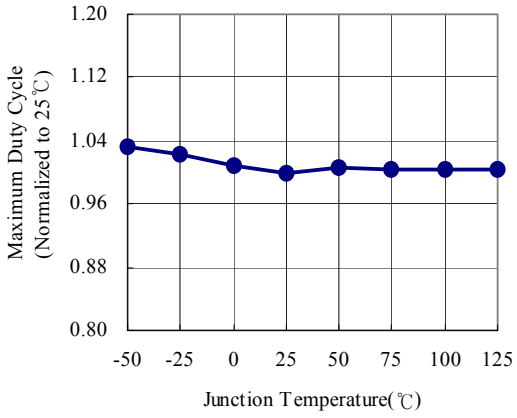
Start Threshold Voltage vs. Temp



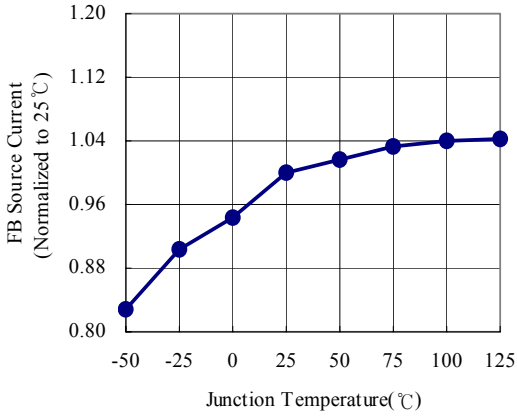
Stop Threshold Voltage vs. Temp



Initial Freqency vs. Temp



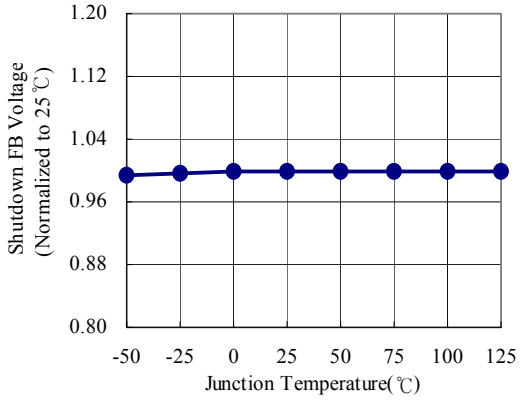
Maximum Duty Cycle vs. Temp



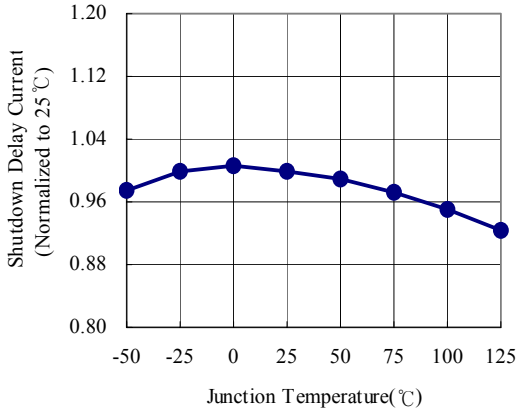
Feedback Source Current vs. Temp

Typical Performance Characteristics (Continued)

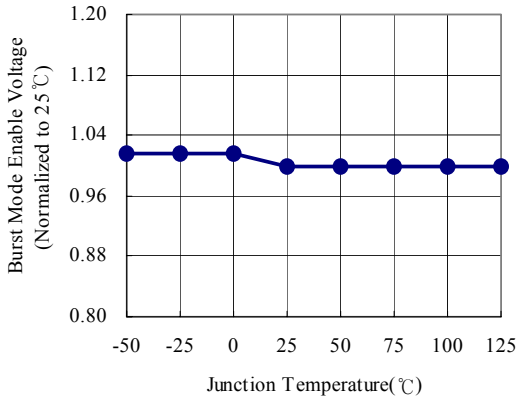
(These Characteristic Graphs are Normalized at Ta= 25°C)



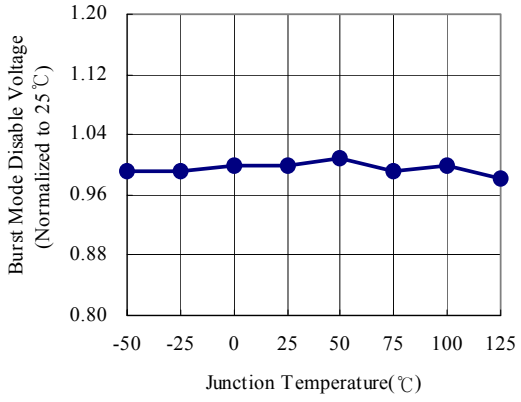
ShutDown Feedback Voltage vs. Temp



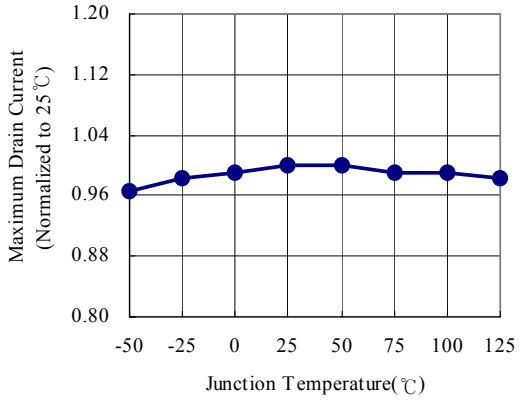
ShutDown Delay Current vs. Temp



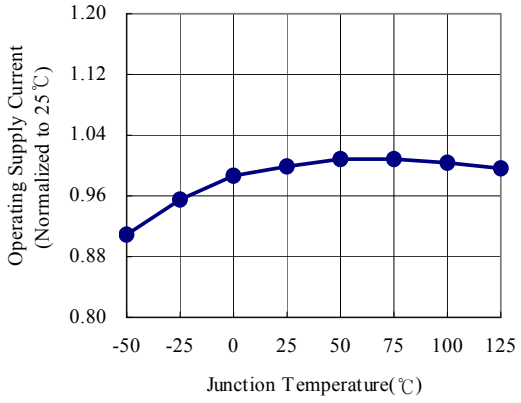
Bust Mode Enable Volage vs. Temp



Burst Mode Disable Voltage vs. Temp



Mavimum Drain Current vs. Temp



Operating Supply Current vs. Temp

Functional Description

1. **Startup** : Figure 4 shows the typical startup circuit and transformer auxiliary winding for FSCM0765R application. Before FSCM0765R begins switching, FSCM0765R consumes only startup current (typically 25uA) and the current supplied from the DC link supply ccurrent consumed by FPS (Icc) and charges the external capacitor (C_a) that is connected to the Vcc pin. When Vcc reaches start voltage of 12V (V_{START}), FSCM0765R begins switching, and the current consumed by FSCM0765R increases to 3mA. Then, FSCM0765R continues its normal switching operation and the power required for this device is supplied from the transformer auxiliary winding, unless Vcc drops below the stop voltage of 8V (V_{STOP}). To guarantee the stable operation of the control IC, Vcc has under voltage lockout (UVLO) with 4V hysteresis. Figure 5 shows the relation between the current consumed by FPS (Icc) and the supply voltage (Vcc).

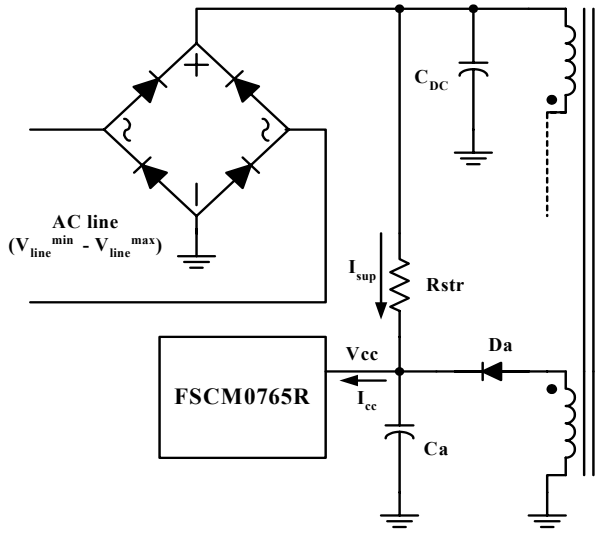


Figure 4. Startup circuit

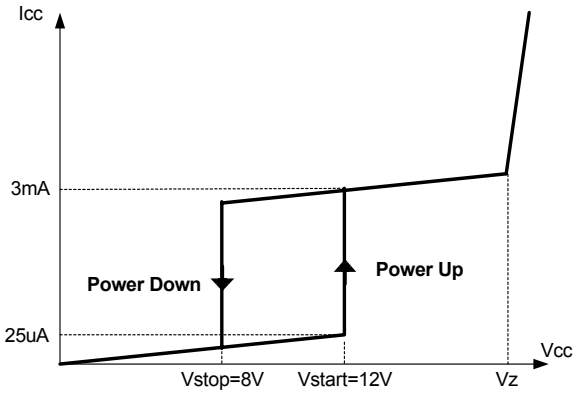


Figure 5. Relation between operating supply current and Vcc voltage

The minimum current supplied through the startup resistor is given by

$$I_{sup}^{min} = (\sqrt{2} \cdot V_{line}^{min} - V_{start}) \cdot \frac{1}{R_{str}}$$

where V_{line}^{min} is the minimum input voltage, V_{start} is the start voltage (12V) and R_{str} is the startup resistor. The startup resistor should be chosen so that I_{sup}^{min} is larger than the maximum startup current (40uA). If not, Vcc can not be charged to the start voltage and FPS will fail to start up.

2. Feedback Control : FSCM0765R employs current mode control, as shown in Figure 6. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the KA431 exceeds the internal reference voltage of 2.5V, the H11A817A LED current increases, thus pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-pulse current limit: Because current mode control is employed, the peak current through the Sense FET is determined by the inverting input of PWM comparator (Vfb*) as shown in Figure 6. When the current through the opto transistor is zero and the current limit pin (#5) is left floating, the feedback current source (I_{FB}) of 0.9mA flows only through the internal resistor (R+2.5R=2.8k). In this case, the cathode voltage of diode D2 and the peak drain current have maximum values of 2.5V and 3A, respectively. The pulse-by-pulse current limit can be adjusted using a resistor to GND on current limit pin (#5). The current limit level using an external resistor (R_{LIM}) is given by

$$I_{LIM} = \frac{R_{LIM} \cdot 3A}{2.8k\Omega + R_{LIM}}$$

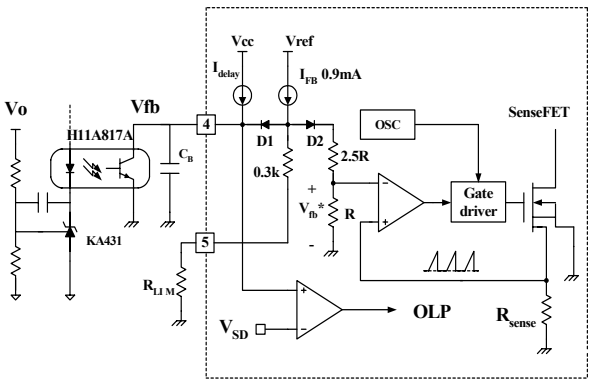


Figure 6. Pulse width modulation (PWM) circuit

2.2 Leading edge blanking (LEB) : At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the Rsense resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSCM0765R employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (T_{LEB}) after the Sense FET is turned on.

3. Protection Circuit : The FSCM0765R has several self protective functions such as over load protection (OLP), over voltage protection (OVP) and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without increasing cost. Once the fault condition occurs, switching is terminated and the Sense FET remains off. This causes Vcc to fall. When Vcc reaches the UVLO stop voltage of 8V, the current consumed by FSCM0765R reduces to the startup current (typically 25uA) and the current supplied from the DC link charges the external capacitor (C_a) that is connected to the Vcc pin. When Vcc reaches the start voltage of 12V, FSCM0765R resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated (see Figure 7).

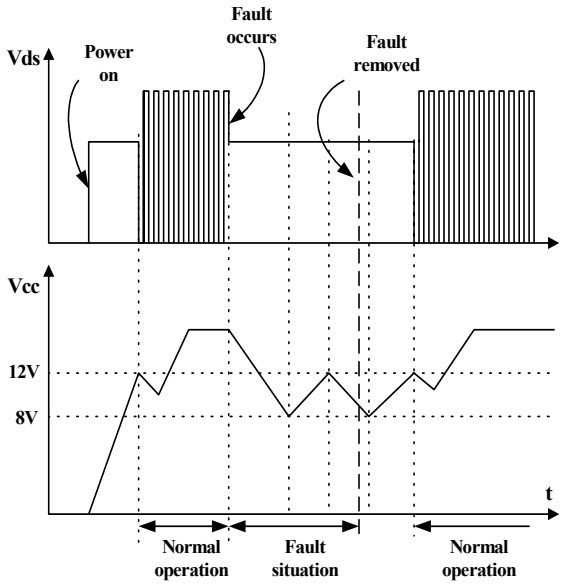


Figure 7. Auto restart operation

3.1 Over Load Protection (OLP) : Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated in order to protect the SMPS. However, even when the SMPS is in the normal operation, the over load protection circuit can be activated during the load transition. In order to avoid this undesired operation, the over load protection circuit is designed to be activated after a specified time to determine whether it is a transient situation or an overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the Sense FET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (Vfb). If Vfb exceeds 2.5V, D1 is blocked and the 5.3uA current source (I_{delay}) starts to charge C_B slowly up to Vcc. In this condition, Vfb continues increasing until it reaches 6V, when the switching operation is terminated as shown in Figure 8. The delay time for shutdown is the time required to charge C_B from 2.5V to 6.0V with 5.3uA (I_{delay}). In general, a 10 ~ 50 ms delay time is typical for most applications.

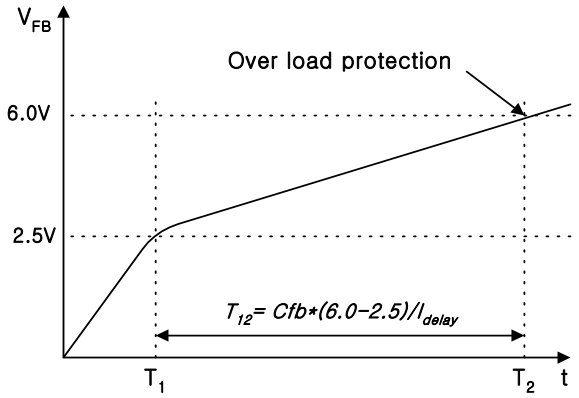


Figure 8. Over load protection

3.2 Over voltage Protection (OVP) : If the secondary side feedback circuit were to malfunction or a solder defect caused an open in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FSCM0765R uses Vcc instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, an OVP circuit is activated resulting in the termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be designed to be below 19V.

3.3 Thermal Shutdown (TSD) : The Sense FET and the control IC are built in one package. This makes it easy for the control IC to detect the heat generation from the Sense FET. When the temperature exceeds approximately 145°C, the thermal protection is triggered resulting in shutdown of FPS.

4. Frequency Modulation : EMI reduction can be accomplished by modulating the switching frequency of a switched power supply. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the band width measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 9, the frequency changes from 63KHz to 69KHz in 4ms.

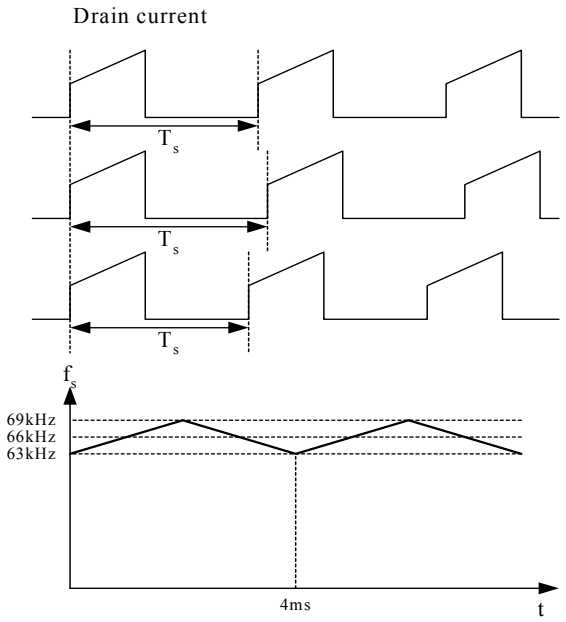


Figure 9. Frequency Modulation

5. Soft Start : The FSCM0765R has an internal soft start circuit that increases PWM comparator inverting input voltage together with the Sense FET current slowly after it starts up. The typical soft start time is 15msec, The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, rectifier diodes and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode during startup.

6. Burst operation : In order to minimize power dissipation in standby mode, the FSCM0765R enters into burst mode operation at light load condition. As the load decreases, the feedback voltage decreases. As shown in Figure 10, the device automatically enters into burst mode when the feedback voltage drops below V_{BL} (300mV). At this point switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BH} (500mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in standby mode.

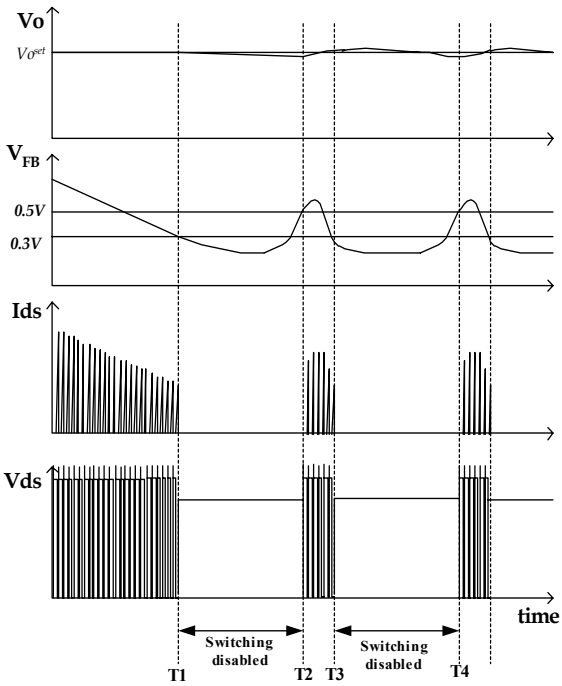


Figure 10. Waveforms of burst operation

Typical application circuit

Application	Output power	Input voltage	Output voltage (Max current)
LCD Monitor	40W	Universal input (85-265Vac)	5V (2.0A) 12V (2.5A)

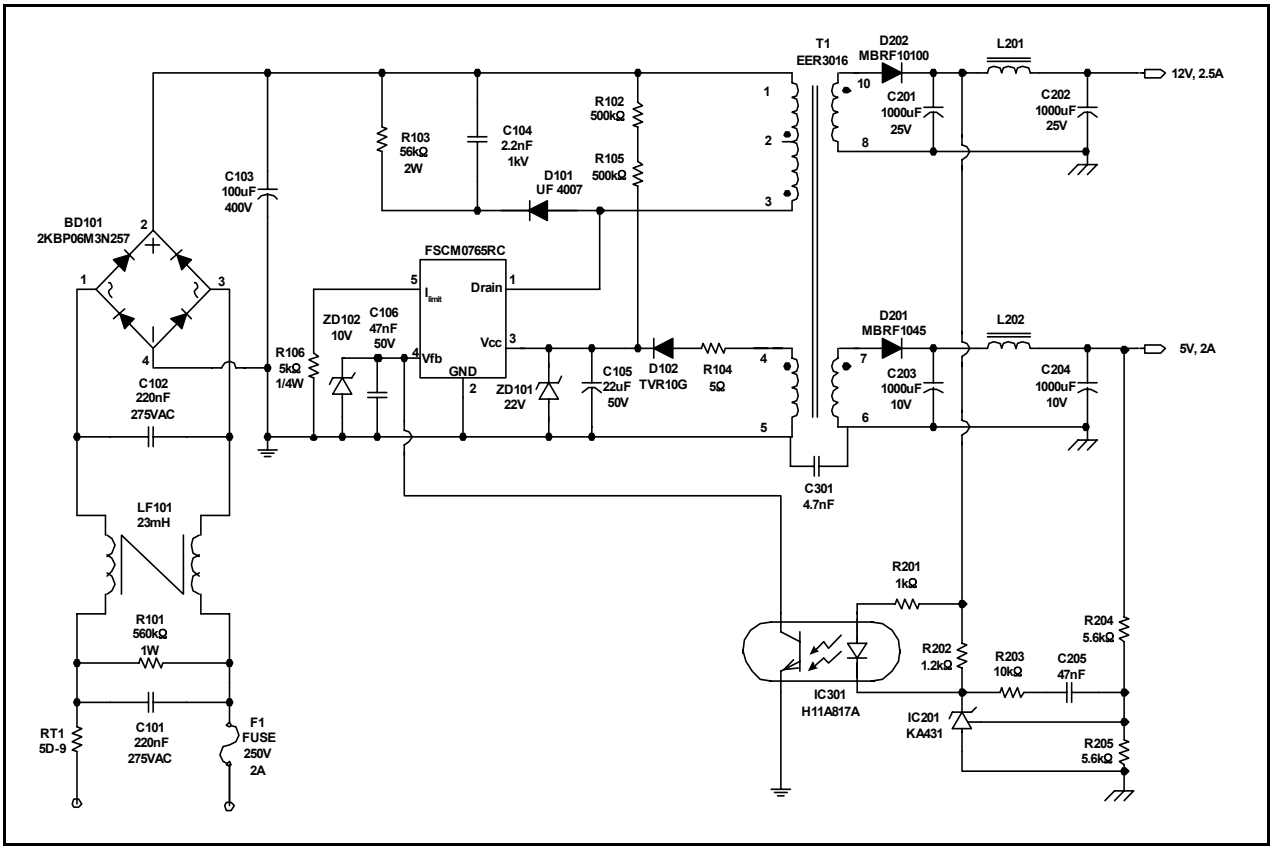
Features

- High efficiency (>81% at 85Vac input)
- Low standby mode power consumption (<1W at 240Vac input and 0.4W load)
- Low component count
- Enhanced system reliability through various protection functions
- Low EMI through frequency modulation
- Internal soft-start (15ms)

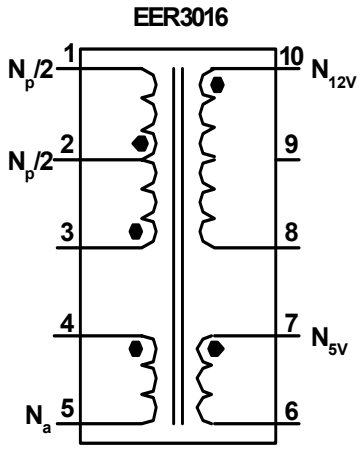
Key Design Notes

- The delay time for over load protection is designed to be about 50ms with C106 of 47nF. If a faster triggering of OLP is required, C106 can be reduced to 22nF.
- Using a resistor R106 on the current limit pin (#5), the pule-by-pulse current limit level is reduced to about 2A.
- Zener diode ZD102 is used for a safety test such as UL. When the drain pin and feedback pin are shorted, the zener diode fails and remains short, which causes the fuse (F1) blown and prevents explosion of the opto-coupler (IC301). This zener diode also increases the immunity against line surge.

1. Schematic



2. Transformer Schematic Diagram



3.Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
Na	4 → 5	$0.2^{\phi} \times 1$	8	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	2 → 1	$0.4^{\phi} \times 1$	18	Solenoid Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N_{12V}	10 → 8	$0.3^{\phi} \times 3$	7	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
N5V	7 → 6	$0.3^{\phi} \times 3$	3	Center Winding
Insulation: Polyester Tape t = 0.050mm, 2Layers				
Np/2	3 → 2	$0.4^{\phi} \times 1$	18	Solenoid Winding
Outer Insulation: Polyester Tape t = 0.050mm, 2Layers				

4.Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	520uH ± 10%	100kHz, 1V
Leakage Inductance	1 - 3	10uH Max	2^{nd} all short

5. Core & Bobbin

Core : EER 3016
Bobbin : EER3016
Ae(mm2) : 96

6.Demo Circuit Part List

Part	Value	Note	Part	Value	Note
Fuse			C301	4.7nF	Polyester Film Cap.
F101	2A/250V				
NTC			**Inductor**		
RT101	5D-9		L201	5uH	Wire 1.2mm
Resistor			L202	5uH	Wire 1.2mm
R101	560K	1W			
R102	500K	1/4W			
R103	56K	2W			
R104	5	1/4W	**Diode**		
R105	500K	1/4W	D101	UF4007	
R106	5K	1/4W	D102	TVR10G	
R201	1K	1/4W	D201	MBRF1045	
R202	10K	1/4W	D202	MBRF10100	
R203	1.2K	1/4W	ZD101	22V Zener diode	
R204	5.6K	1/4W	ZD102	10V Zener diode	
R205	5.6K	1/4W	**Bridge Diode**		
			BD101	2KBP06M 3N257	Bridge Diode
Capacitor					
C101	220nF/275VAC	Box Capacitor	**Line Filter**		
C102	220nF/275VAC	Box Capacitor	LF101	23mH	Wire 0.4mm
C103	100uF/400V	Electrolytic Capacitor	**IC**		
C104	10nF/1kV	Ceramic Capacitor	IC101	FSCM0765RC	FPS^{TM}(7A,650V)
C105	22uF/50V	Electrolytic Capacitor	IC201	KA431(TL431)	Voltage reference
C106	47nF/50V	Ceramic Capacitor	IC301	H11A817A	Opto-coupler
C201	1000uF/25V	Electrolytic Capacitor			
C202	1000uF/25V	Electrolytic Capacitor			
C203	1000uF/10V	Electrolytic Capacitor			
C204	1000uF/10V	Electrolytic Capacitor			
C205	47nF/50V	Ceramic Capacitor			

7. Layout

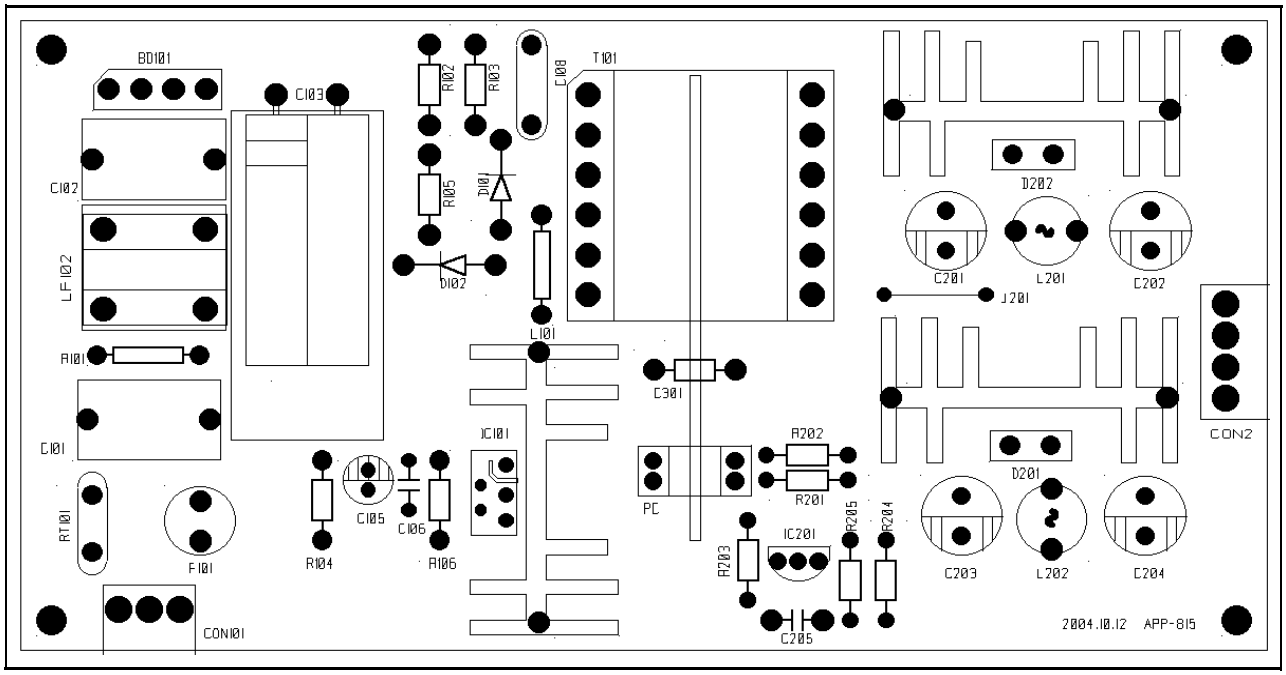


Figure 11. Layout Considerations for FSCM0765RC

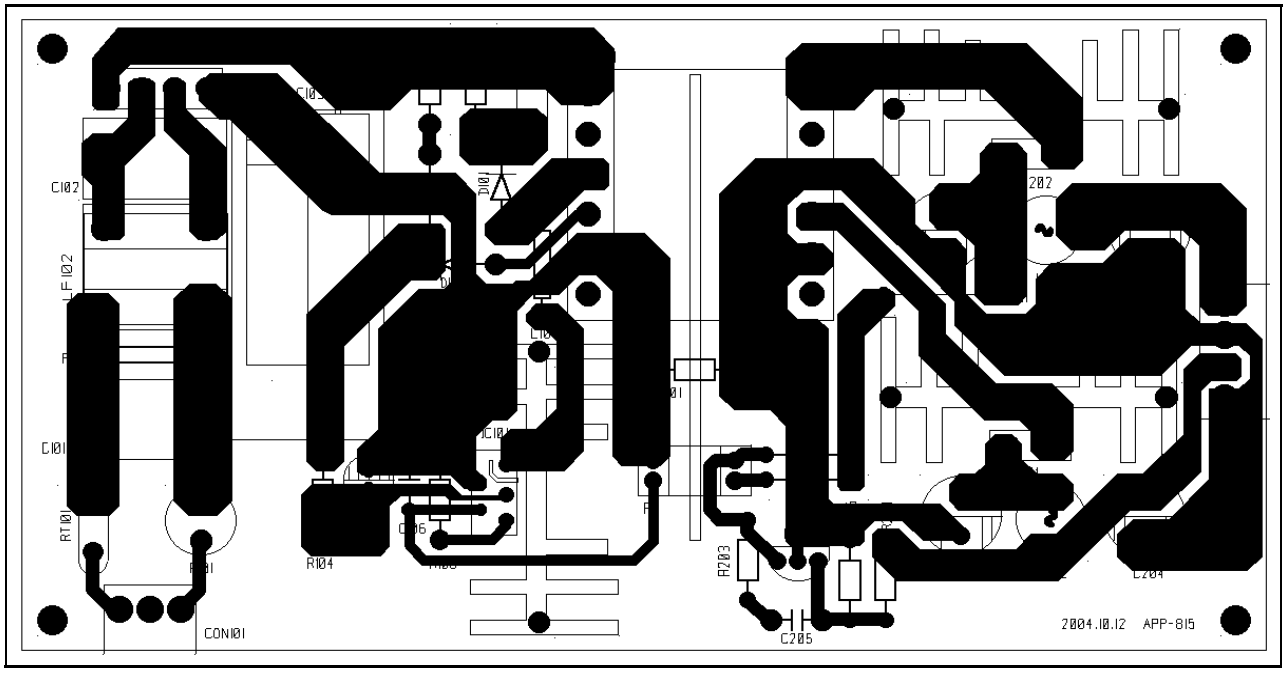
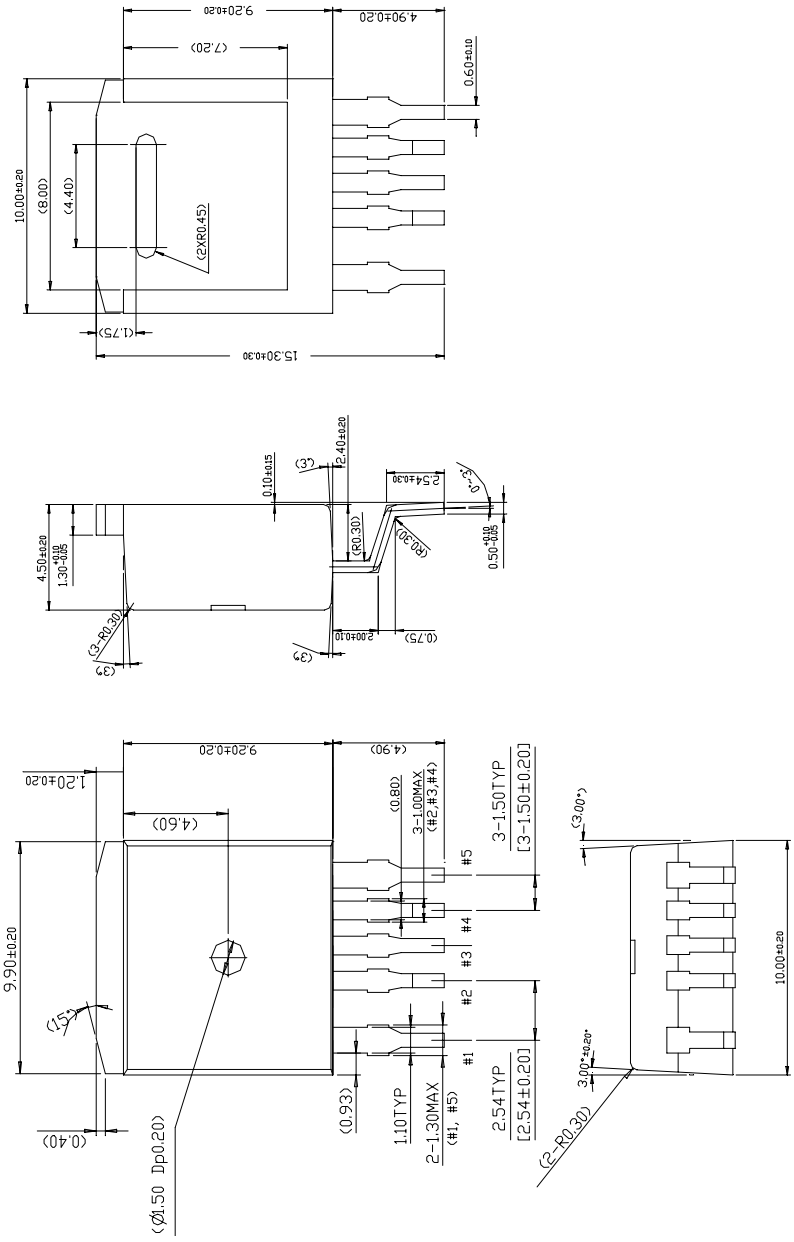


Figure 12. Layout Considerations for FSCM0765RC

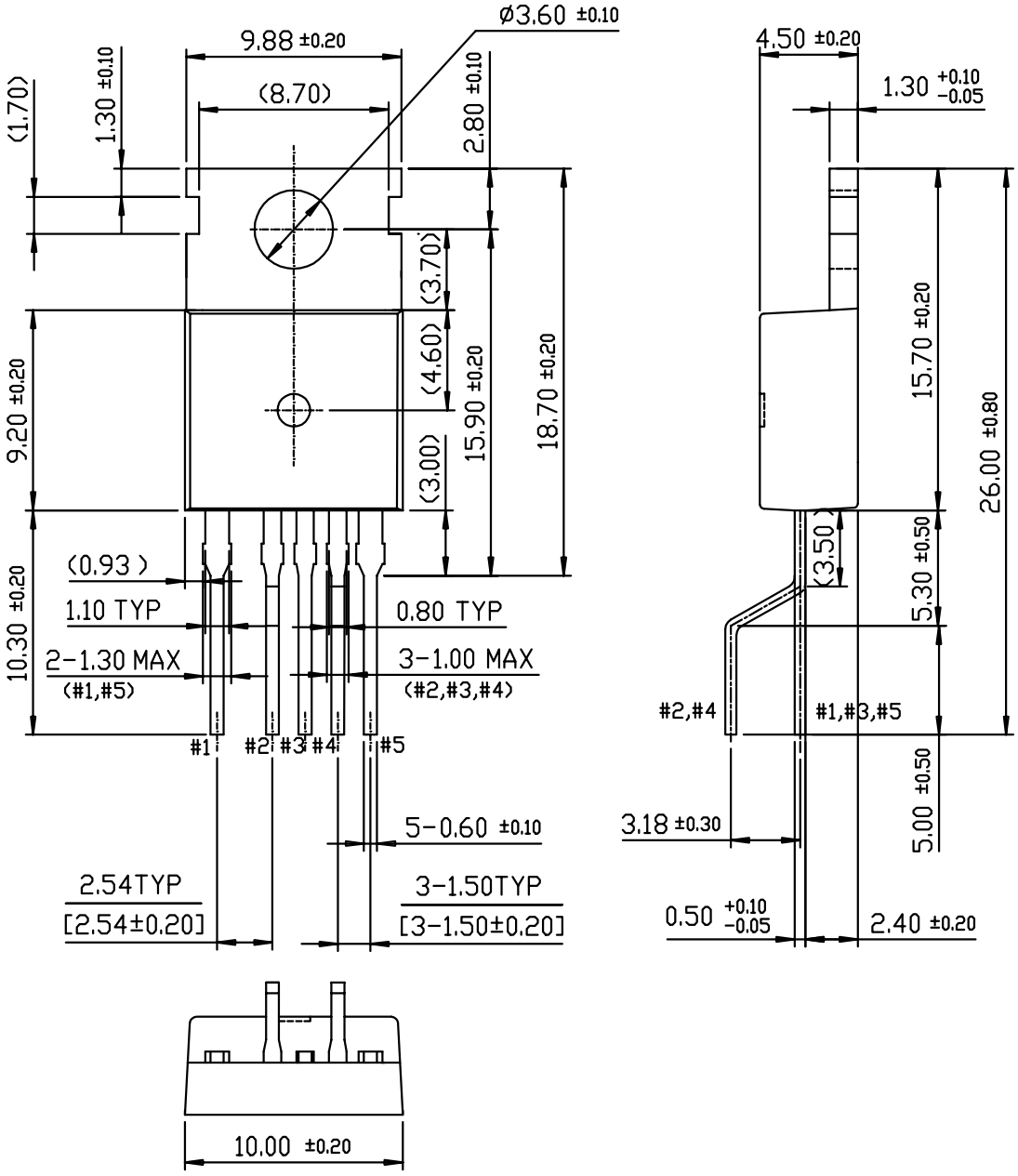
Package Dimensions

D2-PAK-5L



Package Dimensions (Continued)

TO-220-5L(Forming)



Ordering Information

Product Number	Package	Marking Code	BVdss	Rds(on)Max.
FSCM0765RD	D2-PAK-5L	CM0765RD	650V	1.6 Ω
FSCM0765RCYDTU	TO-220-5L	CM0765RC	650V	1.6 Ω