

75A, 30V, 0.011 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs



These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process. This advanced process technology

achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76132.

Ordering Information

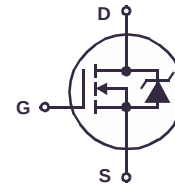
PART NUMBER	PACKAGE	BRAND
HUF76132P3	TO-220AB	76132P
HUF76132S3S	TO-263AB	76132S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF76132S3ST.

Features

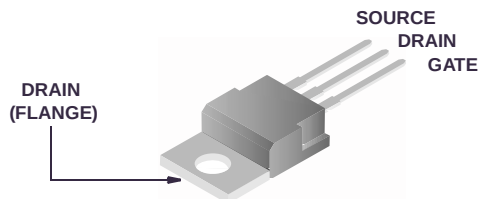
- Logic Level Gate Drive
- 75A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.011\Omega$
- Temperature Compensating PSPICE® Model
- Temperature Compensating SABER® Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

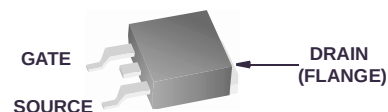


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



HUF76132P3, HUF76132S3S

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30 V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	30 V
Gate to Source Voltage	V_{GS}	± 20 V
Drain Current		
Continuous ($T_C = 25^{\circ}\text{C}$, $V_{GS} = 10\text{V}$) (Figure 2)	I_D	75 A
Continuous ($T_C = 100^{\circ}\text{C}$, $V_{GS} = 5\text{V}$)	I_D	44 A
Continuous ($T_C = 100^{\circ}\text{C}$, $V_{GS} = 4.5\text{V}$) (Figure 2)	I_D	41 A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	E_{AS}	Figures 6, 17, 18
Power Dissipation	P_D	120 W
Derate Above 25°C		0.97 W/ $^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-40 to 150 $^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334.	T_{pkg}	260 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_A = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25V, V _{GS} = 0V	-	-	1	μA
		V _{DS} = 25V, V _{GS} = 0V, T _C = 150 ⁰ C	-	-	250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V
Drain to Source On Resistance	r _{DS(ON)}	I _D = 75A, V _{GS} = 10V (Figure 9, 10)	-	0.0085	0.011	Ω
		I _D = 44A, V _{GS} = 5V (Figure 9)	-	0.013	0.016	Ω
		I _D = 41A, V _{GS} = 4.5V (Figure 9)	-	0.015	0.018	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	-	-	1.03	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-220, TO-262 and TO-263	-	-	62	°C/W
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)						
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≅ 41A, R _L = 0.366Ω, V _{GS} = 4.5V, R _{GS} = 6.2Ω (Figures 15, 21, 22)	-	-	185	ns
Turn-On Delay Time	t _{d(ON)}		-	17	-	ns
Rise Time	t _r		-	105	-	ns
Turn-Off Delay Time	t _{d(OFF)}		-	33	-	ns
Fall Time	t _f		-	42	-	ns
Turn-Off Time	t _{OFF}		-	-	113	ns

HUF76132P3, HUF76132S3S

Electrical Specifications $T_A = 25^{\circ}\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING SPECIFICATIONS (VGS = 10V)							
Turn-On Time	tON	VDD = 15V, ID ≅ 75A, RL = 0.20, VGS = 10V, RGS = 6.8Ω (Figures 16, 21, 22)		-	-	72	ns
Turn-On Delay Time	td(ON)			-	11	-	ns
Rise Time	tr			-	37	-	ns
Turn-Off Delay Time	td(OFF)			-	65	-	ns
Fall Time	tf			-	42	-	ns
Turn-Off Time	tOFF			-	-	160	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Qg(TOT)	VGS = 0V to 10V	VDD = 15V, ID ≅ 44A, RL = 0.341Ω Ig(REF) = 1.0mA (Figures 14, 19, 20)	-	44	52	nC
Gate Charge at 5V	Qg(5)	VGS = 0V to 5V		-	25	30	nC
Threshold Gate Charge	Qg(TH)	VGS = 0V to 1V		-	1.8	2.2	nC
Gate to Source Gate Charge	Qgs			-	4.80	-	nC
Gate to Drain “Miller” Charge	Qgd			-	13.50	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	CISS	VDS = 25V, VGS = 0V, f = 1MHz (Figure 13)		-	1650	-	pF
Output Capacitance	COSS			-	850	-	pF
Reverse Transfer Capacitance	CRSS			-	200	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 44\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 44\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	71	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 44\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	104	nC

Typical Performance Curves Unless Otherwise Specified

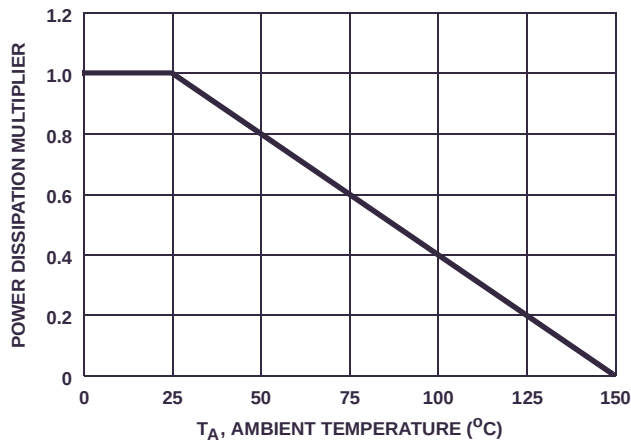


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

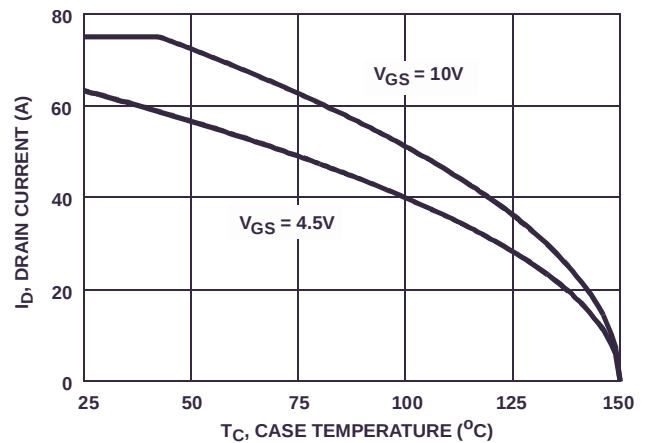


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

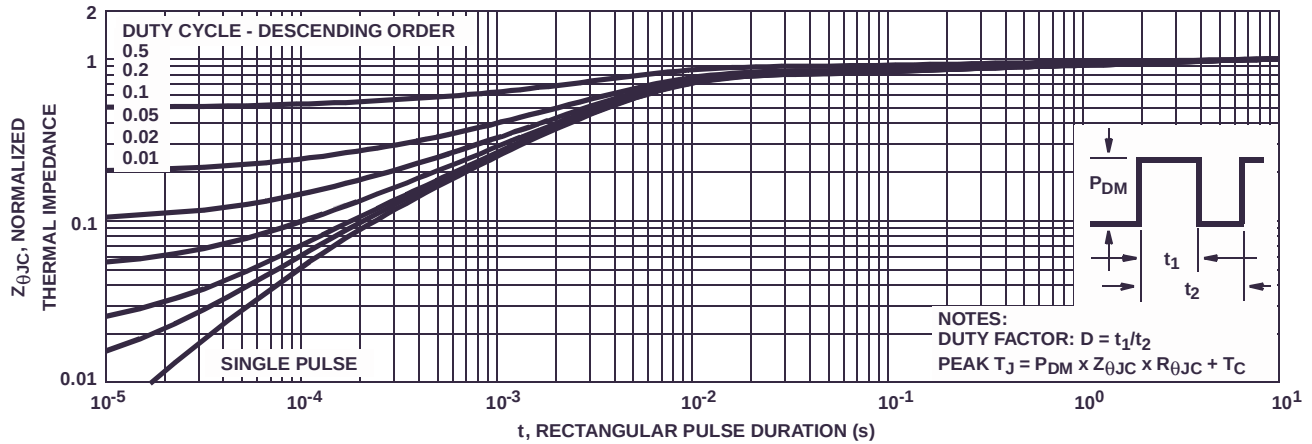


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

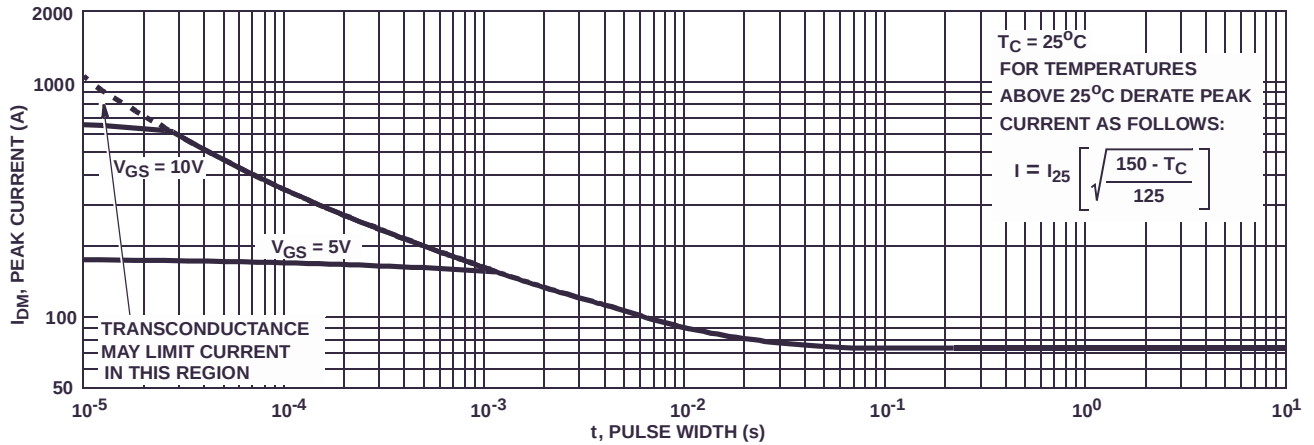


FIGURE 4. PEAK CURRENT CAPABILITY

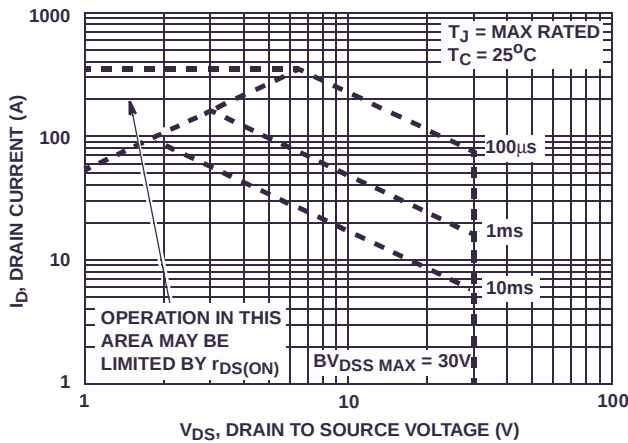
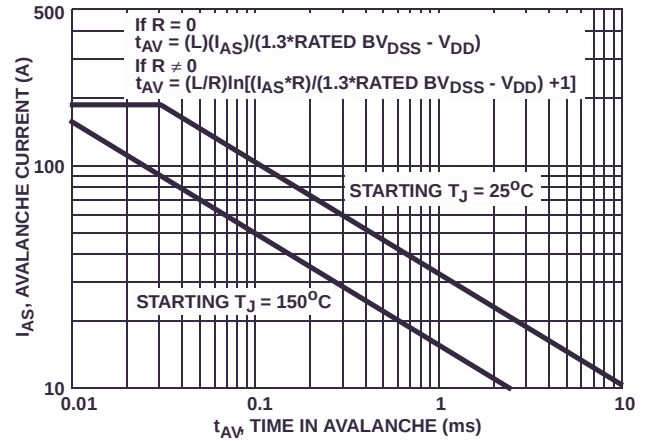


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)

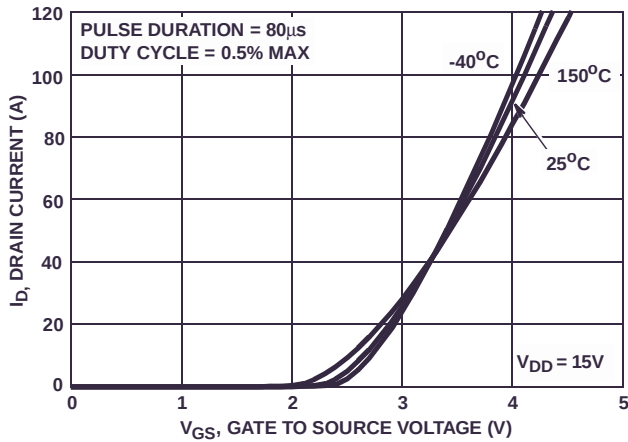


FIGURE 7. TRANSFER CHARACTERISTICS

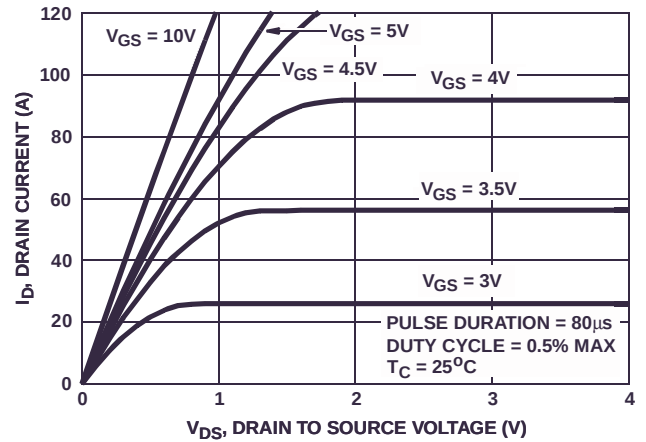


FIGURE 8. SATURATION CHARACTERISTICS

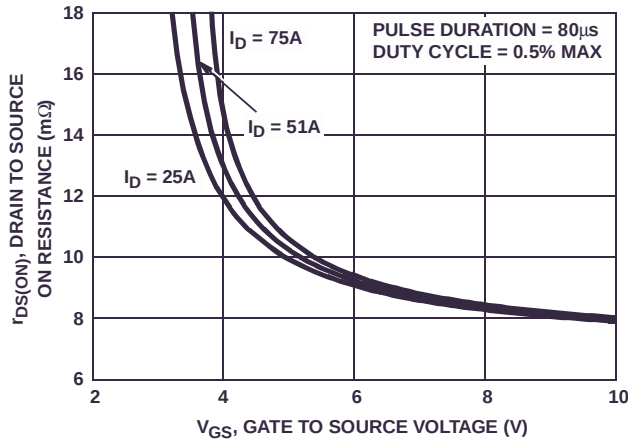


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

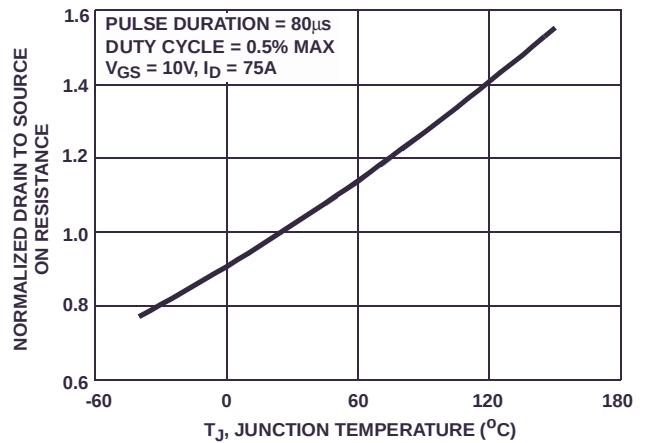


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

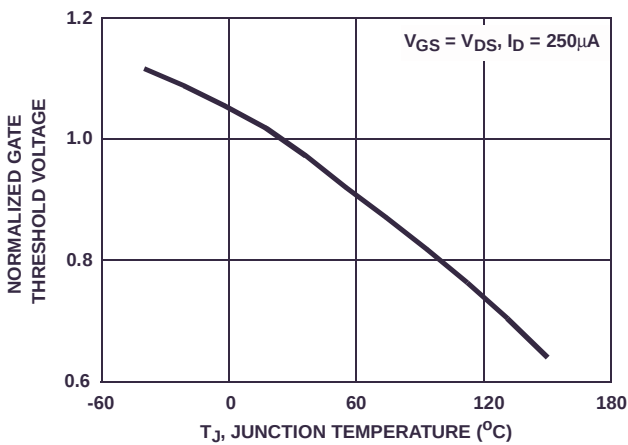


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

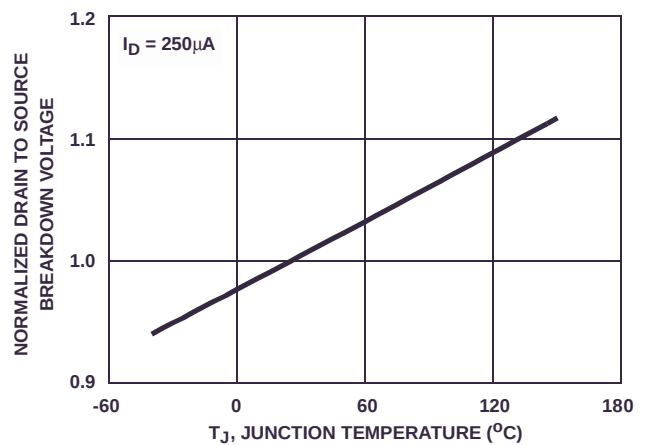


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Test Circuits and Waveforms (Continued)

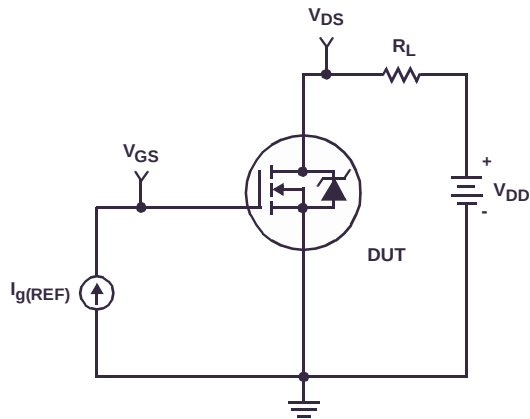


FIGURE 19. GATE CHARGE TEST CIRCUIT

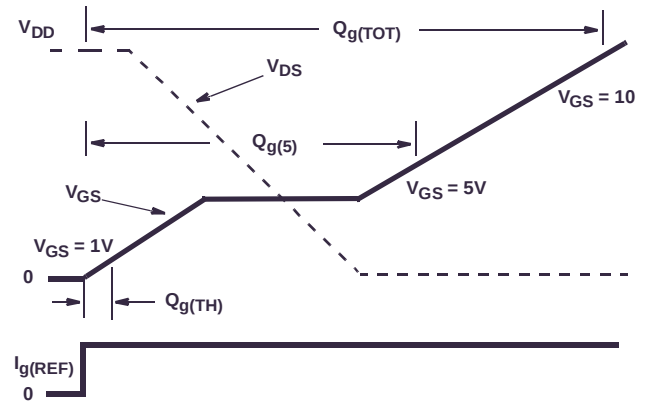


FIGURE 20. GATE CHARGE WAVEFORMS

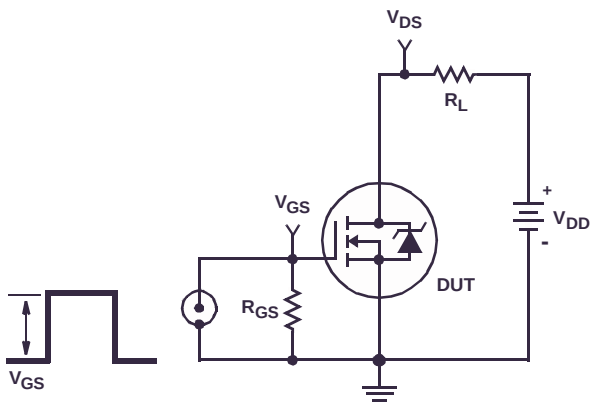


FIGURE 21. SWITCHING TIME TEST CIRCUIT

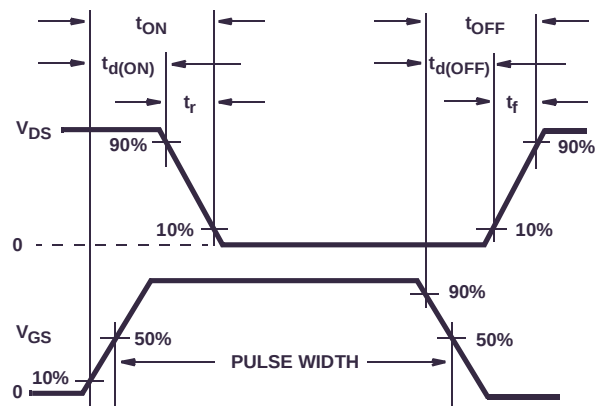


FIGURE 22. SWITCHING TIME WAVEFORM

SPICE Thermal Model

REV May 1998

HUF76132

CTHERM1 th 6 5.00e-3
 CTHERM2 6 5 1.18e-2
 CTHERM3 5 4 15.5e-2
 CTHERM4 4 3 1.85e-2
 CTHERM5 3 2 2.00e-2
 CTHERM6 2 tl 2.5e-2

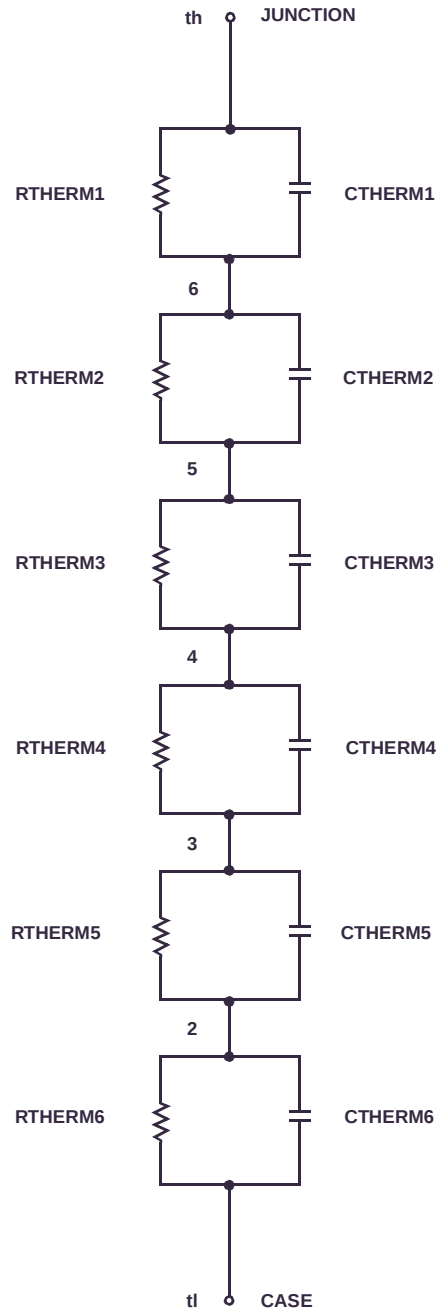
RTHERM1 th 6 1.51e-2
 RTHERM2 6 5 1.51e-2
 RTHERM3 5 4 3.03e-2
 RTHERM4 4 3 6.05e-2
 RTHERM5 3 2 1.81e-1
 RTHERM6 2 tl 2.45e-1

SABER Thermal Model

SABER thermal model HUF76132

```
template thermal_model th tl
thermal_c th, tl
{
    ctherm.ctherm1 th 6 = 6.50e-3
    ctherm.ctherm2 6 5 = 1.18e-2
    ctherm.ctherm3 5 4 = 1.55e-2
    ctherm.ctherm4 4 3 = 1.85e-2
    ctherm.ctherm5 3 2 = 2.00e-2
    ctherm.ctherm6 2 tl = 2.50e-2

    rtherm.rtherm1 th 6 = 1.51e-2
    rtherm.rtherm2 6 5 = 1.51e-2
    rtherm.rtherm3 5 4 = 3.03e-2
    rtherm.rtherm4 4 3 = 6.05e-2
    rtherm.rtherm5 3 2 = 1.81e-1
    rtherm.rtherm6 2 tl = 2.45e-1
}
```



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