

75A, 30V, 0.009 Ohm, N-Channel, Logic Level UltraFET Power MOSFETs



These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process.

This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76137.

Ordering Information

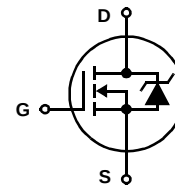
PART NUMBER	PACKAGE	BRAND
HUF76137P3	TO-220AB	76137P
HUF76137S3S	TO-263AB	76137S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF76137S3ST.

Features

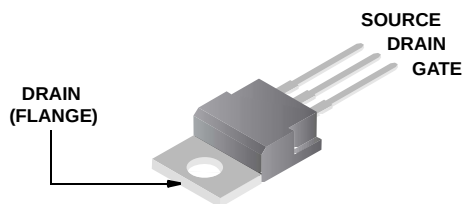
- Logic Level Gate Drive
- 75A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.009\Omega$
- Temperature Compensating PSpice™ Model
- Temperature Compensating SABER™ Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

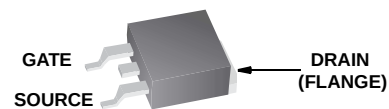


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



HUF76137P3, HUF76137S3S

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30 V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	30 V
Gate to Source Voltage	V_{GS}	± 16 V
Drain Current		
Continuous ($T_C = 25^{\circ}\text{C}$, $V_{GS} = 10\text{V}$) (Figure 2)	I_D	75 A
Continuous ($T_C = 100^{\circ}\text{C}$, $V_{GS} = 5\text{V}$)	I_D	55 A
Continuous ($T_C = 100^{\circ}\text{C}$, $V_{GS} = 4.5\text{V}$) (Figure 2)	I_D	52 A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	E_{AS}	Figures 6, 17, 18
Power Dissipation	P_D	145 W
Derate Above 25°C		1.16 W/ $^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-40 to 150 $^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_A = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25V, V _{GS} = 0V	-	-	1	μA
		V _{DS} = 25V, V _{GS} = 0V, T _C = 150 ⁰ C	-	-	250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V
Drain to Source On Resistance	r _{DS(ON)}	I _D = 75A, V _{GS} = 10V (Figures 9, 10)	-	0.0075	0.009	Ω
		I _D = 55A, V _{GS} = 5V (Figure 9)	-	0.010	0.0125	Ω
		I _D = 52A, V _{GS} = 4.5V (Figure 9)	-	0.011	0.014	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	-	-	0.86	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	TO-220 and TO-263	-	-	62	°C/W
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)						
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≅ 52A, R _L = 0.289Ω, V _{GS} = 4.5V, R _{GS} = 5.1Ω (Figures 15, 21, 22)	-	-	420	ns
Turn-On Delay Time	t _{d(ON)}		-	20	-	ns
Rise Time	t _r		-	260	-	ns
Turn-Off Delay Time	t _{d(OFF)}		-	28	-	ns
Fall Time	t _f		-	38	-	ns
Turn-Off Time	t _{OFF}		-	-	100	ns

HUF76137P3, HUF76137S3S

Electrical Specifications $T_A = 25^{\circ}\text{C}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≅ 75A, R _L = 0.20Ω, V _{GS} = 10V, R _{GS} = 5.6Ω (Figures 16, 21, 22)		-	-	225	ns
Turn-On Delay Time	t _{d(ON)}			-	10	-	ns
Rise Time	t _r			-	140	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	45	-	ns
Fall Time	t _f			-	35	-	ns
Turn-Off Time	t _{OFF}			-	-	120	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 15V, I _D ≅ 55A, R _L = 0.273Ω I _{g(REF)} = 1.0mA (Figures 14, 19, 20)	-	55	72	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	31	40	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	2.2	2.9	nC
Gate to Source Gate Charge	Q _{gs}			-	6.00	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	15.50	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 13)		-	2100	-	pF
Output Capacitance	C _{OSS}			-	1050	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	225	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 55\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 55\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	77	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 55\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	143	nC

Typical Performance Curves

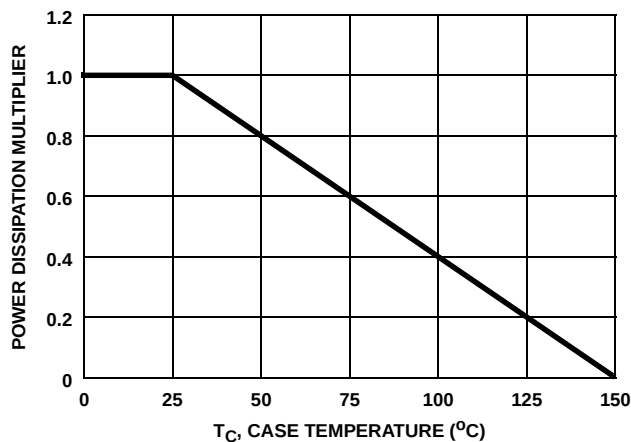


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

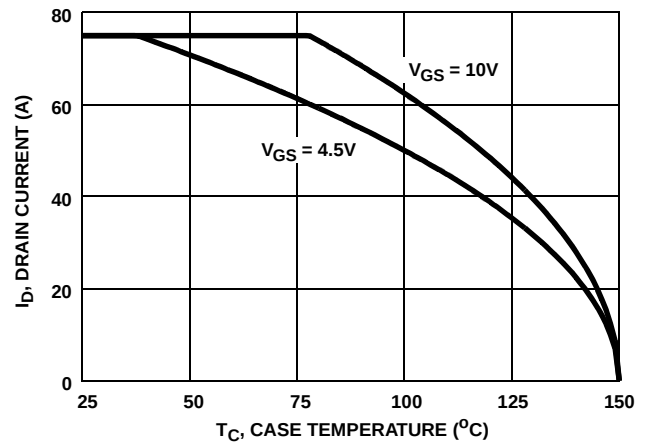
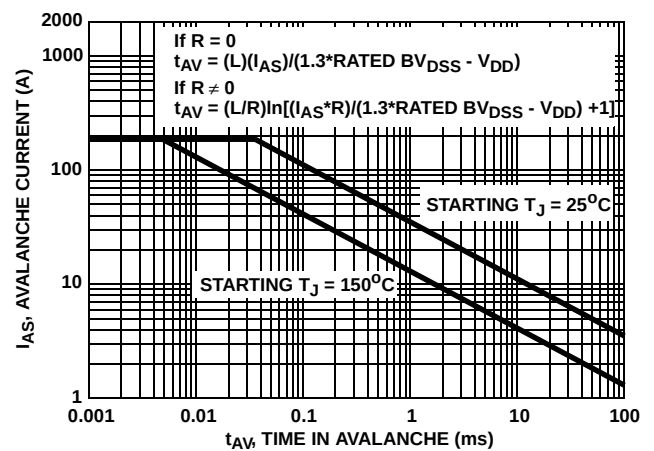
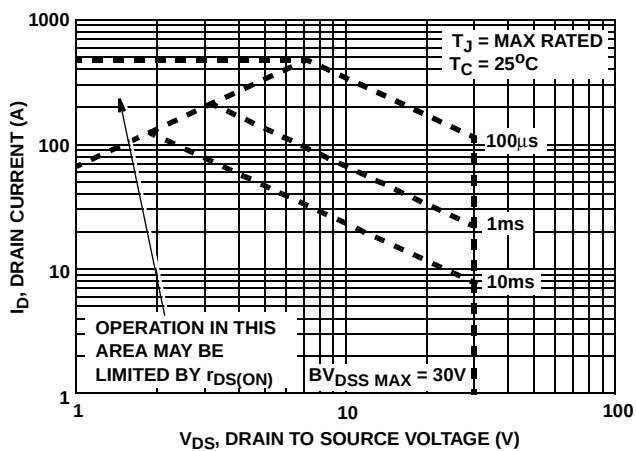
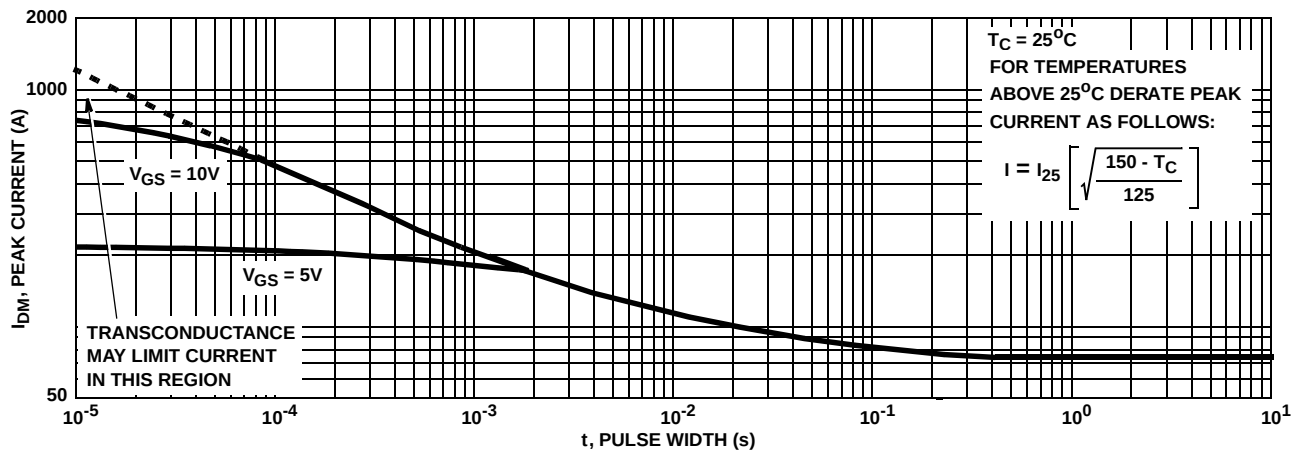
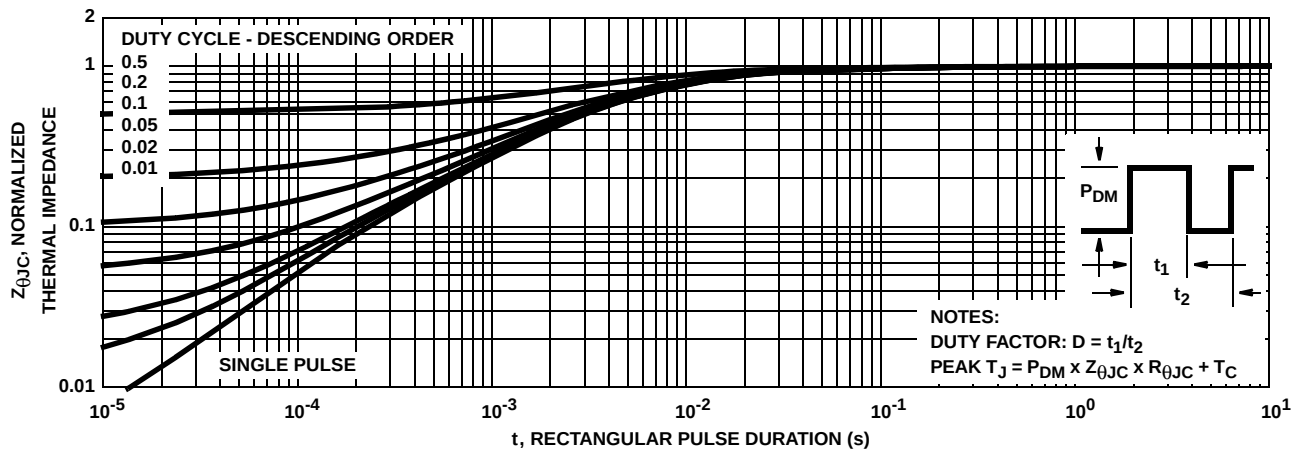


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

Typical Performance Curves (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

Typical Performance Curves (Continued)

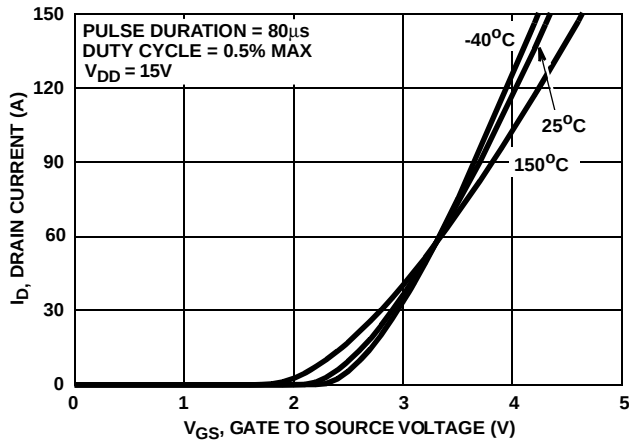


FIGURE 7. TRANSFER CHARACTERISTICS

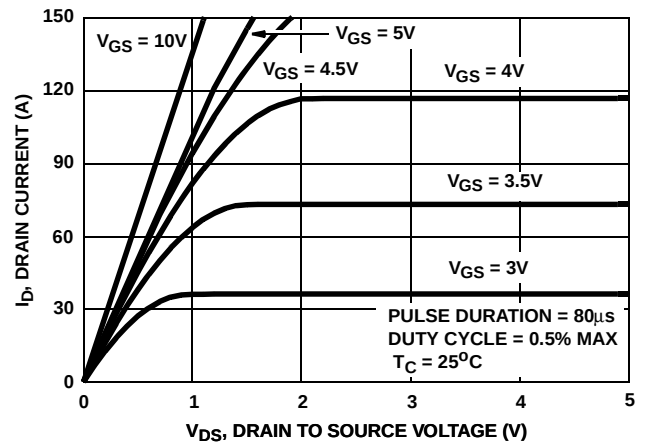


FIGURE 8. SATURATION CHARACTERISTICS

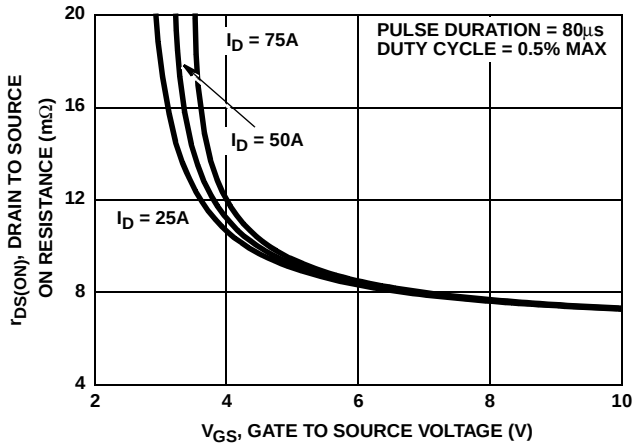


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

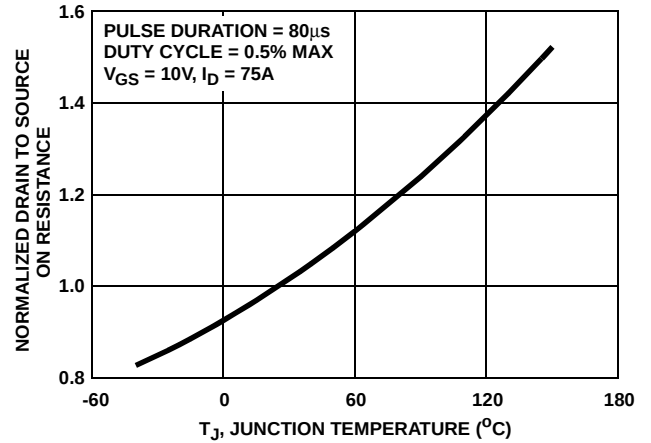


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

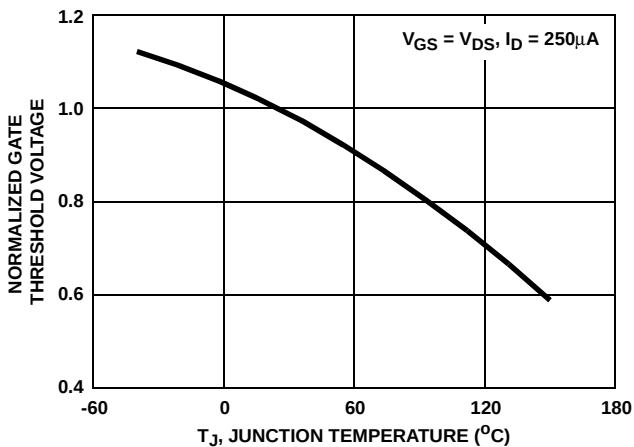


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

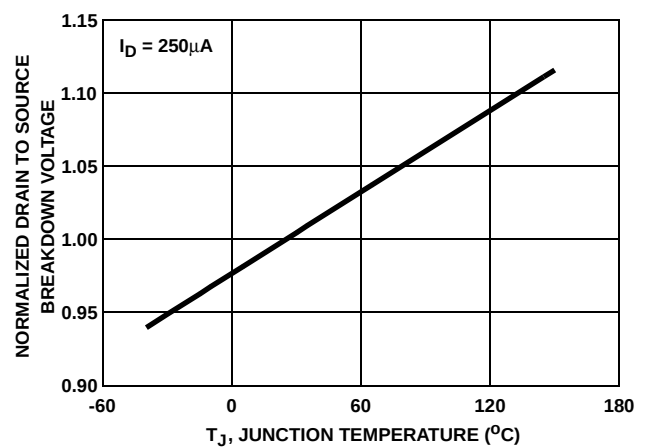


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

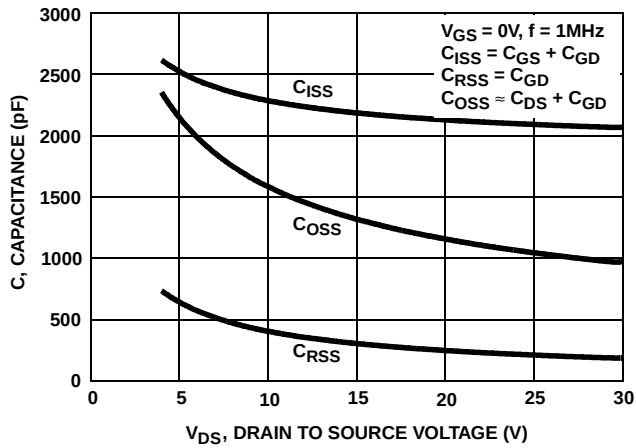
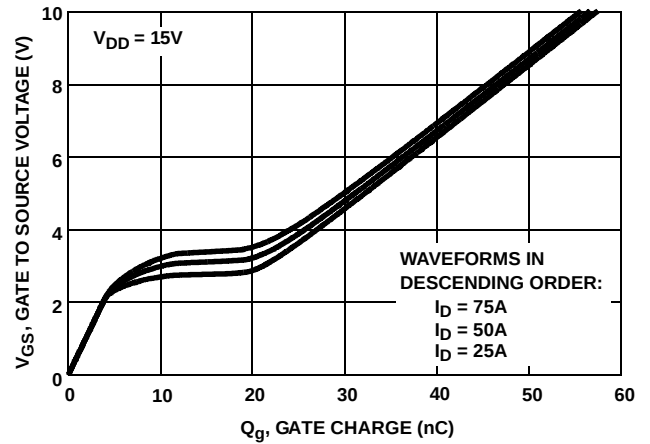


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

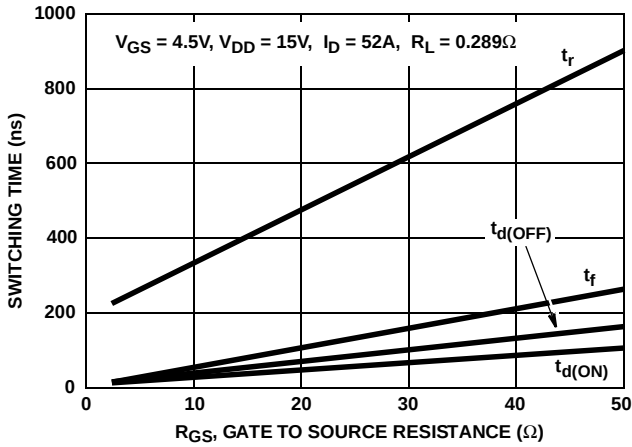


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

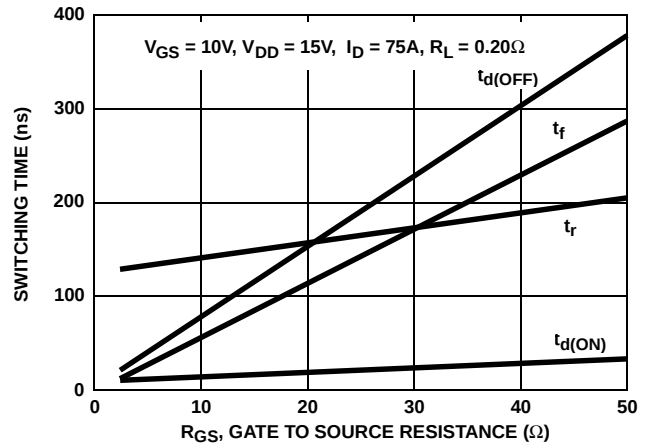


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

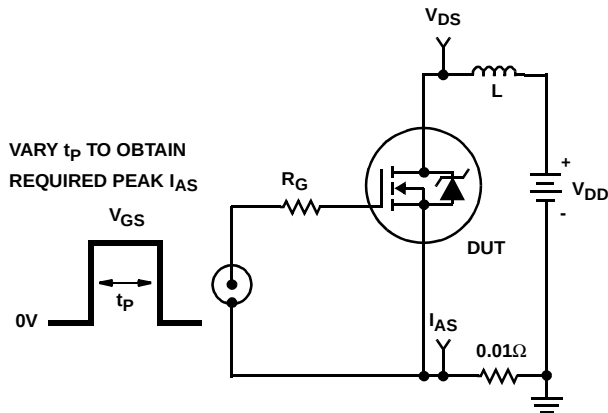


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

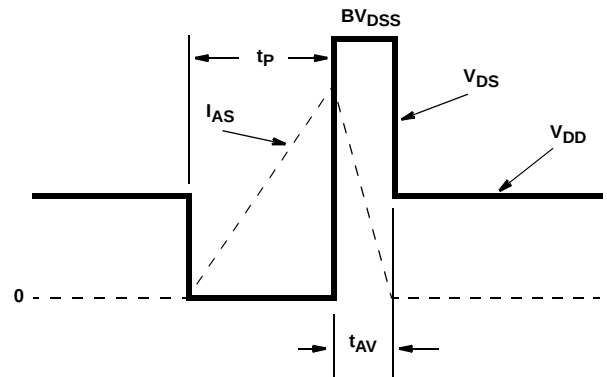


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

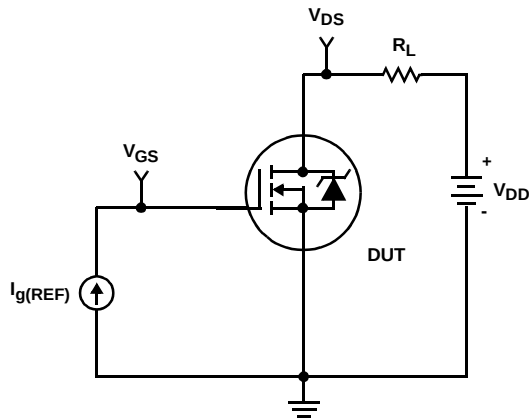


FIGURE 19. GATE CHARGE TEST CIRCUIT

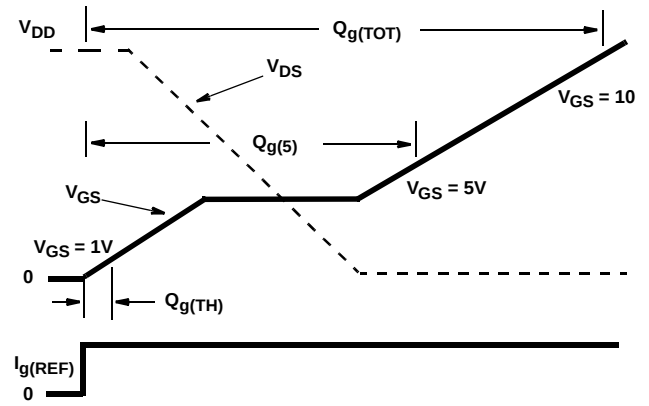


FIGURE 20. GATE CHARGE WAVEFORMS

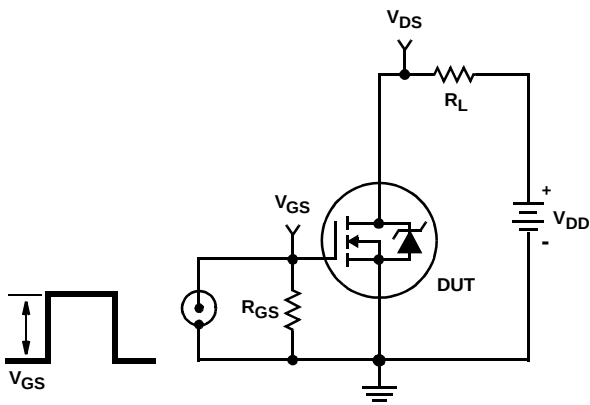


FIGURE 21. SWITCHING TIME TEST CIRCUIT

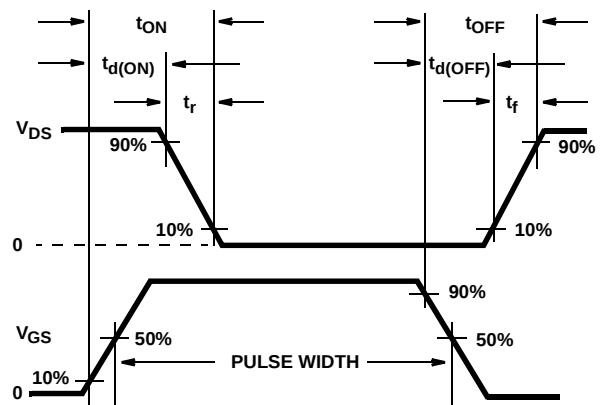
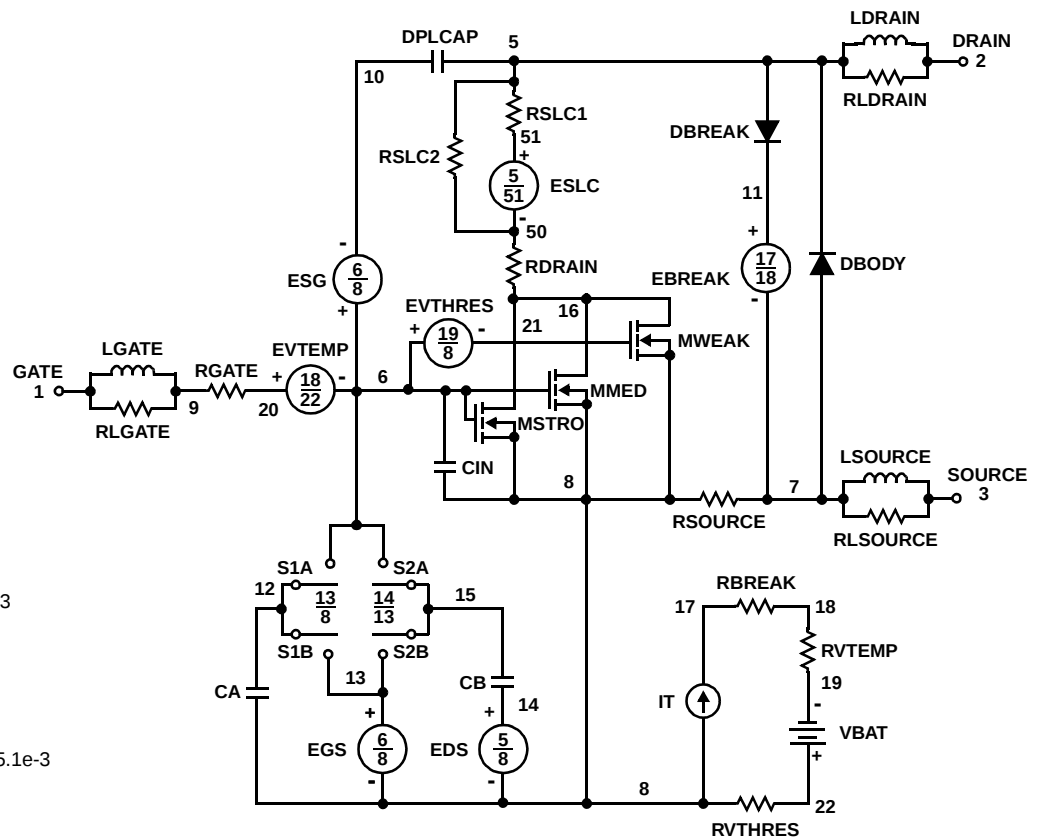


FIGURE 22. SWITCHING TIME WAVEFORM



SABER Electrical Model

nom temp=25 deg c 30v LL Ultrafet

REV May1998

template huf76137 n2,n1,n3

electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is=2.5e-12,xti=5.2,cjo=3.1e-9,tt=9e-8,m=4e-1)
d..model dbreakmod = ()
d..model dplcapmod = (cjo=2.5e-9,is=1e-30,n=10,m=7.5e-1)
m..model mmedmod = (type=_n,vto=1.73,kp=2,is=1e-30,tox=1)
m..model mstrongmod = (type=_n,vto=2.08,kp=130,is=1e-30,tox=1)
m..model mweakmod = (type=_n,vto=1.38,kp=1e-2,is=1e-30,tox=1)
sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-6.5,voff=-0.5)
sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-0.5,voff=-6.5)
sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-1.5,voff=0.5)
sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.5,voff=-1.5)
```

```
c.ca n12 n8 = 3.1e-9
c.cb n15 n14 = 3.1e-9
c.cin n6 n8 = 1.88e-9
```

```
d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod
```

i.it n8 n17 = 1

```
l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 6.73e-9
l.lsource n3 n7 = 26.3e-9
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
```

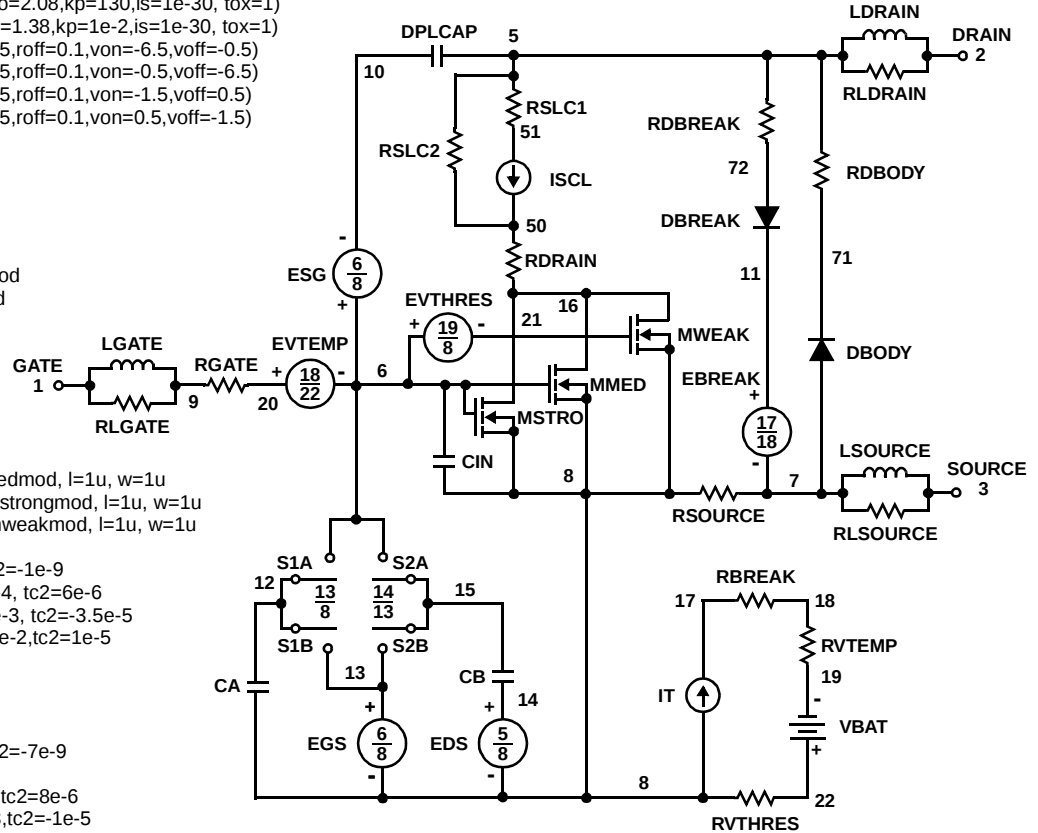
```
res.rbreak n17 n18 = 1, tc1=1e-3,tc2=-1e-9
res.rbody n71 n5 = 3.65e-3, tc1=3e-4, tc2=6e-6
res.rdbreak n72 n5 = 1.25e-2, tc1=3e-3, tc2=-3.5e-5
res.rdrain n50 n16 = 1.2e-3, tc1=1.1e-2,tc2=1e-5
res.rgate n9 n20 = 1
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 67.3
res.rlsource n3 n7 = 26.3
res.rslc1 n5 n51 = 1e-6, tc1=7e-3,tc2=-7e-9
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 5.1e-3, tc1=e-3,tc2=8e-6
res.rvtemp n18 n19 = 1, tc1=-1.8e-3,tc2=-1e-5
res.rvthres n22 n8 = 1, tc1=-1.65e-3,tc2=-1e-6
```

```
spe.ebreak n11 n7 n17 n18 = 33.7
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
```

```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

v.vbat n22 n19 = dc=1

```
equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = (((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51))*1e6/500)** 4))
}
}
```



SPICE Thermal Model

REV May 1998

HUF76137

CTHERM1 th 6 1.0e-6
 CTHERM2 6 5 2.0e-6
 CTHERM3 5 4 6.0e-3
 CTHERM4 4 3 9.5e-3
 CTHERM5 3 2 3.0e-2
 CTHERM6 2 tl 1.8

RTHERM1 th 6 1.0e-4
 RTHERM2 6 5 1.4e-3
 RTHERM3 5 4 2.9e-2
 RTHERM4 4 3 1.8e-1
 RTHERM5 3 2 2.6e-1
 RTHERM6 2 tl 4.0e-2

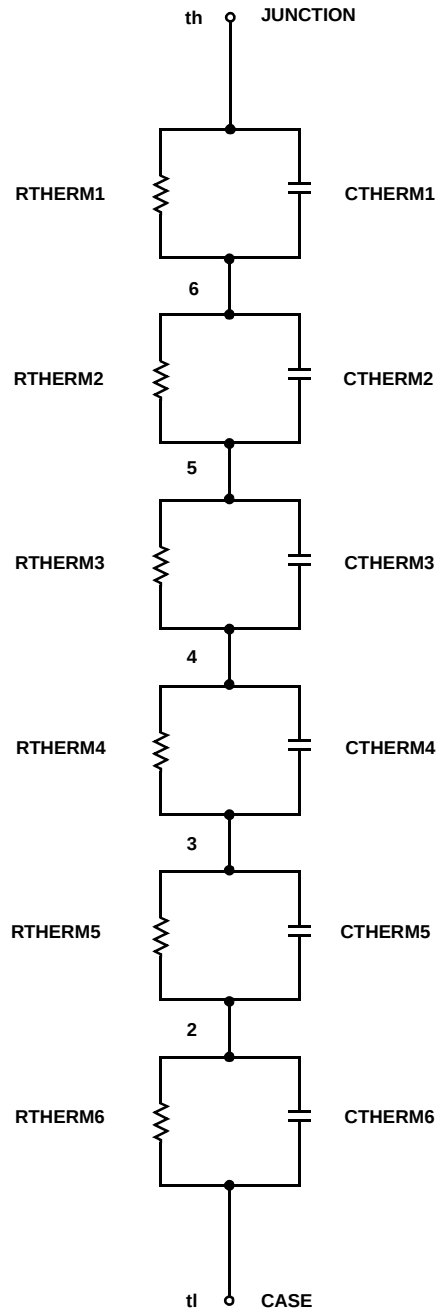
SABER Thermal Model

Saber thermal model HUF76137

template thermal_model th tl
 thermal_c th, tl

```
{
    ctherm.ctherm1 th 6 = 1.0e-6
    ctherm.ctherm2 6 5 = 2.0e-6
    ctherm.ctherm3 5 4 = 6.0e-3
    ctherm.ctherm4 4 3 = 9.5e-3
    ctherm.ctherm5 3 2 = 3.0e-2
    ctherm.ctherm6 2 tl = 1.8
```

```
    rtherm.rtherm1 th 6 = 1.0e-4
    rtherm.rtherm2 6 5 = 1.4e-3
    rtherm.rtherm3 5 4 = 2.9e-2
    rtherm.rtherm4 4 3 = 1.8e-1
    rtherm.rtherm5 3 2 = 2.6e-1
    rtherm.rtherm6 2 tl = 4.0e-2
}
```



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CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POP TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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