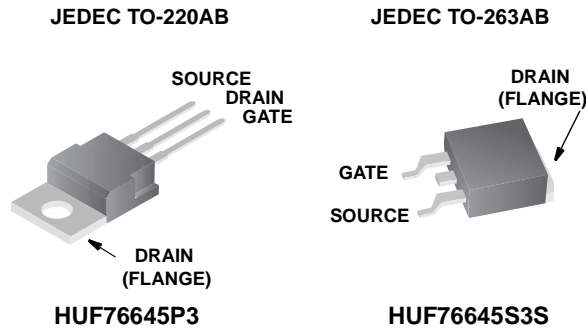


75A, 100V, 0.015 Ohm, N-Channel, Logic Level UltraFET® Power MOSFET



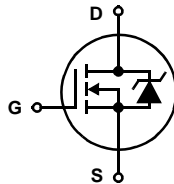
Packaging



Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.014\Omega, V_{GS} = 10V$
 - $r_{DS(ON)} = 0.015\Omega, V_{GS} = 5V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - Spice and SABER Thermal Impedance Models
 - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Symbol



Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|-------------|----------|--------|
| HUF76645P3 | TO-220AB | 76645P |
| HUF76645S3S | TO-263AB | 76645S |

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF76645S3ST.

Absolute Maximum Ratings $T_C = 25^\circ C$, Unless Otherwise Specified

| | HUF76645P3, HUF76645S3S | UNITS |
|--|----------------------------|---------------|
| Drain to Source Voltage (Note 1) | 100 | V |
| Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1) | 100 | V |
| Gate to Source Voltage | ± 16 | V |
| Drain Current | | |
| Continuous ($T_C = 25^\circ C, V_{GS} = 5V$) | 75 | A |
| Continuous ($T_C = 25^\circ C, V_{GS} = 10V$) (Figure 2) | 75 | A |
| Continuous ($T_C = 100^\circ C, V_{GS} = 5V$) | 63 | A |
| Continuous ($T_C = 100^\circ C, V_{GS} = 4.5V$) (Figure 2) | 62 | A |
| Pulsed Drain Current | Figure 4 | |
| Pulsed Avalanche Rating | Figures 6, 17, 18 | |
| Power Dissipation | 310 | W |
| Derate Above $25^\circ C$ | 2.07 | W/ $^\circ C$ |
| Operating and Storage Temperature | -55 to 175 | $^\circ C$ |
| Maximum Temperature for Soldering | | |
| Leads at 0.063in (1.6mm) from Case for 10s. | 300 | $^\circ C$ |
| Package Body for 10s, See Techbrief TB334. | 260 | $^\circ C$ |

NOTES:

1. $T_J = 25^\circ C$ to $150^\circ C$.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>

For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUF76645P3, HUF76645S3S

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|-----------------|---|--|--------|-----------|--------------------|----|
| OFF STATE SPECIFICATIONS | | | | | | | |
| Drain to Source Breakdown Voltage | BV_{DSS} | $I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 12) | 100 | - | - | V | |
| | | $I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_C = -40^\circ\text{C}$ (Figure 12) | 90 | - | - | V | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 95\text{V}$, $V_{GS} = 0\text{V}$ | - | - | 1 | μA | |
| | | $V_{DS} = 90\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$ | - | - | 250 | μA | |
| Gate to Source Leakage Current | I_{GSS} | $V_{GS} = \pm 16\text{V}$ | - | - | ± 100 | nA | |
| ON STATE SPECIFICATIONS | | | | | | | |
| Gate to Source Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ (Figure 11) | 1 | - | 3 | V | |
| Drain to Source On Resistance | $r_{DS(ON)}$ | $I_D = 75\text{A}$, $V_{GS} = 10\text{V}$ (Figures 9, 10) | - | 0.012 | 0.014 | Ω | |
| | | $I_D = 63\text{A}$, $V_{GS} = 5\text{V}$ (Figure 9) | - | 0.013 | 0.015 | Ω | |
| | | $I_D = 62\text{A}$, $V_{GS} = 4.5\text{V}$ (Figure 9) | - | 0.0135 | 0.0155 | Ω | |
| THERMAL SPECIFICATIONS | | | | | | | |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | TO-220 and TO-263 | - | - | 0.48 | $^\circ\text{C/W}$ | |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | | - | - | 62 | $^\circ\text{C/W}$ | |
| SWITCHING SPECIFICATIONS ($V_{GS} = 4.5\text{V}$) | | | | | | | |
| Turn-On Time | t_{ON} | $V_{DD} = 50\text{V}$, $I_D = 62\text{A}$ $V_{GS} = 4.5\text{V}$, $R_{GS} = 2.4\Omega$ (Figures 15, 21, 22) | - | - | 490 | ns | |
| Turn-On Delay Time | $t_{d(ON)}$ | | - | 17 | - | ns | |
| Rise Time | t_r | | - | 310 | - | ns | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | - | 46 | - | ns | |
| Fall Time | t_f | | - | 155 | - | ns | |
| Turn-Off Time | t_{OFF} | | - | - | 300 | ns | |
| SWITCHING SPECIFICATIONS ($V_{GS} = 10\text{V}$) | | | | | | | |
| Turn-On Time | t_{ON} | $V_{DD} = 50\text{V}$, $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 2.4\Omega$ (Figures 16, 21, 22) | - | - | 175 | ns | |
| Turn-On Delay Time | $t_{d(ON)}$ | | - | 11 | - | ns | |
| Rise Time | t_r | | - | 106 | - | ns | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | - | 69 | - | ns | |
| Fall Time | t_f | | - | 175 | - | ns | |
| Turn-Off Time | t_{OFF} | | - | - | 365 | ns | |
| GATE CHARGE SPECIFICATIONS | | | | | | | |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS} = 0\text{V to } 10\text{V}$ | $V_{DD} = 50\text{V}$, $I_D = 63\text{A}$, $I_{g(REF)} = 1.0\text{mA}$ (Figures 14, 19, 20) | - | 127 | 153 | nC |
| Gate Charge at 5V | $Q_{g(5)}$ | $V_{GS} = 0\text{V to } 5\text{V}$ | | - | 70 | 84 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS} = 0\text{V to } 1\text{V}$ | | - | 3.8 | 4.6 | nC |
| Gate to Source Gate Charge | Q_{gs} | | | - | 10 | - | nC |
| Gate to Drain "Miller" Charge | Q_{gd} | | | - | 34 | - | nC |
| CAPACITANCE SPECIFICATIONS | | | | | | | |
| Input Capacitance | C_{ISS} | $V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 13) | - | 4400 | - | pF | |
| Output Capacitance | C_{OSS} | | - | 900 | - | pF | |
| Reverse Transfer Capacitance | C_{RSS} | | - | 280 | - | pF | |

Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|----------|--|-----|-----|------|-------|
| Source to Drain Diode Voltage | V_{SD} | $I_{SD} = 63\text{A}$ | - | - | 1.25 | V |
| | | $I_{SD} = 30\text{A}$ | - | - | 1.0 | V |
| Reverse Recovery Time | t_{rr} | $I_{SD} = 63\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | - | - | 128 | ns |
| Reverse Recovered Charge | Q_{RR} | $I_{SD} = 63\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | - | - | 520 | nC |

Typical Performance Curves

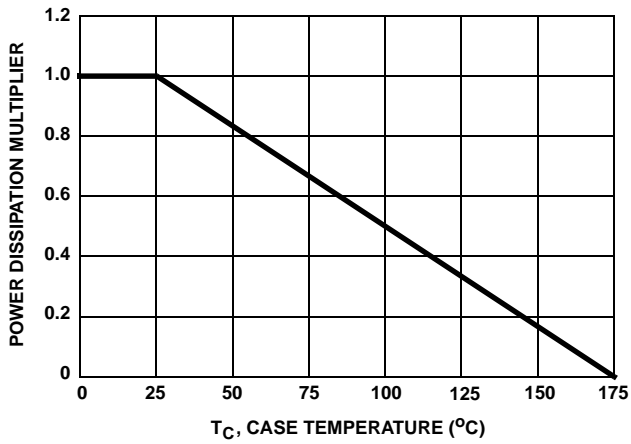


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

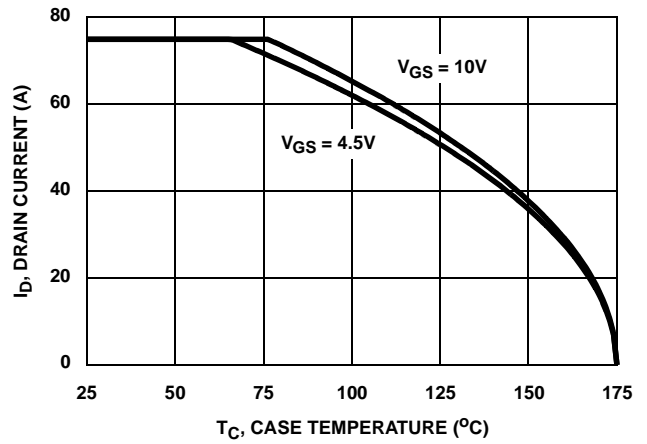


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

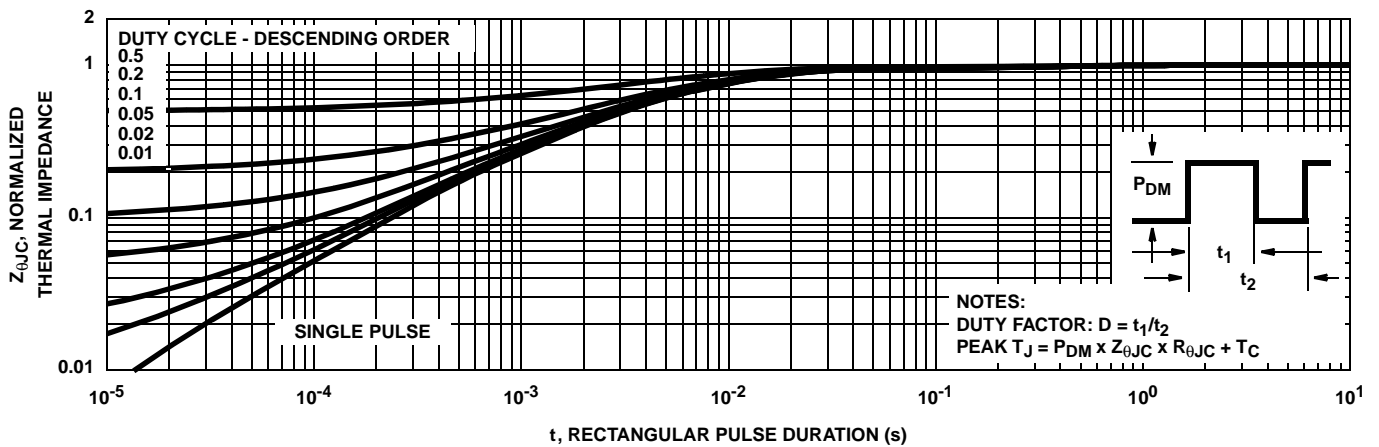


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

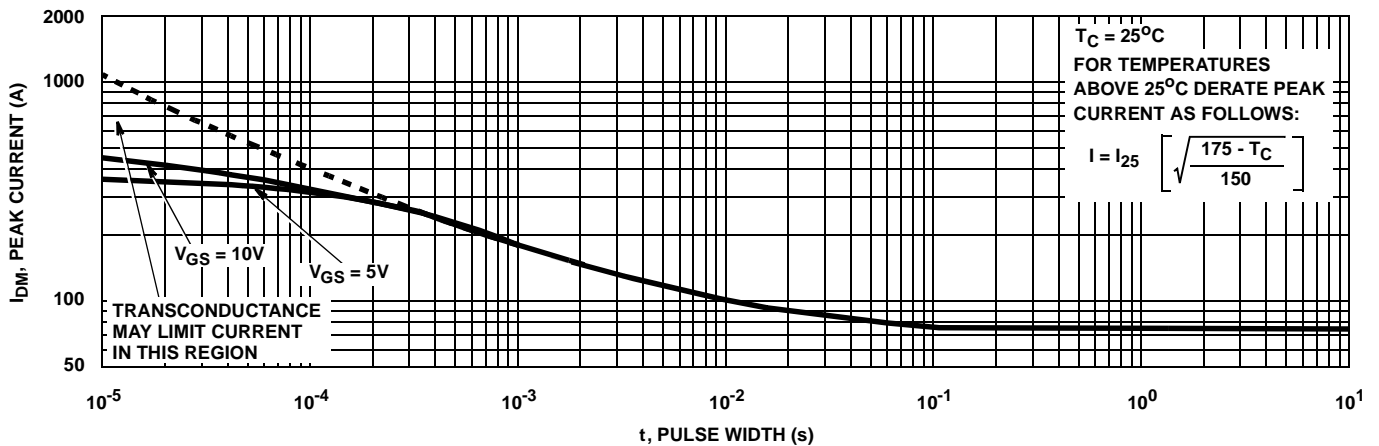


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

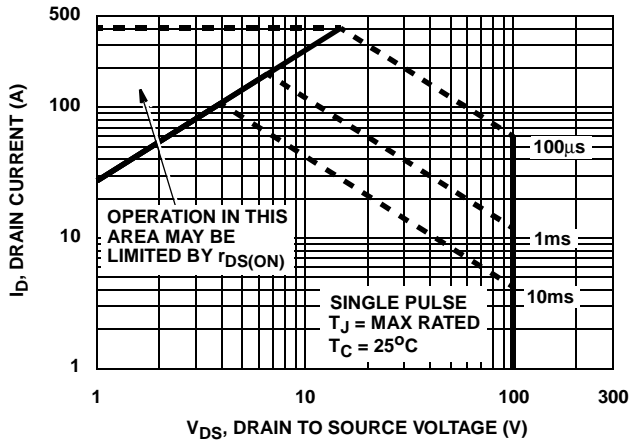
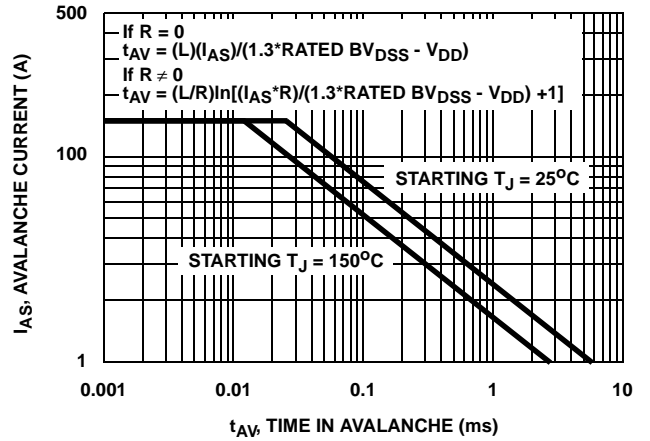


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

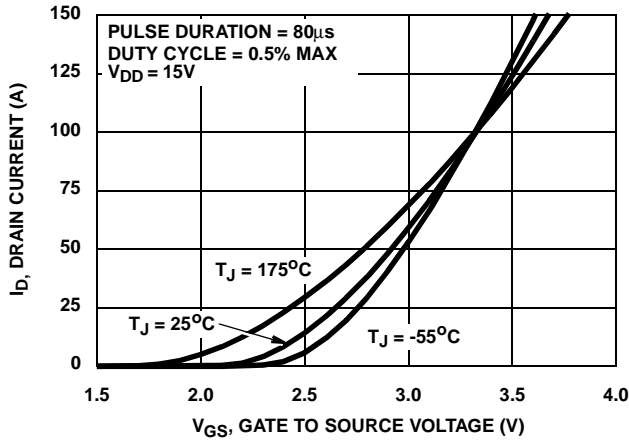


FIGURE 7. TRANSFER CHARACTERISTICS

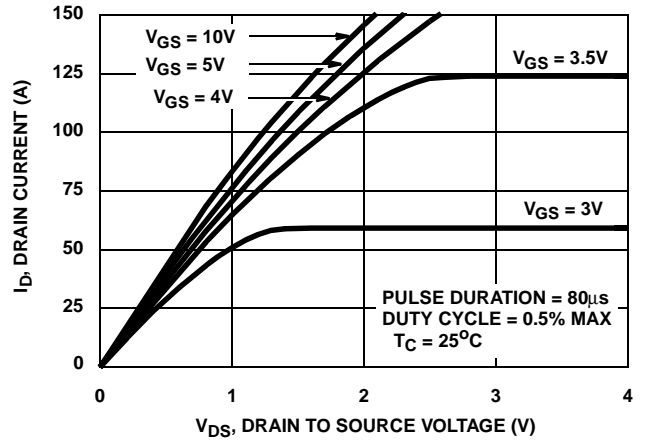


FIGURE 8. SATURATION CHARACTERISTICS

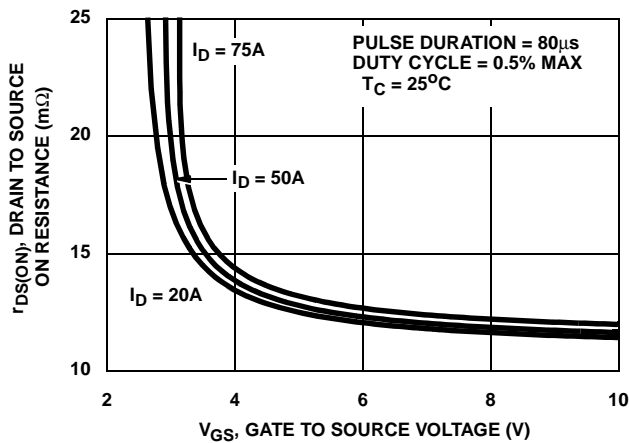


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs. GATE VOLTAGE AND DRAIN CURRENT

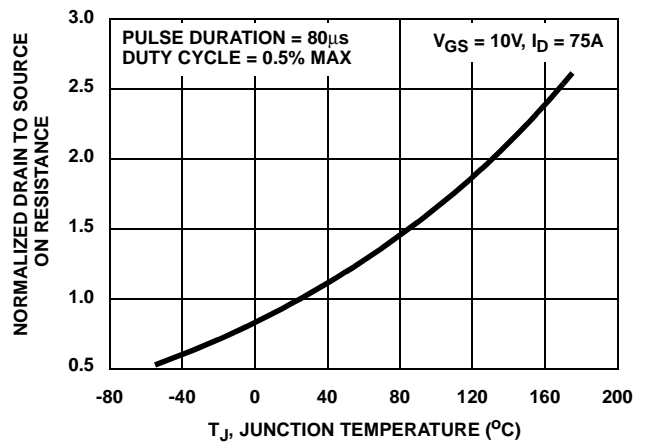


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs. JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

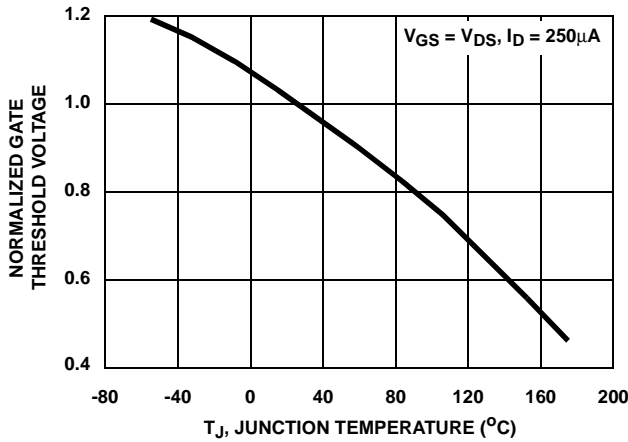


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

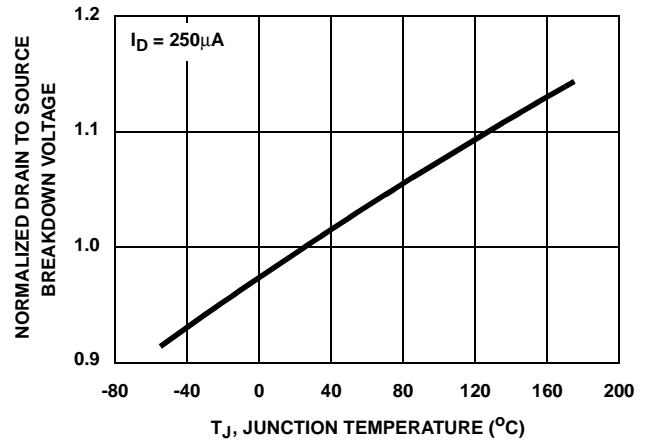


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

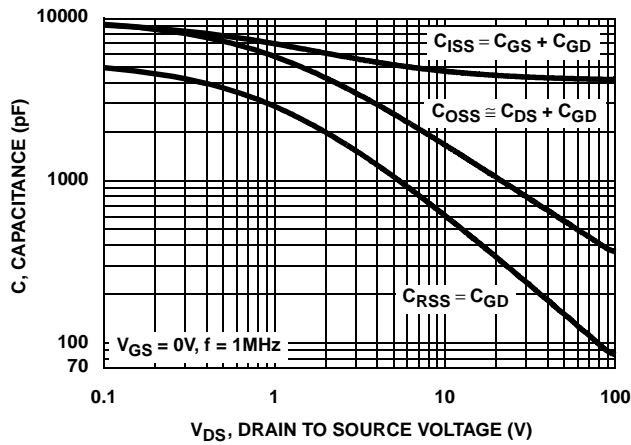
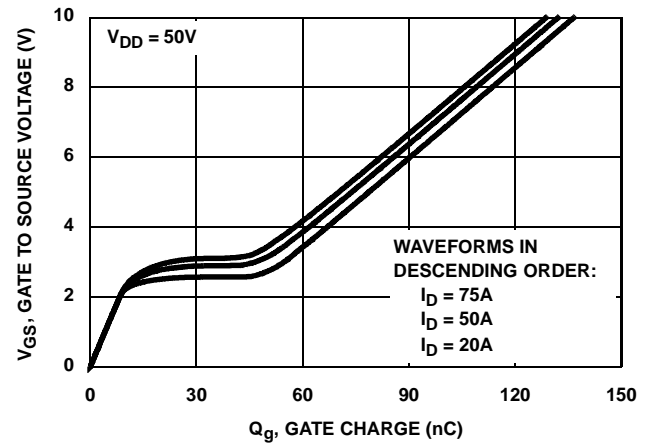


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

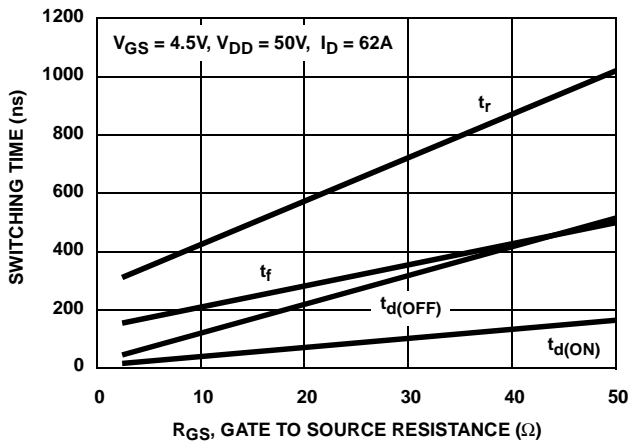


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

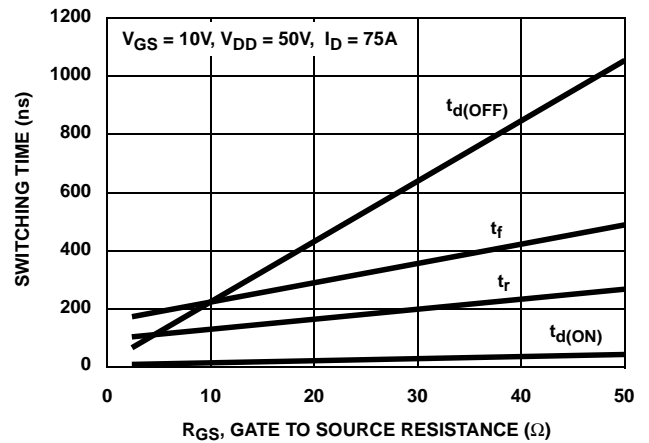


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

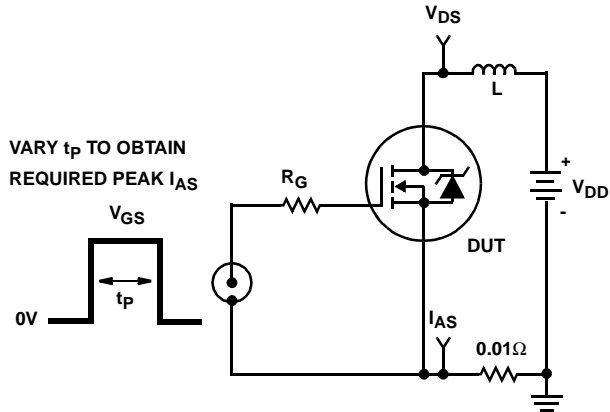


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

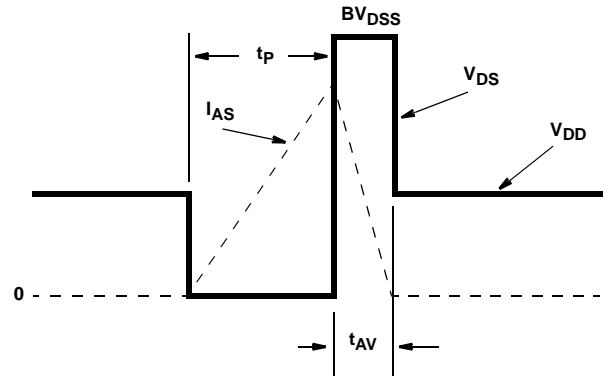


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

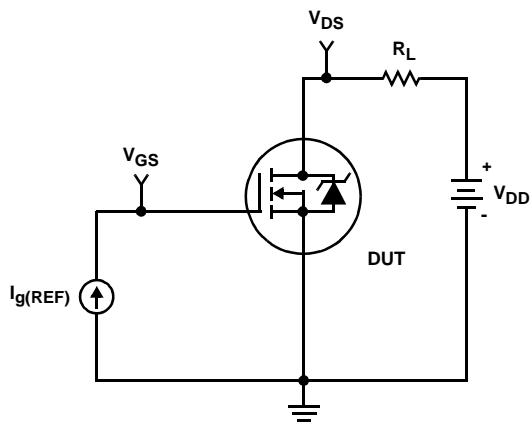


FIGURE 19. GATE CHARGE TEST CIRCUIT

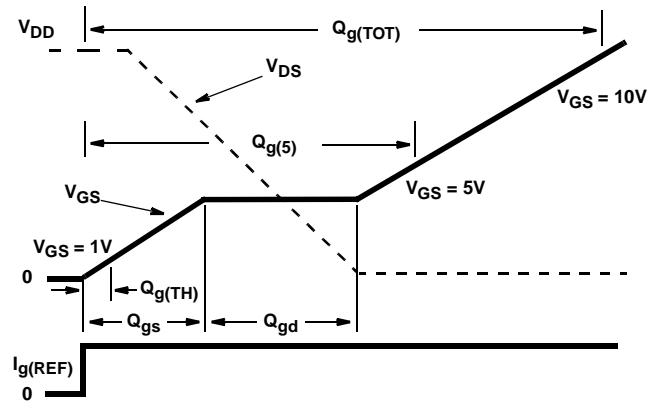


FIGURE 20. GATE CHARGE WAVEFORMS

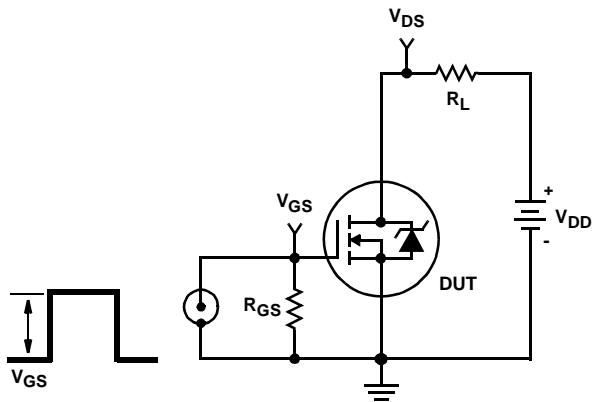


FIGURE 21. SWITCHING TIME TEST CIRCUIT

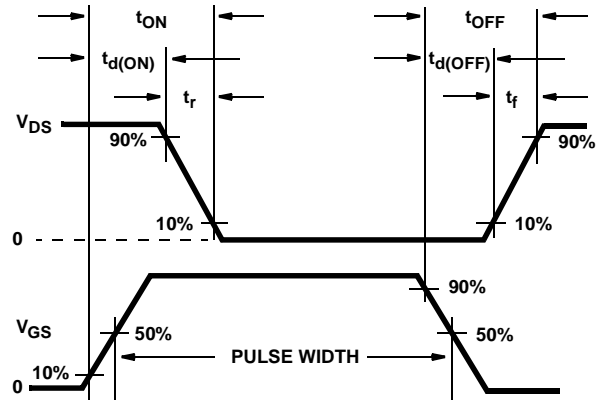


FIGURE 22. SWITCHING TIME WAVEFORM

HUF76645P3, HUF76645S3S

PSPICE Electrical Model

.SUBCKT HUF76645 2 1 3 ; rev 7 June 1999

CA 12 8 7.4e-9
 CB 15 14 7.4e-9
 CIN 6 8 4.13e-9

DBODY 7 5 DBODYMOD
 DBREAK 5 11 DBREAKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 121
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTHRES 6 21 19 8 1
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
 LGATE 1 9 5.1e-9
 LSOURCE 3 7 4.4e-9

MMED 16 6 8 8 MMEDMOD
 MSTRO 16 6 8 8 MSTROMOD
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 50 16 RDRAINMOD 8.3e-3
 RGATE 9 20 0.96
 RLDRAIN 2 5 10
 RLGATE 1 9 51
 RLSOURCE 3 7 4.4
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 RSOURCE 8 7 RSOURCEMOD 2.5e-3
 RVTHRES 22 8 RVTHRESMOD 1
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

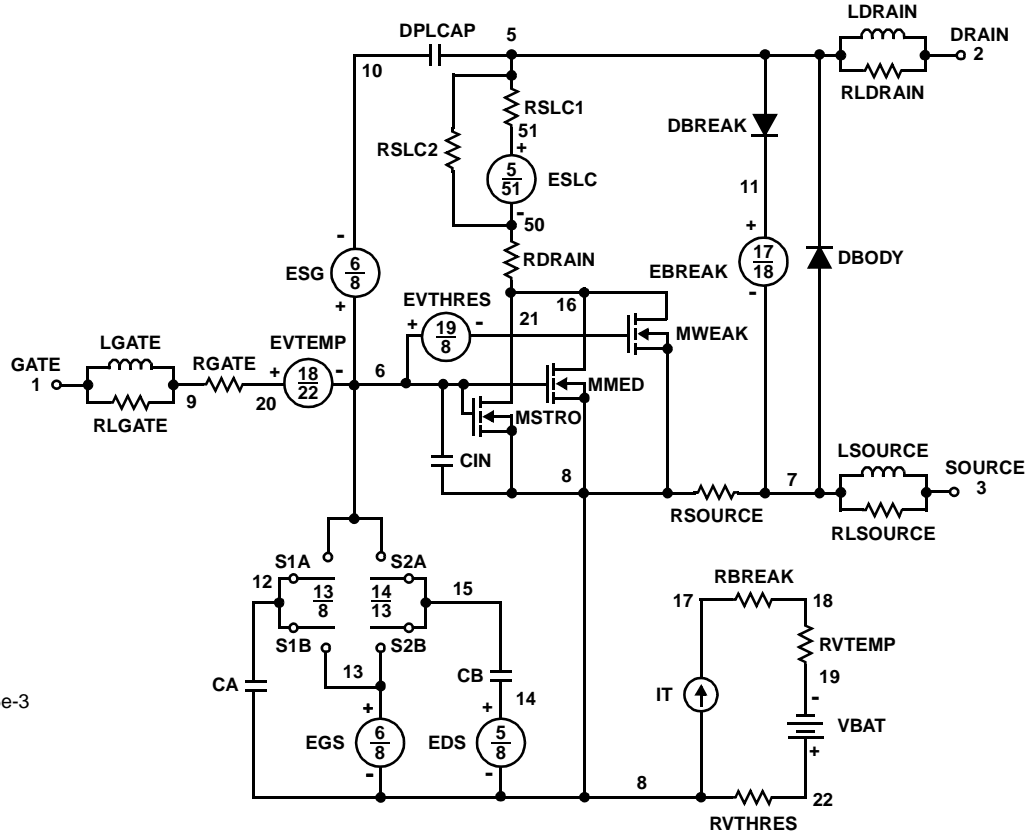
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51))/(1e-6*200),3.2))}

.MODEL DBODYMOD D (IS = 3.6e-12 RS = 2.24e-3 TRS1 = 2e-3 TRS2 = 1.03e-6 CJO = 4.5e-9 TT = 5.1e-8 M = 0.60)
 .MODEL DBREAKMOD D (RS = 2.5e-1 TRS1 = 1e-4 TRS2 = 1e-7)
 .MODEL DPLCAPMOD D (CJO = 5.4e-9 9IS = 1e-3 0Vj = 1.0 M = 0.9)
 .MODEL MMEDMOD NMOS (VTO = 1.77 KP = 7 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.96)
 .MODEL MSTROMOD NMOS (VTO = 2.11 KP = 200 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
 .MODEL MWEAKMOD NMOS (VTO = 1.5 KP = 0.12 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 9.6 RS = 0.1)
 .MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = -5e-7)
 .MODEL RDRAINMOD RES (TC1 = 8.8e-3 TC2 = 1.7e-5)
 .MODEL RSLCMOD RES (TC1 = 4e-3 TC2 = 1.5e-5)
 .MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 2e-6)
 .MODEL RVTHRESMOD RES (TC1 = -1.9e-3 TC2 = -8e-6)
 .MODEL RVTEMPMOD RES (TC1 = -1.7e-3 TC2 = 1e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.5 VOFF = -2.0)
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF = -4.5)
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.0 VOFF = 0.5)
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -1.0)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV 7 June 1999

HUF76645T

CTHERM1 th 6 6.4e-3
 CTHERM2 6 5 3.0e-2
 CTHERM3 5 4 1.4e-2
 CTHERM4 4 3 1.6e-2
 CTHERM5 3 2 5.5e-2
 CTHERM6 2 tl 1.5

RTHERM1 th 6 3.4e-3
 RTHERM2 6 5 8.6e-3
 RTHERM3 5 4 2.3e-2
 RTHERM4 4 3 1.3e-1
 RTHERM5 3 2 1.8e-1
 RTHERM6 2 tl 3.9e-2

SABER Thermal Model

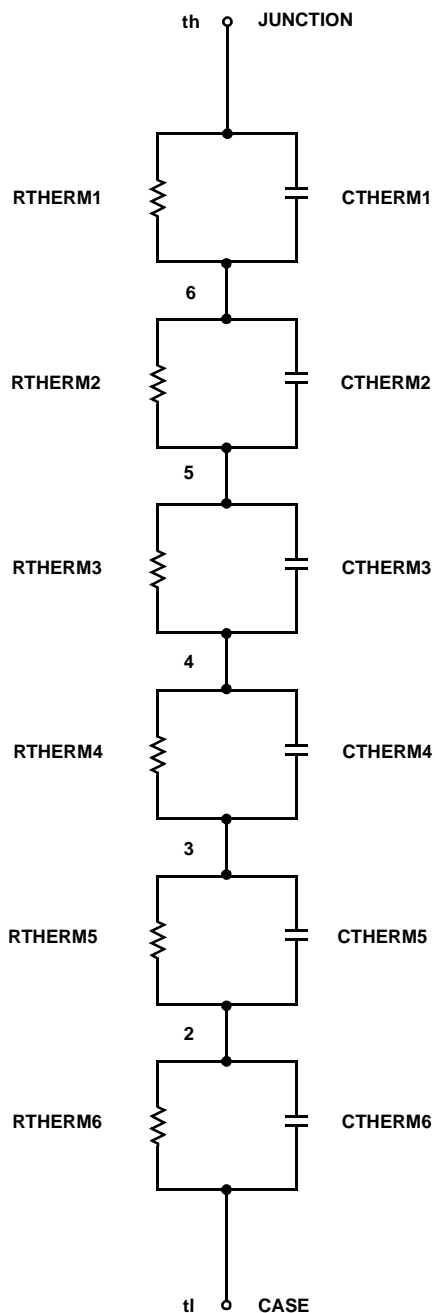
SABER thermal model HUF76645T

template thermal_model th tl
 thermal_c th, tl

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{
ctherm.ctherm1 th 6 = 6.4e-3
ctherm.ctherm2 6 5 = 3.0e-2
ctherm.ctherm3 5 4 = 1.4e-2
ctherm.ctherm4 4 3 = 1.6e-2
ctherm.ctherm5 3 2 = 5.5e-2
ctherm.ctherm6 2 tl = 1.5
```

```
rtherm.rtherm1 th 6 = 3.4e-3
rtherm.rtherm2 6 5 = 8.6e-3
rtherm.rtherm3 5 4 = 2.3e-2
rtherm.rtherm4 4 3 = 1.3e-1
rtherm.rtherm5 3 2 = 1.8e-1
rtherm.rtherm6 2 tl = 3.9e-2
```

```
}
```



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|-----------------------------------|----------------------------------|----------------------------------|------------------------------|-------------------|
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| Bottomless TM | FAST _r TM | OPTOPLANAR TM | STAR*POWER TM | |
| CoolFET TM | FRFET TM | PACMAN TM | Stealth TM | |
| CROSSVOLT TM | GlobalOptoisolator TM | POP TM | SuperSOT TM -3 | |
| DenseTrench TM | GTO TM | Power247 TM | SuperSOT TM -6 | |
| DOMET TM | HiSeC TM | PowerTrench [®] | SuperSOT TM -8 | |
| EcoSPARK TM | ISOPLANAR TM | QFET TM | SyncFET TM | |
| E ² CMOS TM | LittleFET TM | QST TM | TinyLogic TM | |
| EnSigna TM | MicroFET TM | QT Optoelectronics TM | TruTranslation TM | |
| FACT TM | MicroPak TM | Quiet Series TM | UHC TM | |
| FACT Quiet Series TM | MICROWIRE TM | SILENT SWITCHER [®] | UltraFET [®] | |

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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| Datasheet Identification | Product Status | Definition |
|--------------------------|------------------------|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
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| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
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