

31A, 100V, 0.077 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17421.

Ordering Information

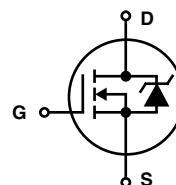
PART NUMBER	PACKAGE	BRAND
IRFP140	TO-247	IRFP140

NOTE: When ordering, include the entire part number.

Features

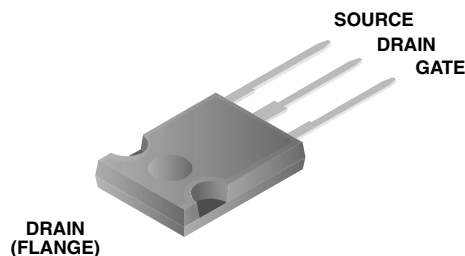
- 31A, 100V
- $r_{DS(ON)} = 0.077\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC STYLE TO-247



IRFP140

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

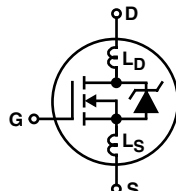
	IRFP140	UNITS
Drain to Source Voltage (Note 1)	V_{DS} 100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR} 100	V
Continuous Drain Current	I_D 31	A
$T_C = 100^\circ\text{C}$	I_D 22	A
Pulsed Drain Current (Note 3)	I_{DM} 120	A
Gate to Source Voltage	V_{GS} ± 20	V
Maximum Power Dissipation	P_D 180	W
Linear Derating Factor	1.2	W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS} 100	mJ
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L 300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg} 260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA (Figure 10)		100	-	-	V
Gate to Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA		2.0	-	4.0	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V		-	-	25	μA
		V _{DS} = 0.8 x Rated BV _{DSS} , V _{GS} = 0V, T _J = 125°C		-	-	250	μA
On-State Drain Current (Note 2)	I _{D(ON)}	V _{DS} > I _{D(ON)} x r _{DS(ON)MAX} ; V _{GS} = 10V		31	-	-	A
Gate to Source Leakage	I _{GSS}	V _{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	r _{DS(ON)}	V _{GS} = 10V, I _D = 19A (Figures 8, 9)		-	0.055	0.077	Ω
Forward Transconductance (Note 2)	g _{fs}	V _{DS} ≥ 50V, I _D = 19A (Figure 12)		9.3	14	-	S
Turn-On Delay Time	t _{d(ON)}	V _{DD} = 50V, I _D ≈ 28A, R _{GS} = 9.1Ω, R _L = 1.7Ω, V _{GS} = 10V MOSFET Switching Times are Essentially Independent of Operating Temperature	-	15	23	ns	
Rise Time	t _r		-	72	110	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	40	60	ns	
Fall Time	t _f		-	50	75	ns	
Total Gate Charge (Gate to Source + Gate to Drain)	Q _{g(TOT)}	V _{GS} = 10V, I _D ≈ 27A, V _{DS} = 0.8 x Rated BV _{DSS} , I _{G(REF)} = 1.5mA (Figure 14)		-	38	59	nC
Gate to Source Charge	Q _{gs}	Gate Charge is Essentially Independent of Operating Temperature		-	10	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	21	-	nC
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} ≈ 25V, f = 1.0MHz (Figure 11)		-	1275	-	pF
Output Capacitance	C _{OSS}			-	550	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	160	-	pF
Internal Drain Inductance	L _D	Measured between the Contact Screw on Header that is Closer to Source and Gate Pins and Center of Die		-	5.0	-	nH
Internal Source Inductance	L _S	Measured from the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	12.5	-	nH
Thermal Resistance Junction to Case	R _{θJC}			-	-	0.83	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	Free Air Operation		-	-	30	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode	-	-	31	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	120	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = 31\text{A}$, $V_{GS} = 0\text{V}$ (Figure 13)	-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_{SD} = 28\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	70	150	300	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^\circ\text{C}$, $I_{SD} = 28\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	0.44	0.91	1.9	μC

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
- $V_{DD} = 25\text{V}$, starting $T_J = 25^\circ\text{C}$, $L = 160\mu\text{H}$, $R_G = 50\Omega$, peak $I_{AS} = 31\text{A}$.

Typical Performance Curves Unless Otherwise Specified

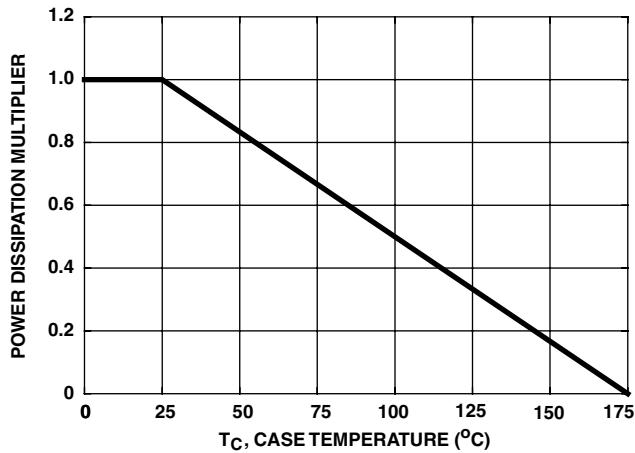


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

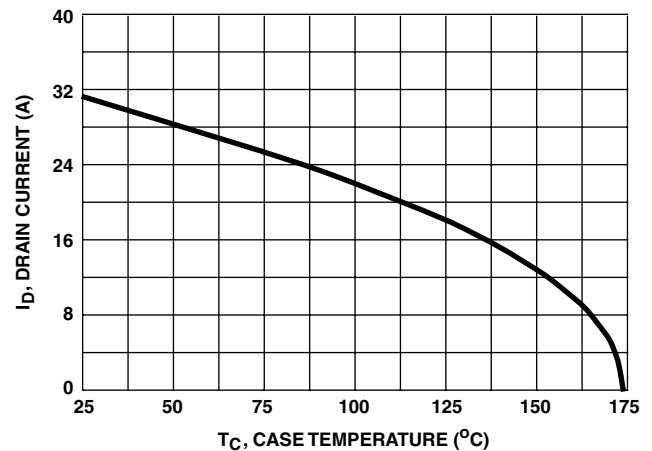


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

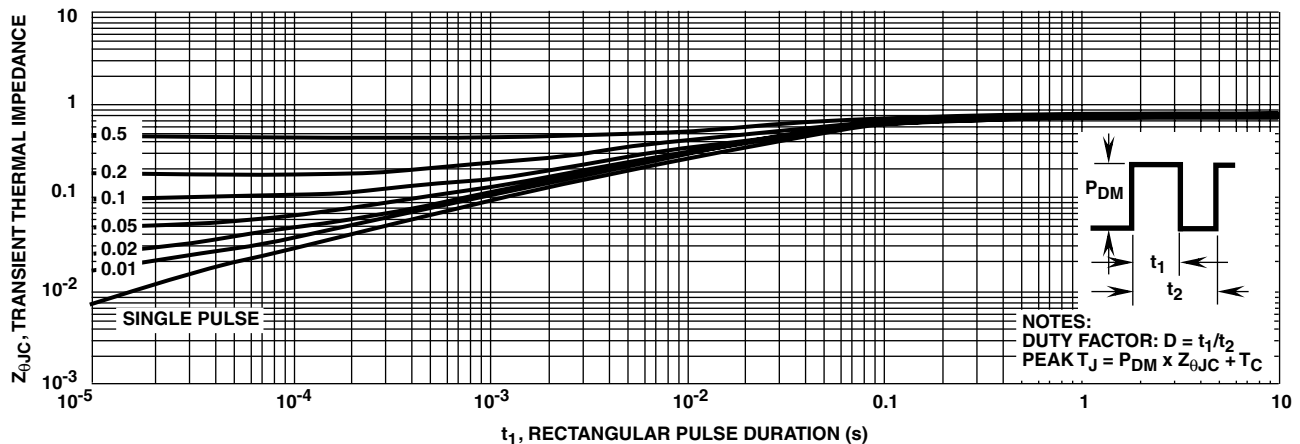


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

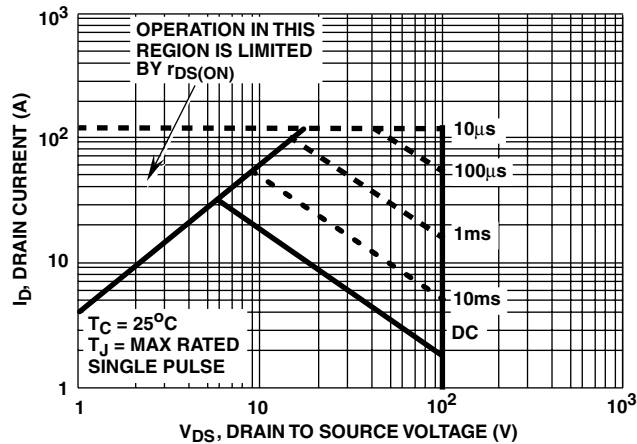


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

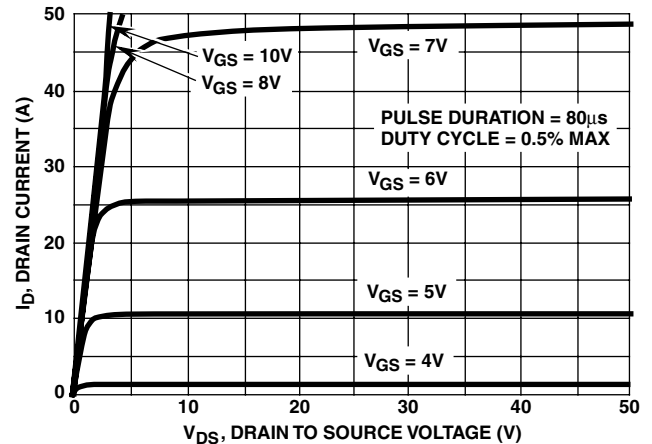


FIGURE 5. OUTPUT CHARACTERISTICS

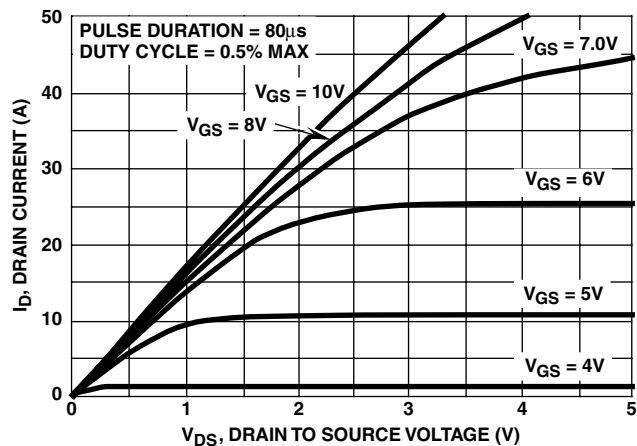


FIGURE 6. SATURATION CHARACTERISTICS

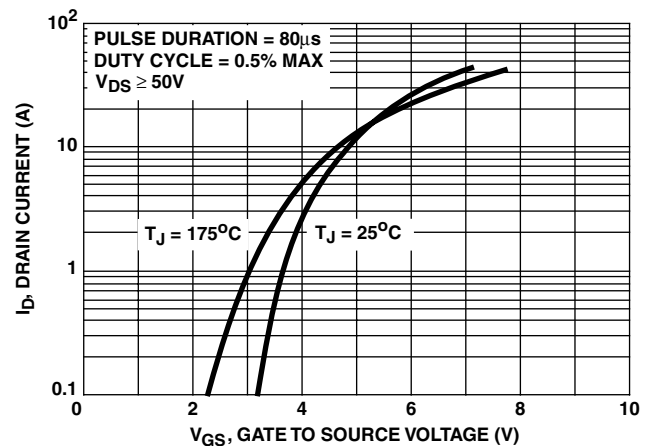
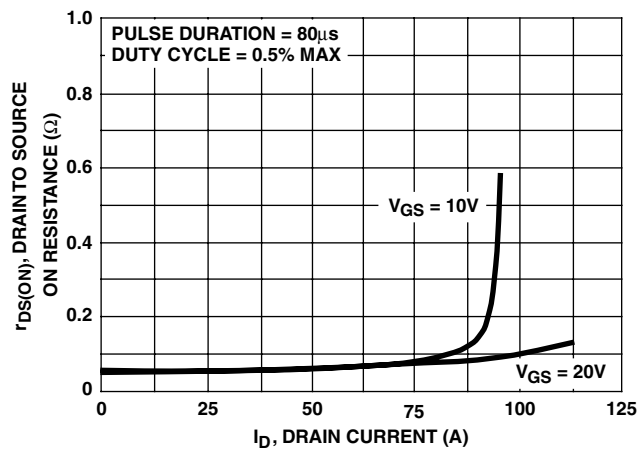


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2μs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

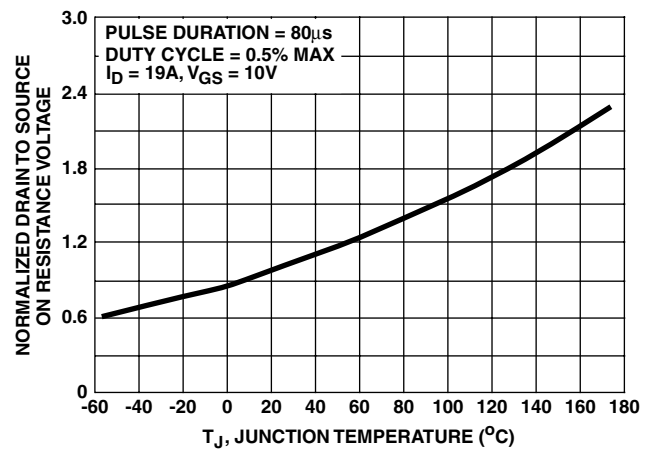


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

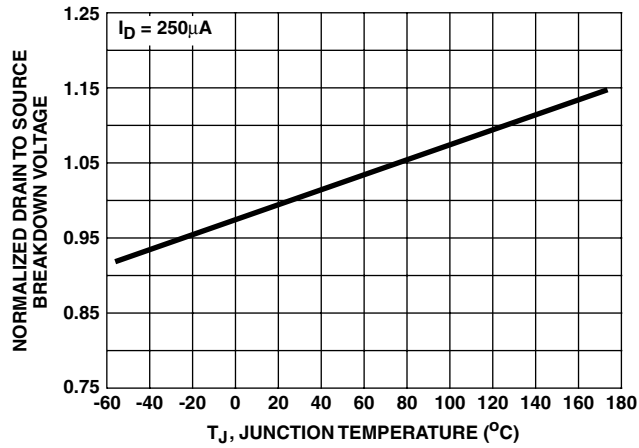


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

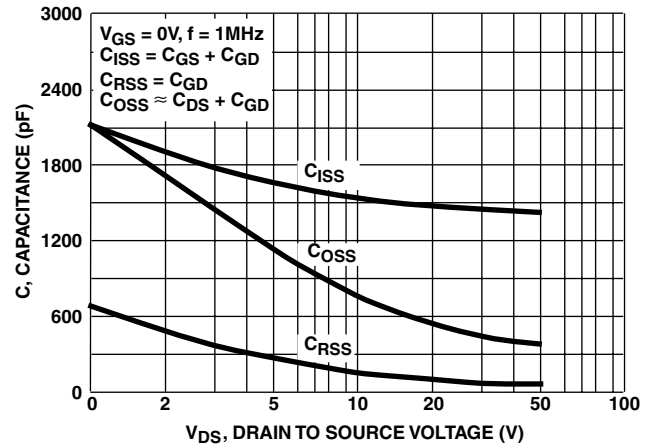


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

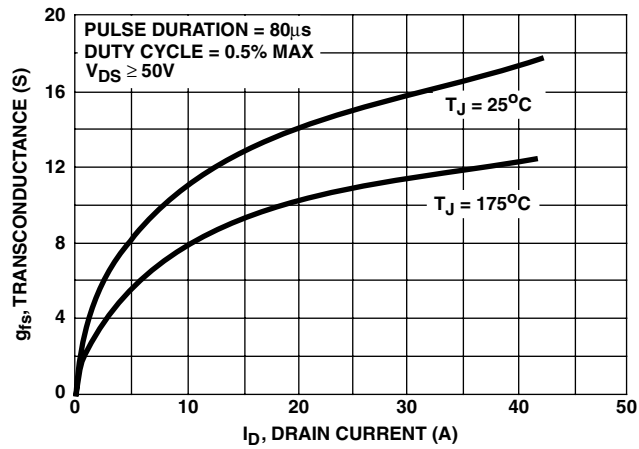


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

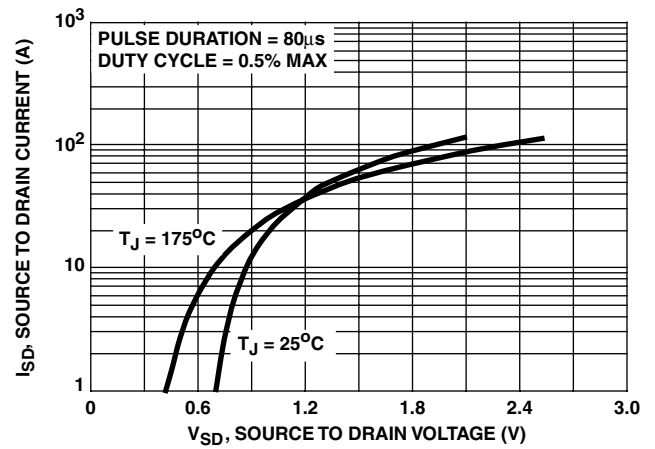


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

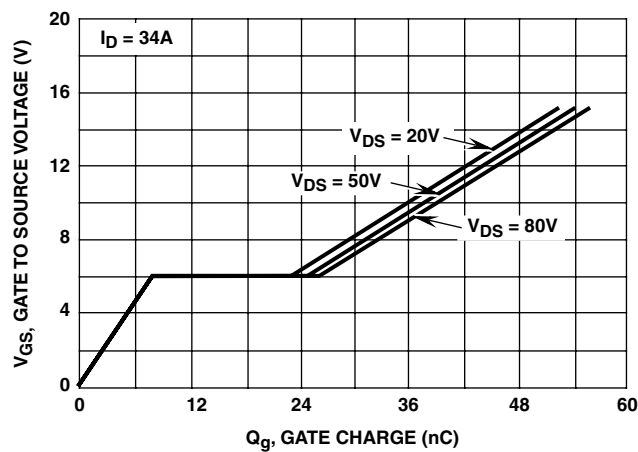


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

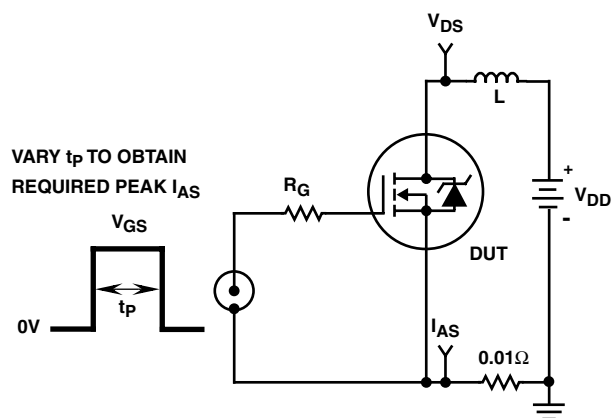


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

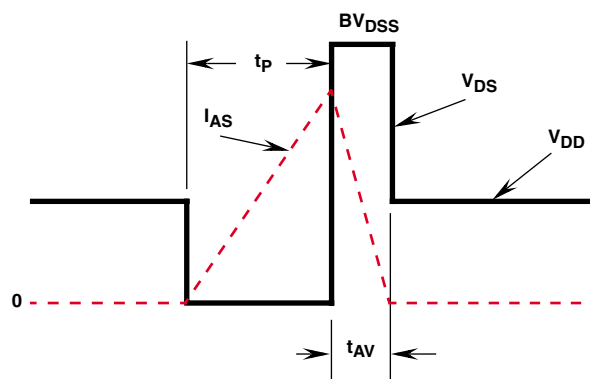


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

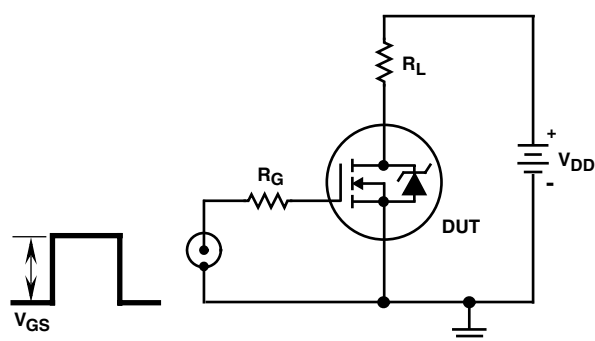


FIGURE 17. SWITCHING TIME TEST CIRCUIT

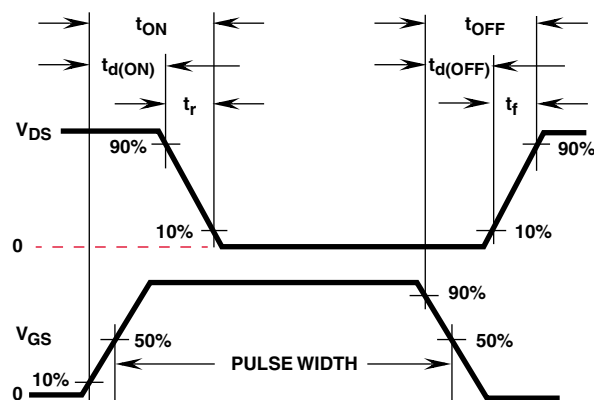


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

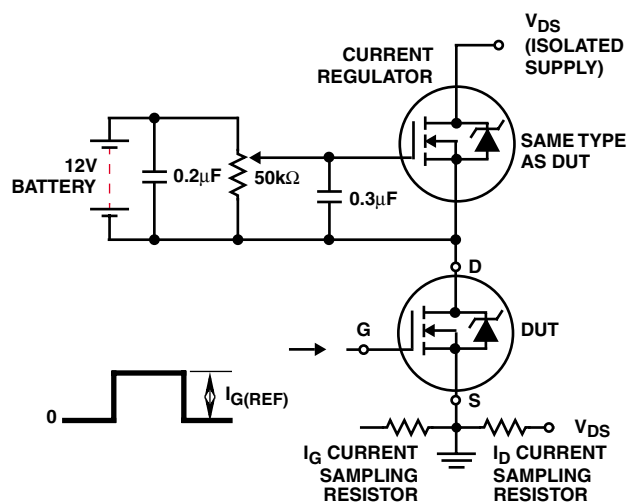


FIGURE 19. GATE CHARGE TEST CIRCUIT

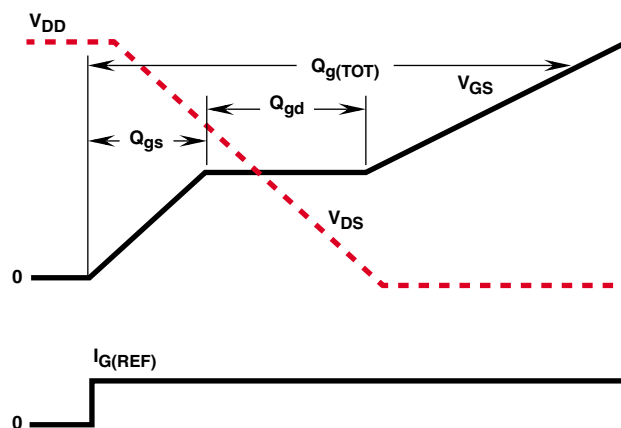


FIGURE 20. GATE CHARGE WAVEFORMS

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DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
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FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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