

25A, 100V, 0.150 Ohm, P-Channel Power MOSFET

This advanced power MOSFET is designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. It is a P-Channel enhancement mode silicon-gate power field effect transistor designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

The P-Channel IRFP9150 is an approximate electrical complement to the N-channel IRFP150.

Formerly developmental type TA49230.

Ordering Information

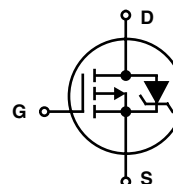
PART NUMBER	PACKAGE	BRAND
IRFP9150	TO-247	IRFP9150

NOTE: When ordering, use the entire part number.

Features

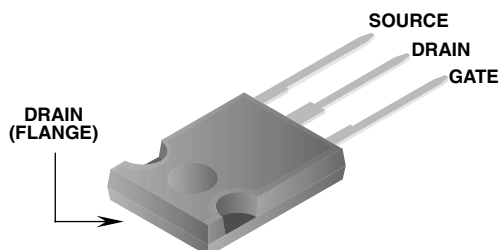
- 25A, 100V
- $r_{DS(ON)} = 0.150\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Symbol



Packaging

JEDEC STYLE TO-247



IRFP9150

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

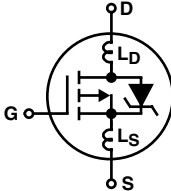
	IRFP9150	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	-100 V
Drain to Gate Voltage ($R_{GS} = 10\text{k}\Omega$) (Note 1)	V_{DGR}	-100 V
Continuous Drain Current	I_D	-25 A
$T_C = 100^\circ\text{C}$	I_D	-18 A
Pulsed Drain Current	I_{DM}	-100 A
Gate to Source Voltage	V_{GS}	± 20 V
Maximum Power Dissipation	P_D	150 W
Linear Derating Factor		1.2 W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 3)	E_{as}	1300 mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = -250μA (Figure 10)		1	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = -250μA		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Rated BV _{DSS} , V _{GS} = 0V		-	-	25	μA
		V _{DS} = 0.8 x Rated BV _{DSS} , V _{GS} = 0V, T _C = 125°C		-	-	250	μA
On-State Drain Current (Note 2)	I _{D(ON)}	V _{DS} > I _{D(ON)} × r _{DS(ON)MAX} , V _{GS} = 10V		-25	-	-	A
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	r _{DS(ON)}	V _{GS} = -10V, I _D = -10A (Figure 8, 9)		-	0.090	0.150	Ω
Forward Transconductance (Note 2)	g _{fs}	V _{DS} ≤ -10V, I _D = -12.5A (Figure 12)		4	10	-	S
Turn-On Delay Time	t _{d(ON)}	V _{DD} = -50V, I _D ≈ -25A, R _G = 6.8Ω, R _L = 2Ω (Figures 17 and 18) MOSFET switching times are essentially independent of operating temperature).		-	16	24	ns
Rise Time	t _r			-	110	160	ns
Turn-Off Delay Time	t _{d(OFF)}			-	65	100	ns
Fall Time	t _f			-	46	70	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q _{g(TOT)}	V _{GS} = -10V, I _D = -25A, V _{DS} = 0.8 x Rated BV _{DSS} I _{g(REF)} = -1.5mA (Figures 14, 19, 20) (Gate Charge is Essentially Independent Of Operating Temperature)		-	82	120	nC
Gate to Source Charge	Q _{gs}			-	14	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	42	-	nC
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = -25V, f = 1.0MHz (Figure 11)		-	2400	-	pF
Output Capacitance	C _{OSS}			-	850	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	400	-	pF
Internal Drain Inductance	L _D	Measured From the Drain Lead, 6mm (0.25in) From the Package to the Center of the Die	Modified MOSFET Symbol Showing the Internal Device Inductances 	-	5.0	-	nH
Internal Source Inductance	L _S	Measured From the Source Pin, 6mm (0.25in) From Header to the Source Bonding Pad		-	13	-	nH
Thermal Resistance Junction to Case	R _{θJC}			-	-	0.83	°C/W
Thermal Resistance Junction to Ambient	R _{θJA}	Free Air Operation		-	-	30	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode	-	-	-25	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	-100	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = -25\text{A}$, $V_{GS} = 0\text{V}$ (Figure 13)	-	-0.9	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = -25\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	150	300	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = -25\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	0.3	0.7	1.5	μC

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive Rating: Pulse width limited by Maximum junction temperature. See Transient Thermal Impedance curve (Figure 3)
- $V_{DD} = 25\text{V}$, start $T_J = 25^{\circ}\text{C}$, $L = 3.2\text{mH}$, $R_G = 25\Omega$, peak $I_{AS} = 25\text{A}$ (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

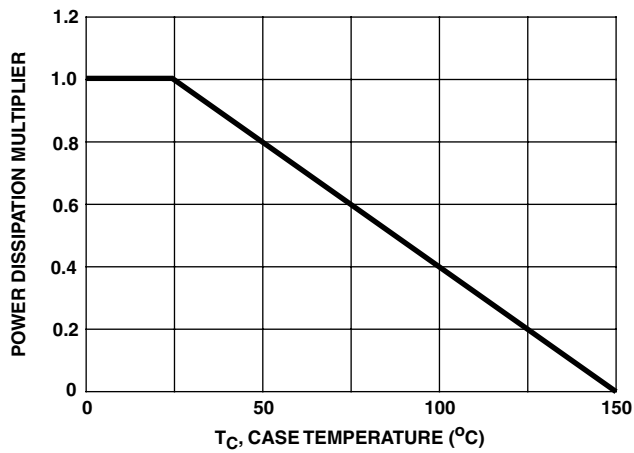


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

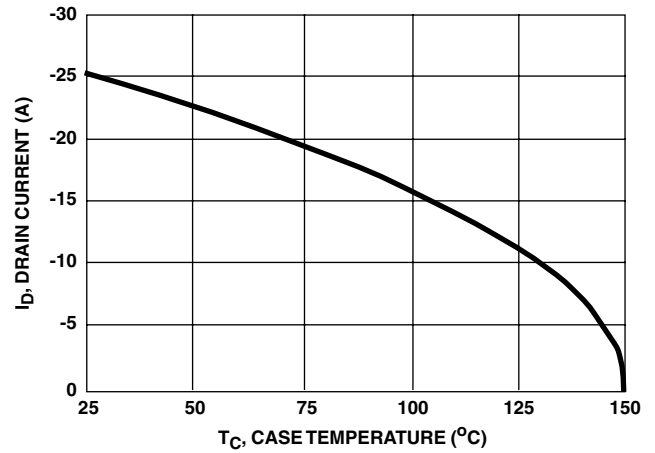


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

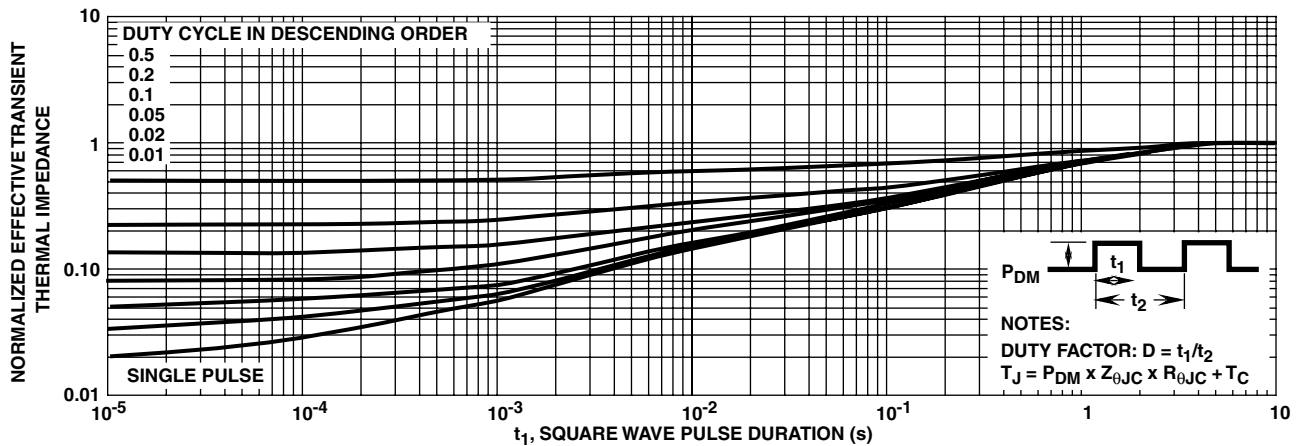


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

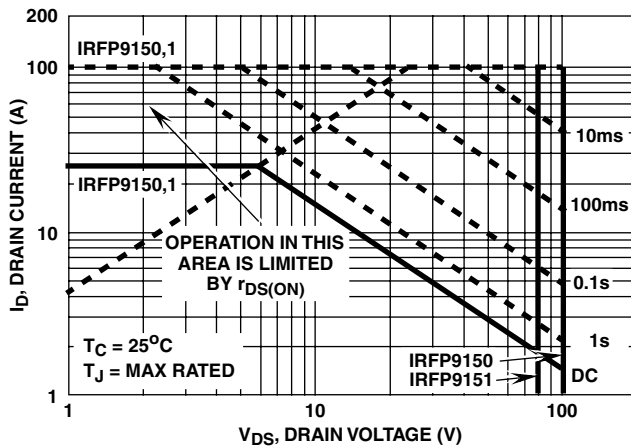


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

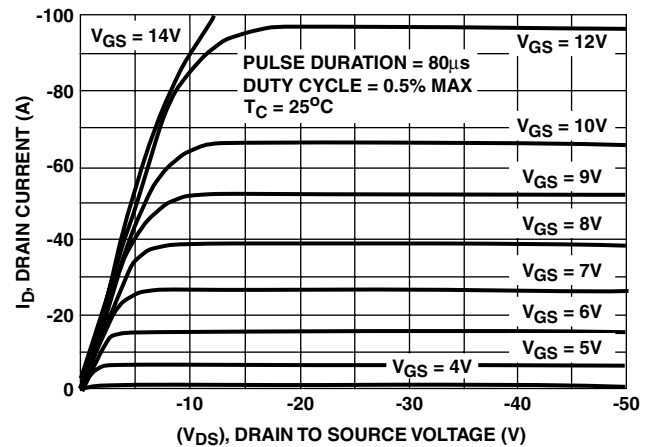


FIGURE 5. OUTPUT CHARACTERISTICS

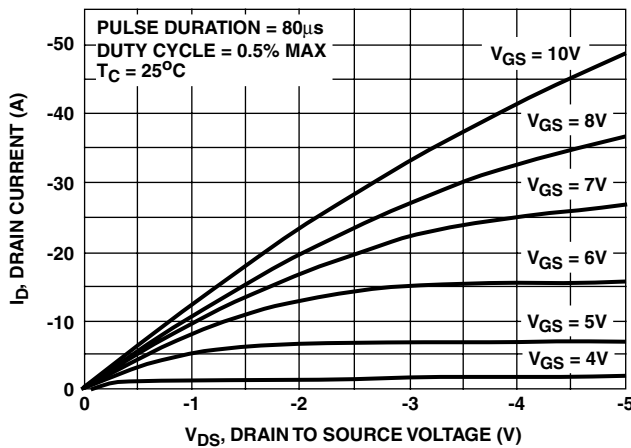


FIGURE 6. SATURATION CHARACTERISTICS

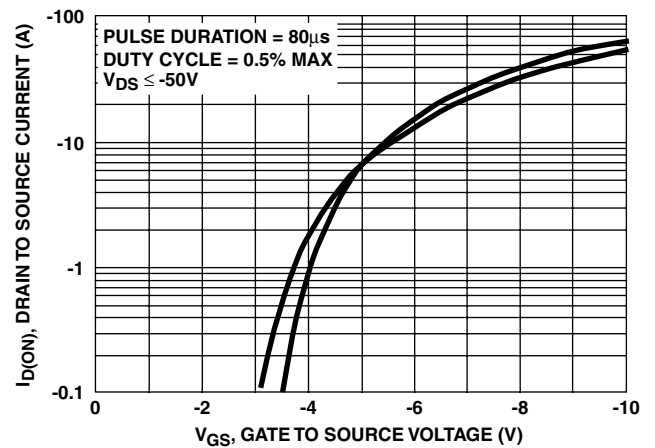


FIGURE 7. TRANSFER CHARACTERISTICS

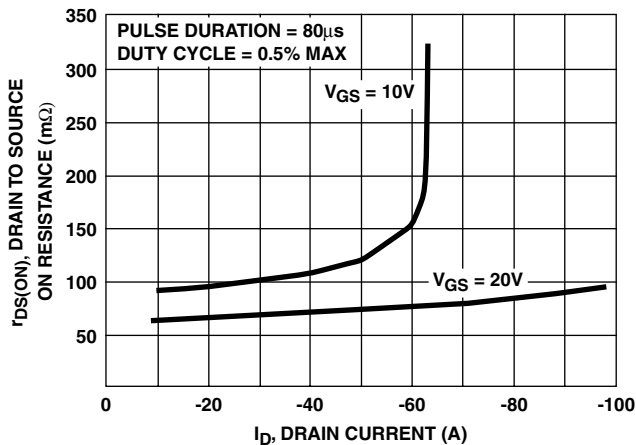


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

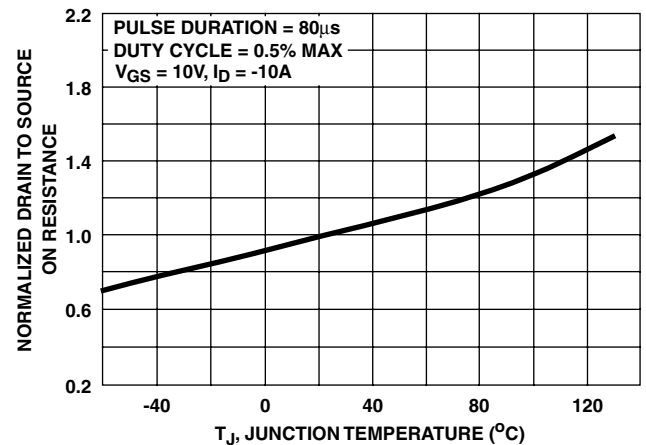


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

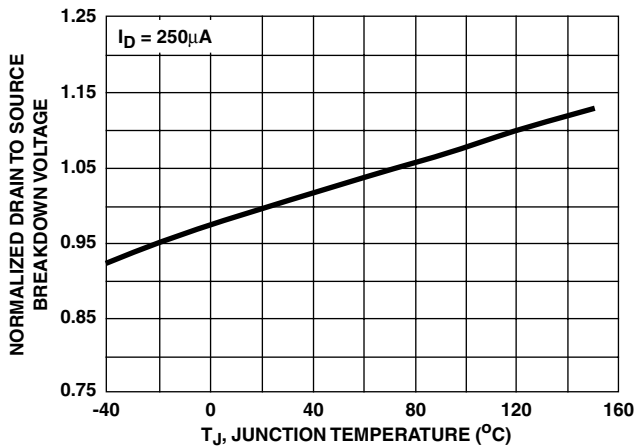


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

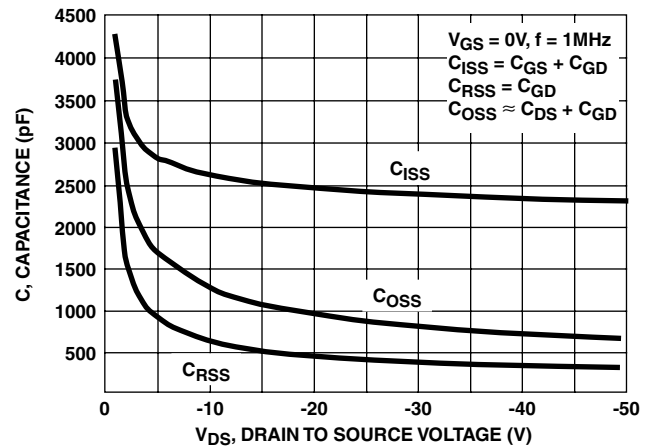


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

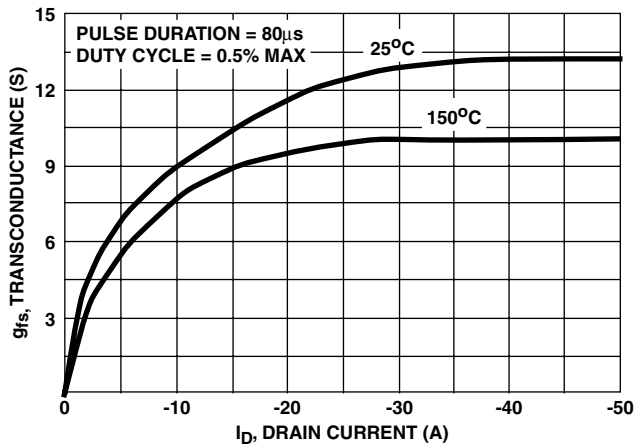


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

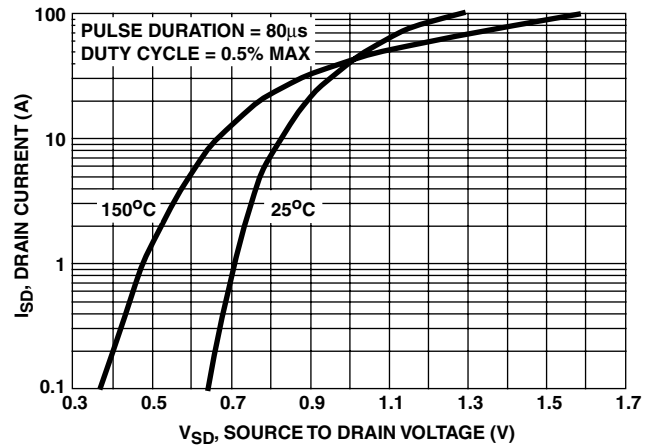


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

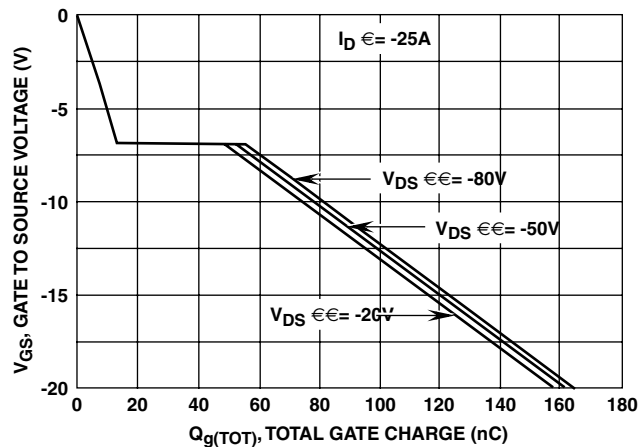


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

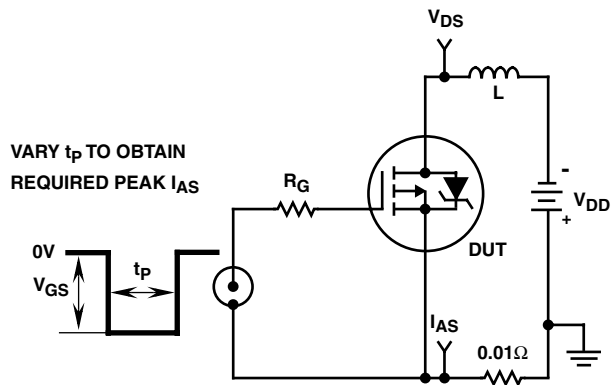


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

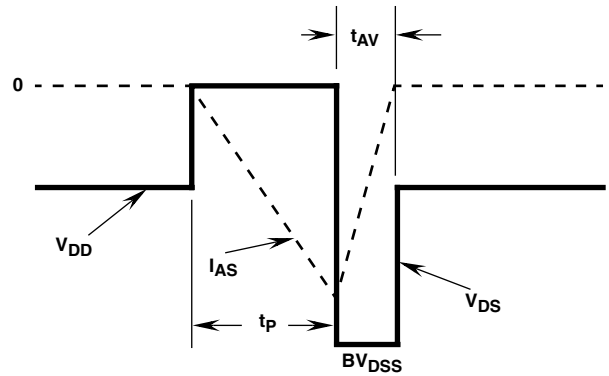


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

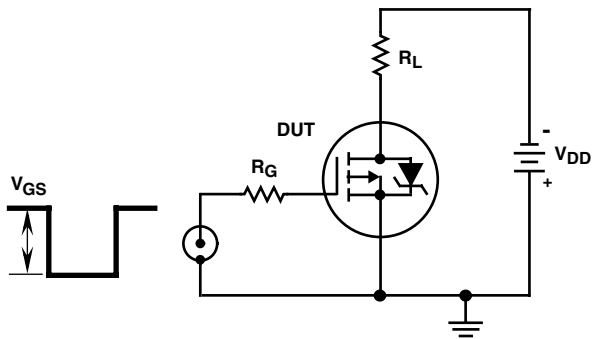


FIGURE 17. SWITCHING TIME TEST CIRCUIT

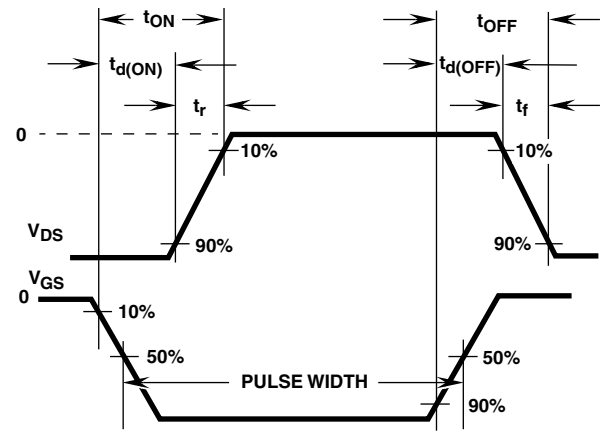


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

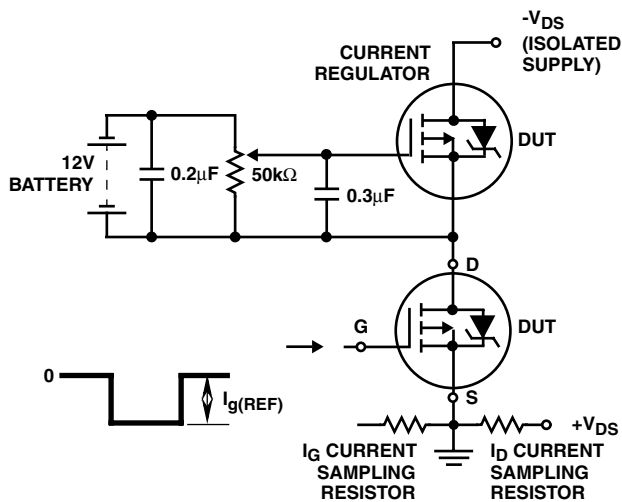


FIGURE 19. GATE CHARGE TEST CIRCUIT

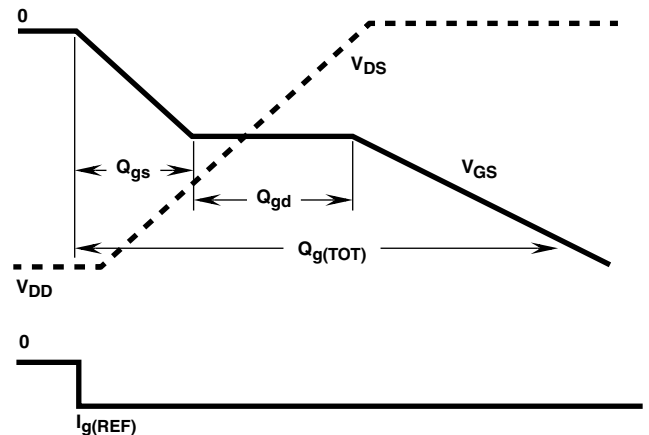


FIGURE 20. GATE CHARGE WAVEFORMS

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DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
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E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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