June 2002

PWM Optimized

ISL9N308AD3 / ISL9N308AD3ST

N-Channel Logic Level UltraFET® Trench Power MOSFETs
30V, 50A, 8mΩ

General Description

This device employs a new advanced trench MOSFET technology and features low gate charge while maintaining low on-resistance.

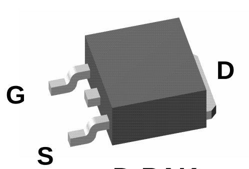
Optimized for switching applications, this device improves the overall efficiency of DC/DC converters and allows operation to higher switching frequencies.

Applications

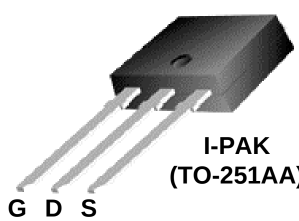
- DC/DC converters

Features

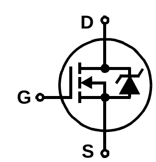
- Fast switching
- $r_{DS(ON)}$ = 0.0064Ω (Typ), V_{GS} = 10V
- $r_{DS(ON)}$ = 0.010Ω (Typ), V_{GS} = 4.5V
- Q_g (Typ) = 24nC, V_{GS} = 5V
- Q_{gd} (Typ) = 8nC
- C_{ISS} (Typ) = 2600pF



D-PAK
(TO-252)



I-PAK
(TO-251AA)



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_C = 25°C, V_{GS} = 10V) Note 1	50	A
	Continuous (T_C = 100°C, V_{GS} = 4.5V) Note 1	48	A
	Continuous (T_C = 25°C, V_{GS} = 10V, $R_{\theta JC}$ = 52°C/W)	14	A
	Pulsed	Figure 4	A
P_D	Power dissipation Derate above 25°C	100 0.67	W W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252, TO-251	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, TO-251	100	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in² copper pad area	52	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
N308AD	ISL9N308AD3ST	TO-252AA	330mm	16mm	2500 units
N308AD	ISL9N308AD3	TO-251AA	Tube	N/A	75 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off Characteristics							
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 25V, V_{GS} = 0V		-	-	1	μA
			T_C = 150^o	-	-	250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA
On Characteristics							
$V_{GS(TH)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA		1	-	3	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 50A, V_{GS} = 10V		-	0.0064	0.008	Ω
		I_D = 48A, V_{GS} = 4.5V		-	0.010	0.012	
Dynamic Characteristics							
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		-	2600	-	pF
C_{OSS}	Output Capacitance			-	520	-	pF
C_{RSS}	Reverse Transfer Capacitance			-	225	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	V_{GS} = 0V to 10V	V_{DD} = 15V, I_D = 48A, I_g = 1.0mA	-	45	68	nC
$Q_{g(5)}$	Total Gate Charge at 5V	V_{GS} = 0V to 5V		-	24	37	nC
$Q_{g(TH)}$	Threshold Gate Charge	V_{GS} = 0V to 1V		-	2.6	4.0	nC
Q_{gs}	Gate to Source Gate Charge			-	7	-	nC
Q_{gd}	Gate to Drain “Miller” Charge			-	8	-	nC
Switching Characteristics (V_{GS} = 4.5V)							
t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 14A, V_{GS} = 4.5V, R_{GS} = 6.2Ω		-	-	122	ns
$t_{d(ON)}$	Turn-On Delay Time			-	15	-	ns
t_r	Rise Time			-	67	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	35	-	ns
t_f	Fall Time			-	32	-	ns
t_{OFF}	Turn-Off Time			-	-	100	ns
Switching Characteristics (V_{GS} = 10V)							
t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 14A, V_{GS} = 10V, R_{GS} = 6.2Ω		-	-	71	ns
$t_{d(ON)}$	Turn-On Delay Time			-	8	-	ns
t_r	Rise Time			-	40	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time			-	64	-	ns
t_f	Fall Time			-	31	-	ns
t_{OFF}	Turn-Off Time			-	-	142	ns
Unclamped Inductive Switching							
t_{AV}	Avalanche Time	I_D = 3.2A, L = 3.0mH		215	-	-	μs
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 48A		-	-	1.25	V
		I_{SD} = 20A		-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 48A, dI_{SD}/dt = 100A/μs		-	-	26	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 48A, dI_{SD}/dt = 100A/μs		-	-	14	nC

Notes:
1: TO-251AA continuous current limited by package to 35A.

Typical Characteristic T_C = 25°C unless otherwise noted

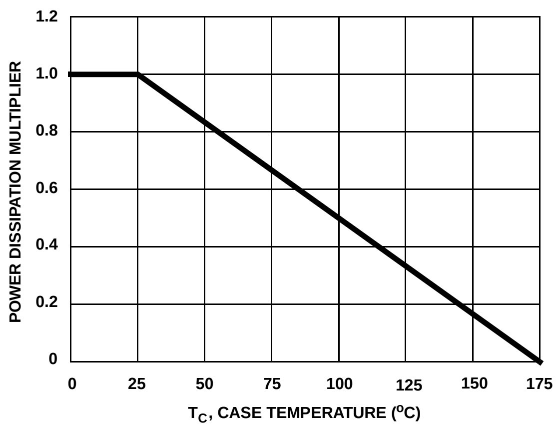


Figure 1. Normalized Power Dissipation vs Ambient Temperature

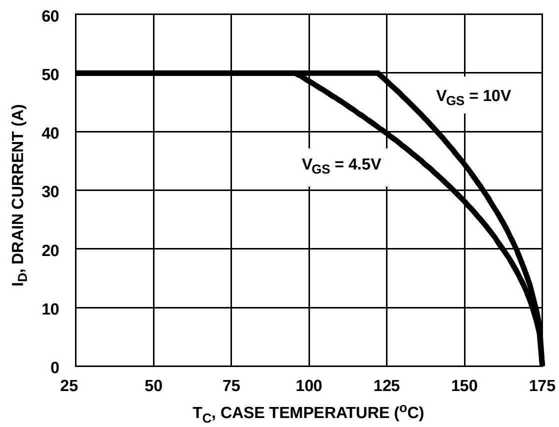


Figure 2. Maximum Continuous Drain Current vs Case Temperature

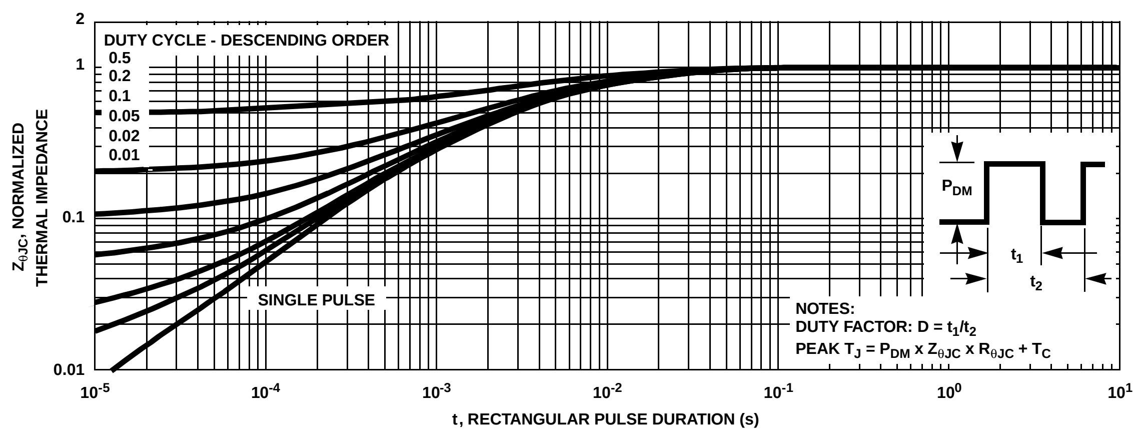


Figure 3. Normalized Maximum Transient Thermal Impedance

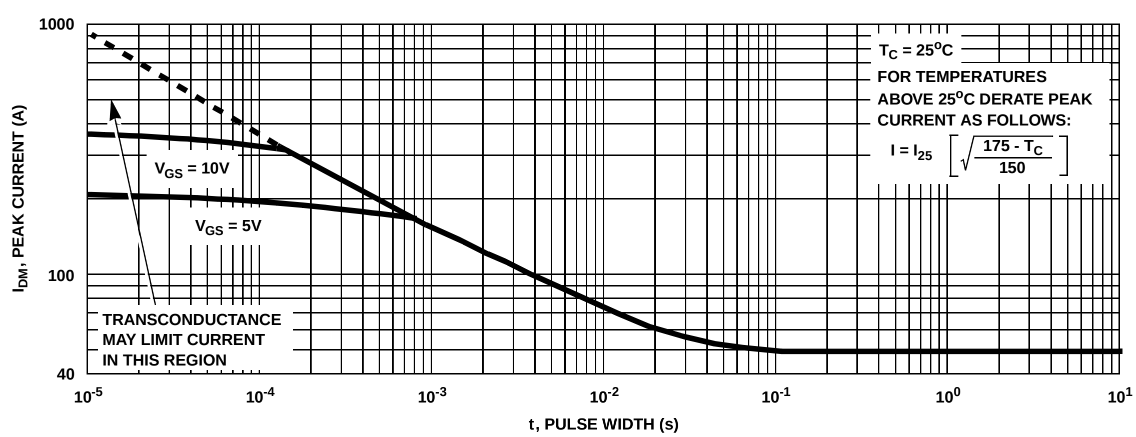


Figure 4. Peak Current Capability

Typical Characteristic (Continued) T_C = 25°C unless otherwise noted

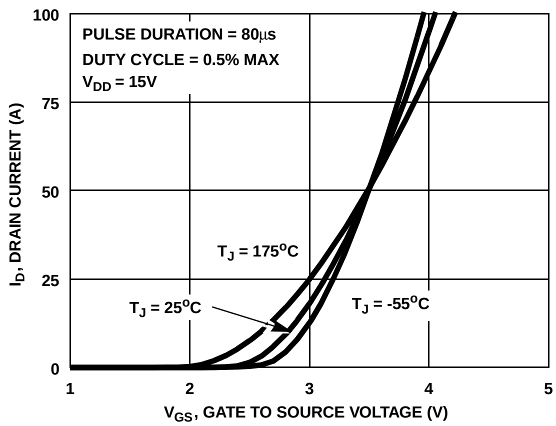


Figure 5. Transfer Characteristics

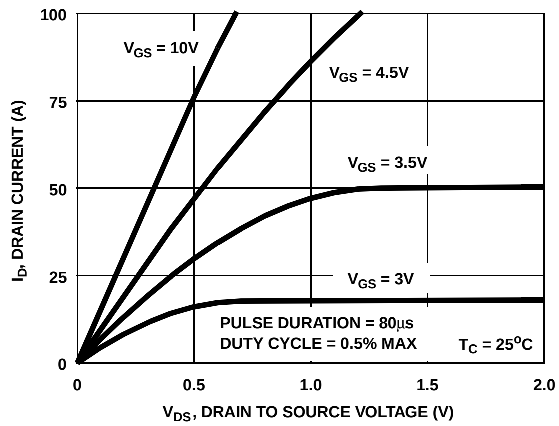


Figure 6. Saturation Characteristics

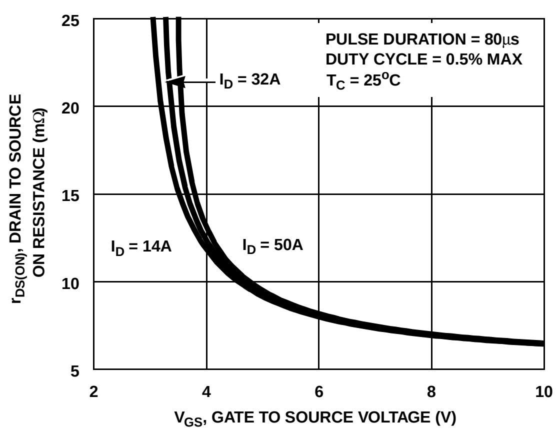


Figure 7. Drain to Source On Resistance vs Gate Voltage and Drain Current

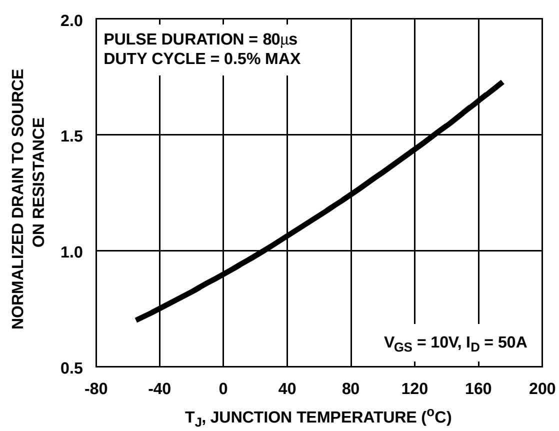


Figure 8. Normalized Drain to Source On Resistance vs Junction Temperature

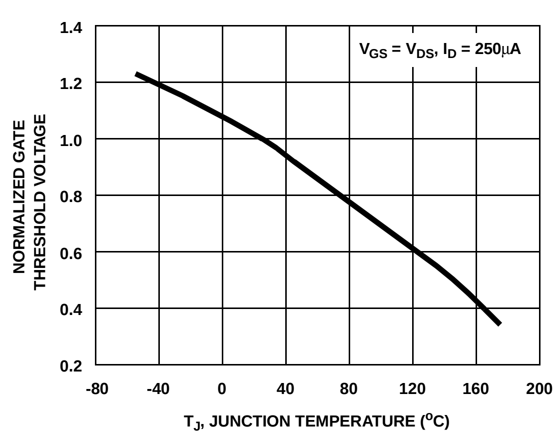


Figure 9. Normalized Gate Threshold Voltage vs Junction Temperature

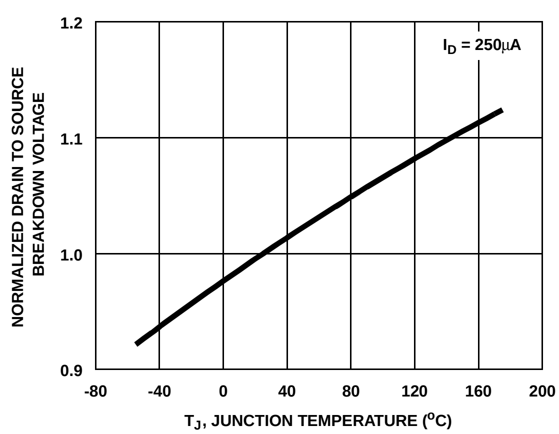


Figure 10. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

Typical Characteristic (Continued) $T_C = 25°C$ unless otherwise noted

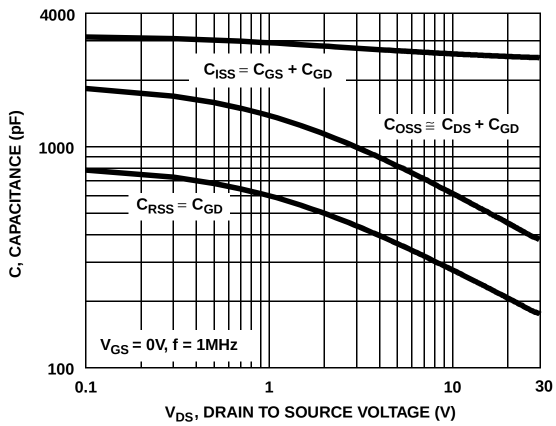


Figure 11. Capacitance vs Drain to Source Voltage

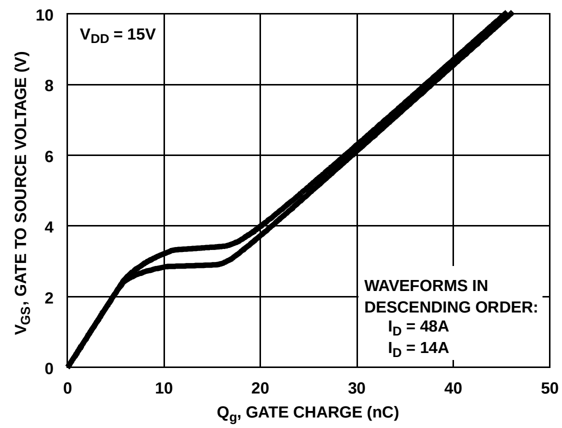


Figure 12. Gate Charge Waveforms for Constant Gate Currents

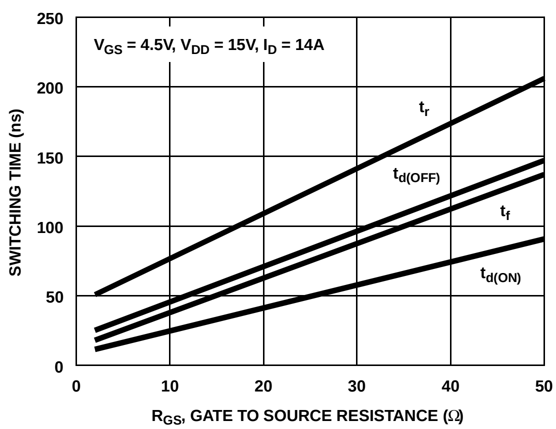


Figure 13. Switching Time vs Gate Resistance

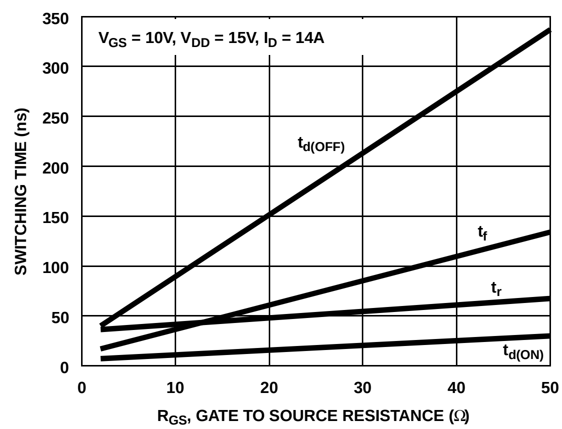


Figure 14. Switching Time vs Gate Resistance

Test Circuits and Waveforms

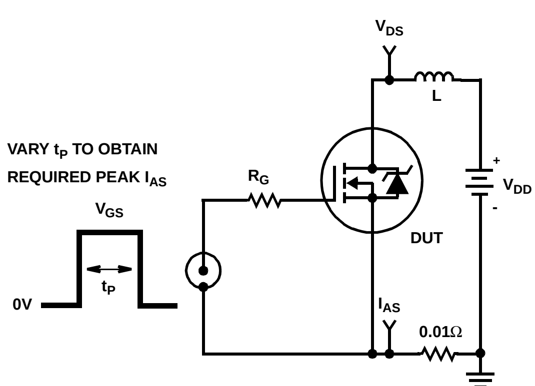


Figure 15. Unclamped Energy Test Circuit

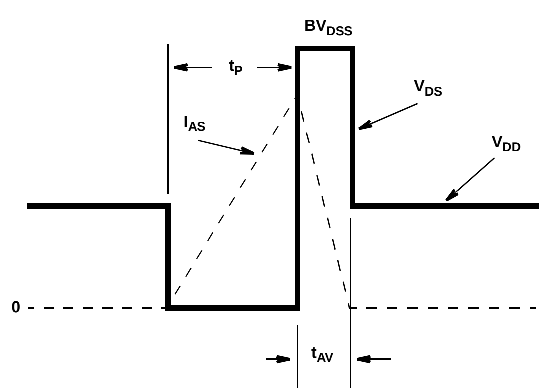


Figure 16. Unclamped Energy Waveforms

Test Circuits and Waveforms (Continued)

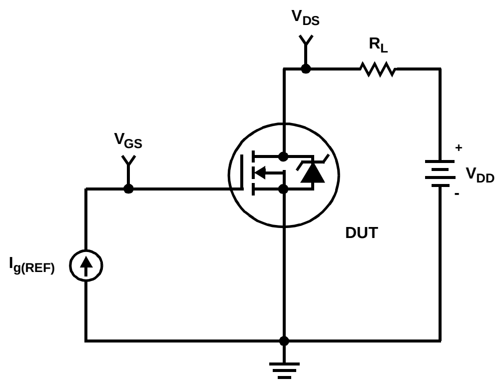


Figure 17. Gate Charge Test Circuit

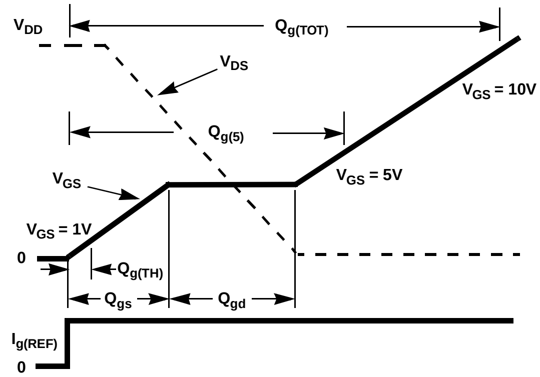


Figure 18. Gate Charge Waveforms

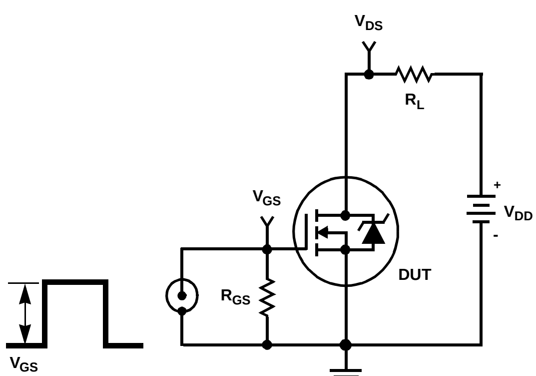


Figure 19. Switching Time Test Circuit

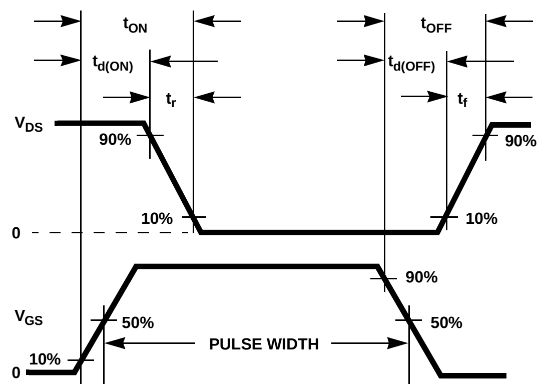


Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM}.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a coefficient added to a constant. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \qquad \text{(EQ. 2)}$$

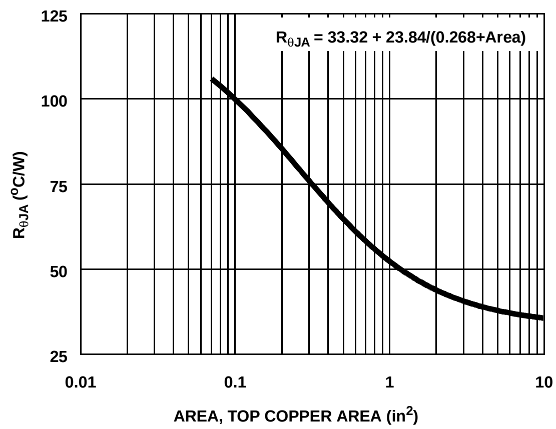
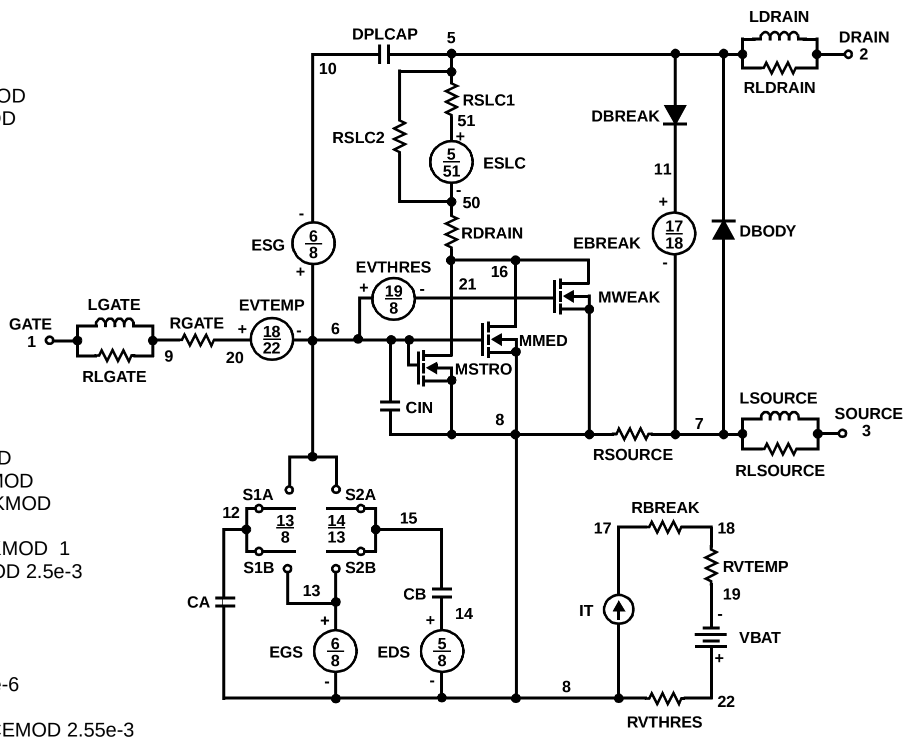


Figure 21. Thermal Resistance vs Mounting Pad Area

PSPICE Electrical Model

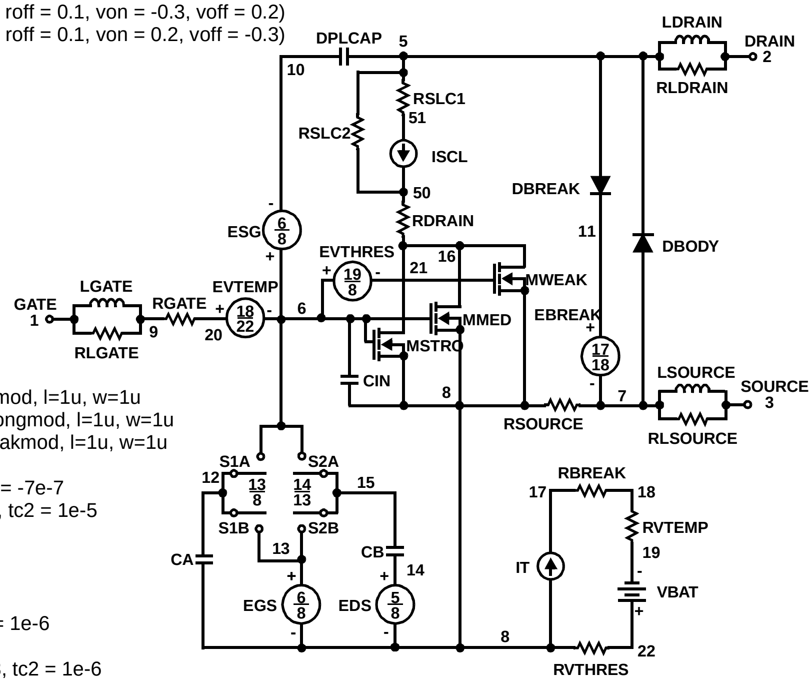
```
.SUBCKT ISL9N308AD3ST 2 1 3 ;        rev Dec2000

CA  12  8 1.5e-9
CB  15  14 1.75e-9
CIN  6  8 2.35e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 32.7
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 1e-9
LGATE 1  9 4.58e-9
LSOURCE  3  7 1.47e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 2.5e-3
RGATE  9  20 3.4
RLDRAIN 2 5 10
RLGATE 1 9 45.8
RLSOURCE 3 7 14.7
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 2.55e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*200),5))}

.MODEL DBODYMOD D (IS = 1.9e-11 N = 1.075  RS = 4.2e-3  TRS1 = 9e-4  TRS2 = 1e-6 XTI = 2.2  CJO = 1.1e-9  TT =  8e-11
M = 0.49)
.MODEL DBREAKMOD D (RS = 1.7e-1  TRS1 = 1e-3  TRS2 = -8.9e-6)
.MODEL DPLCAPMOD D (CJO = 8.2e-10  IS = 1e-30  N = 10 M = 0.45)
.MODEL MMEDMOD NMOS (VTO = 1.9 KP = 3 IS=1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.4)
.MODEL MSTROMOD NMOS (VTO = 2.35KP = 90 IS = 1e-30 N= 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.6 KP = 0.05 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 34 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1e-3  TC2 = -7e-7)
.MODEL RDRAINMOD RES (TC1 = 7e-3  TC2 = 1e-5)
.MODEL RSLCMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -2.7e-3 TC2 = -1e-5)
.MODEL RVTEMPMOD RES (TC1 = -1.8e-3  TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.0  VOFF= -0.8)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -0.8  VOFF= -4.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -0.3  VOFF= 0.2)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 0.2  VOFF= -0.3)

.ENDS
```



For further discussion of the PSPICE model, consult A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

```
REV Dec 2000
template ISL9N308AD3ST n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl = 1.9e-11, nl=1.075 , rs = 4.2e-3, trs1 = 9e-4, trs2 = 1e-6, xti=2.2, cjo = 1.1e-9, tt = 8e-11, m = 0.49,)
dp..model dbreakmod = (rs =0.17, trs1 = 1e-3, trs2 = -8.9e-6)
dp..model dplcapmod =  (cjo = 8.2e-10, isl=10e-30, nl=10, m=0.45)
m..model mmedmod = (type=_n, vto = 1.9, kp=3, is=1e-30, tox=1)
m..model mstrongmod = (type=_n, vto = 2.35, kp = 90, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.6, kp = 0.05, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -4.0, voff = -0.8)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -0.8, voff = -4.0)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -0.3, voff = 0.2)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0.2, voff = -0.3)

c.ca n12 n8 = 1.5e-9
c.cb n15 n14 = 1.75e-9
c.cin n6 n8 = 2.35e-9

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 4.58e-9
l.lsource n3 n7 = 1.47e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 1e-3, tc2 = -7e-7
res.rdrain n50 n16  = 2.5e-3, tc1 = 7e-3, tc2 = 1e-5
res.rgate n9 n20 = 3.4
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 45.8
res.rlsource n3 n7 = 14.7
res.rslc1 n5 n51= 1e-6, tc1 = 1e-3, tc2 = 1e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 2.55e-3, tc1 = 1e-3, tc2 = 1e-6
res.rvtemp n18 n19  = 1, tc1 = -1.8e-3, tc2 = 1e-6
res.rvthres n22 n8  = 1, tc1 = -2.7e-3, tc2 = -1e-5

spe.ebreak n11 n7 n17 n18 = 32.7
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e-6/200))** 5))
}
}
```



SPICE Thermal Model

REV 23 Sept 2000

ISL9N308AT

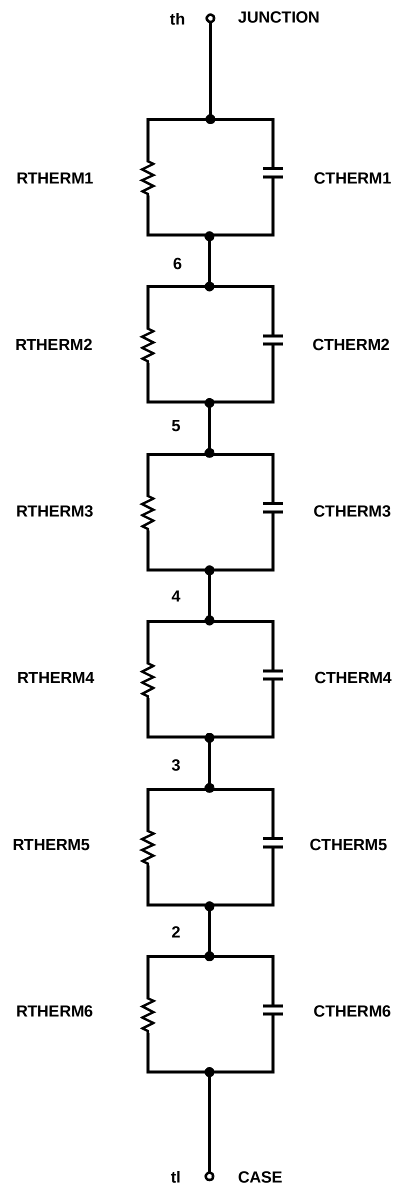
CTHERM1 th 6 2.0e-4
CTHERM2 6 5 3.0e-3
CTHERM3 5 4 3.4e-3
CTHERM4 4 3 4.0e-3
CTHERM5 3 2 1.0e-2
CTHERM6 2 tl 5.0e-2

RTHERM1 th 6 1.5e-3
RTHERM2 6 5 5.5e-3
RTHERM3 5 4 5.2e-2
RTHERM4 4 3 3.5e-1
RTHERM5 3 2 3.8e-1
RTHERM6 2 tl 4.1e-1

SABER Thermal Model

SABER thermal model ISL9N308AT
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 2.0e-4
ctherm.ctherm2 6 5 = 3.0e-3
ctherm.ctherm3 5 4 = 3.4e-3
ctherm.ctherm4 4 3 = 4.0e-3
ctherm.ctherm5 3 2 = 1.0e-2
ctherm.ctherm6 2 tl = 5.0e-2

rtherm.rtherm1 th 6 = 1.5e-3
rtherm.rtherm2 6 5 = 5.5e-3
rtherm.rtherm3 5 4 = 5.2e-2
rtherm.rtherm4 4 3 = 3.5e-1
rtherm.rtherm5 3 2 = 3.8e-1
rtherm.rtherm6 2 tl = 4.1e-1
}



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DOME™	I^2C™	QFET™	TinyLogic™
EcoSPARK™	ISOPLANAR™	QS™	TruTranslation™
E^2CMOS™	LittleFET™	QT Optoelectronics™	UHC™
EnSigna™	MicroFET™	Quiet Series™	UltraFET®
FACT™	MicroPak™	SILENT SWITCHER®	VCX™
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FAST®	OPTOLOGIC®	SPM™	
FASTr™	OPTOPLANAR™	Stealth™	

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