

# LMV321, LMV358, LMV324

## General Purpose, Low Voltage, Rail-to-Rail Output Amplifiers

### Features at +2.7V

- 80μA supply current per channel
- 1.2MHz gain bandwidth product
- Output voltage range: 0.01V to 2.69V
- Input voltage range: -0.25V to +1.5V
- 1.5V/μs slew rate
- LMV321 directly replaces other industry standard LMV321 amplifiers; available in SC70-5 and SOT23-5 packages
- LMV358 directly replaces other industry standard LMV358 amplifiers; available in MSOP-8 and SOIC-8 packages
- LMV324 directly replaces other industry standard LMV324 amplifiers; available in TSSOP-14 and SOIC-14 packages
- Fully specified at +2.7V and +5V supplies
- Operating temperature range: -40°C to +125°C

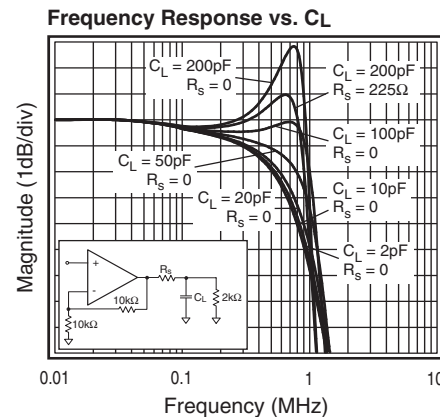
### Applications

- Low cost general purpose applications
- Cellular phones
- Personal data assistants
- A/D buffer
- DSP interface
- Smart card readers
- Portable test instruments
- Keyless entry
- Infrared receivers for remote controls
- Telephone systems
- Audio applications
- Digital still cameras
- Hard disk drives
- MP3 players

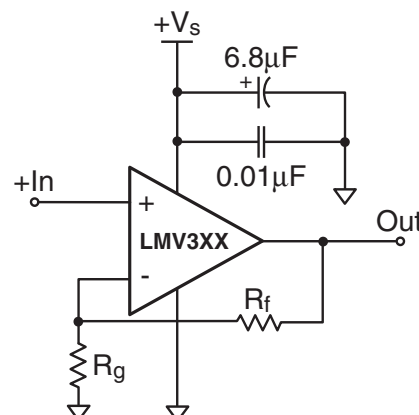
### Description

The LMV321 (single), LMV358 (dual), and LMV324 (quad) are a low cost, voltage feedback amplifiers that consume only 80μA of supply current per amplifier. The LMV3XX family is designed to operate from 2.7V (±1.35V) to 5.5V (±2.75V) supplies. The common mode voltage range extends below the negative rail and the output provides rail-to-rail performance.

The LMV3XX family is designed on a CMOS process and provides 1.2MHz of bandwidth and 1.5V/μs of slew rate at a low supply voltage of 2.7V. The combination of low power, rail-to-rail performance, low voltage operation, and tiny package options make the LMV3XX family well suited for use in personal electronics equipment such as cellular handsets, pagers, PDAs, and other battery powered applications.

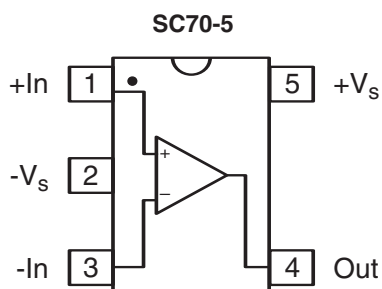
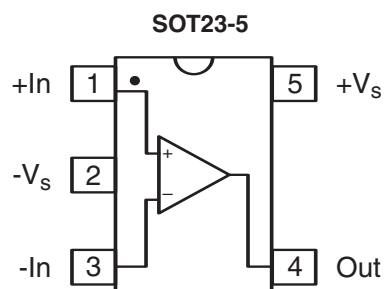


### Typical Application

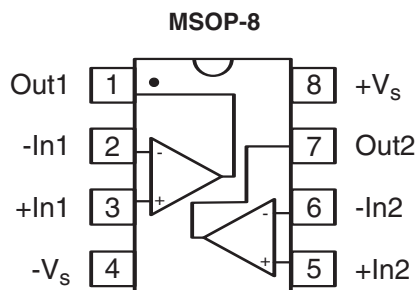
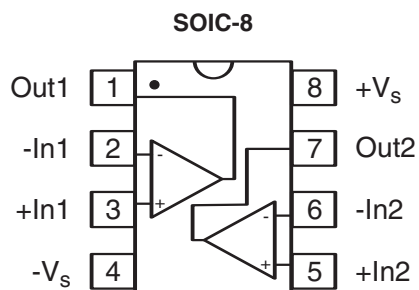


## Pin Assignments

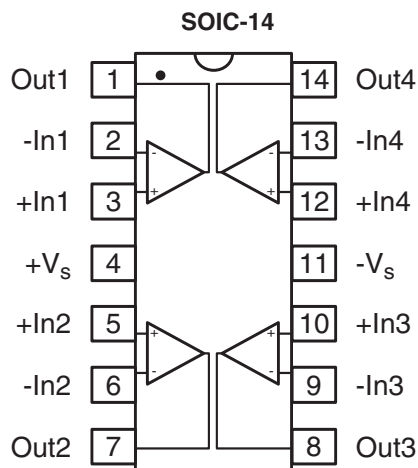
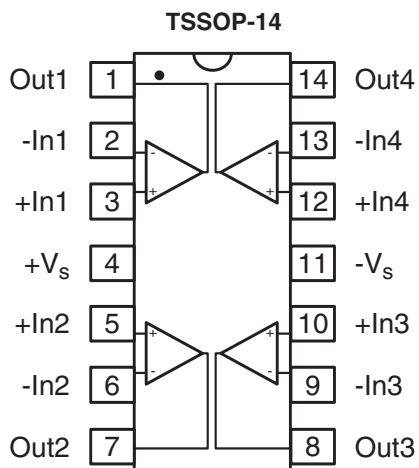
### LMV321



### LMV358



### LMV324



## Absolute Maximum Ratings

| Parameter                    | Min.                 | Max.                 | Unit |
|------------------------------|----------------------|----------------------|------|
| Supply Voltages              | 0                    | +6                   | V    |
| Maximum Junction Temperature | –                    | +175                 | °C   |
| Storage Temperature Range    | -65                  | +150                 | °C   |
| Lead Temperature, 10 seconds | –                    | +260                 | °C   |
| Input Voltage Range          | -V <sub>S</sub> -0.5 | +V <sub>S</sub> +0.5 | V    |

## Recommended Operating Conditions

| Parameter                    | Min. | Max. | Unit |
|------------------------------|------|------|------|
| Operating Temperature Range  | -40  | +125 | °C   |
| Power Supply Operating Range | 2.5  | 5.5  | V    |

## Electrical Specifications

(T<sub>C</sub> = 25°C, V<sub>S</sub> = +2.7V, G = 2, R<sub>L</sub> = 10kΩ to V<sub>S</sub>/2, R<sub>f</sub> = 10kΩ, V<sub>O</sub> (DC) = V<sub>CC</sub>/2; unless otherwise noted)

| Parameter                                    | Conditions   | Min. | Typ.  | Max. | Unit   |
|--|--|------|-------|------|--------|
| <b>AC Performance</b>                        |  |      |       |      |        |
| Gain Bandwidth Product                       | C <sub>L</sub> = 50pF, R <sub>L</sub> = 2kΩ to V <sub>S</sub> /2 |      | 1.2   |      | MHz    |
| Phase Margin                                 |  |      | 52    |      | deg    |
| Gain Margin                                  |  |      | 17    |      | dB     |
| Slew Rate                                    | V <sub>O</sub> = 1V <sub>pp</sub>                                |      | 1.5   |      | V/μs   |
| Input Voltage Noise                          | >50kHz   |      | 36    |      | nV/√Hz |
| Crosstalk: LMV358                            | 100kHz   |      | 91    |      | dB     |
| LMV324                                       | 100kHz   |      | 80    |      | dB     |
| <b>DC Performance</b>                        |  |      |       |      |        |
| Input Offset Voltage <sup>1</sup>            |  |      | 1.7   | 7    | mV     |
| Average Drift                                |  |      | 8     |      | μV/°C  |
| Input Bias Current <sup>2</sup>              |  |      | <1    |      | nA     |
| Input Offset Current <sup>2</sup>            |  |      | <1    |      | nA     |
| Power Supply Rejection Ratio <sup>1</sup>    | DC   | 50   | 65    |      | dB     |
| Supply Current (Per Channel) <sup>1</sup>    |  |      | 80    | 120  | μA     |
| <b>Input Characteristics</b>                 |  |      |       |      |        |
| Input Common Mode Voltage Range <sup>1</sup> | LO   | 0    | -0.25 |      | V      |
|  | HI   |      | 1.5   | 1.3  | V      |
| Common Mode Rejection Ratio <sup>1</sup>     |  | 50   | 70    |      | dB     |
| <b>Output Characteristics</b>                |  |      |       |      |        |
| Output Voltage Swing                         | R <sub>L</sub> = 10kΩ to V <sub>S</sub> /2; LO <sup>1</sup>      | 0.1  | 0.01  |      | V      |
|  | R <sub>L</sub> = 10kΩ to V <sub>S</sub> /2; HI <sup>1</sup>      |      | 2.69  | 2.6  | V      |

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

### Notes:

1. Guaranteed by testing or statistical analysis at +25°C.
2. +IN and -IN are gates to CMOS transistors with typical input bias current of <1nA. CMOS leakage is too small to practically measure.

## Electrical Specifications

( $T_C = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $G = 2$ ,  $R_L = 10\text{k}\Omega$  to  $V_S/2$ ,  $R_f = 10\text{k}\Omega$ ,  $V_O(\text{DC}) = V_{CC}/2$ ; unless otherwise noted)

| Parameter                                    | Conditions   | Min. | Typ.          | Max. | Unit                         |
|--|--|------|---------------|------|------------------------------|
| <b>AC Performance</b>                        |  |      |               |      |                              |
| Gain Bandwidth Product                       | $C_L = 50\text{pF}$ , $R_L = 2\text{k}\Omega$ to $V_S/2$ |      | 1.4           |      | MHz                          |
| Phase Margin                                 |  |      | 73            |      | deg                          |
| Gain Margin                                  |  |      | 12            |      | dB                           |
| Slew Rate                                    |  |      | 1.5           |      | V/ $\mu\text{s}$             |
| Input Voltage Noise                          | $>50\text{kHz}$  |      | 33            |      | nV/ $\sqrt{\text{Hz}}$       |
| Crosstalk: LMV358                            | 100kHz   |      | 91            |      | dB                           |
| LMV324                                       | 100kHz   |      | 80            |      | dB                           |
| <b>DC Performance</b>                        |  |      |               |      |                              |
| Input Offset Voltage <sup>1</sup>            |  |      | 1             | 7    | mV                           |
| Average Drift                                |  |      | 6             |      | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current <sup>2</sup>              |  |      | $<1$          |      | nA                           |
| Input Offset Current <sup>2</sup>            |  |      | $<1$          |      | nA                           |
| Power Supply Rejection Ratio <sup>1</sup>    | DC   | 50   | 65            |      | dB                           |
| Open Loop Gain <sup>1</sup>                  |  | 50   | 70            |      | dB                           |
| Supply Current (Per Channel) <sup>1</sup>    |  |      | 100           | 150  | $\mu\text{A}$                |
| <b>Input Characteristics</b>                 |  |      |               |      |                              |
| Input Common Mode Voltage Range <sup>1</sup> | LO   | 0    | -0.4          |      | V                            |
|  | HI   |      | 3.8           | 3.6  | V                            |
| Common Mode Rejection Ratio <sup>1</sup>     |  | 50   | 75            |      | dB                           |
| <b>Output Characteristics</b>                |  |      |               |      |                              |
| Output Voltage Swing                         | $R_L = 2\text{k}\Omega$ to $V_S/2$ ; LO/HI               |      | 0.036 to 4.95 |      | V                            |
|  | $R_L = 10\text{k}\Omega$ to $V_S/2$ ; LO <sup>1</sup>    | 0.1  | 0.013         |      | V                            |
|  | $R_L = 10\text{k}\Omega$ to $V_S/2$ ; HI <sup>1</sup>    |      | 4.98          | 4.9  | V                            |
| Short Circuit Output Current <sup>1</sup>    | sourcing; $V_O = 0\text{V}$                              | 5    | +34           |      | mA                           |
|  | sinking; $V_O = 5\text{V}$                               | 10   | -23           |      | mA                           |

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

### Notes:

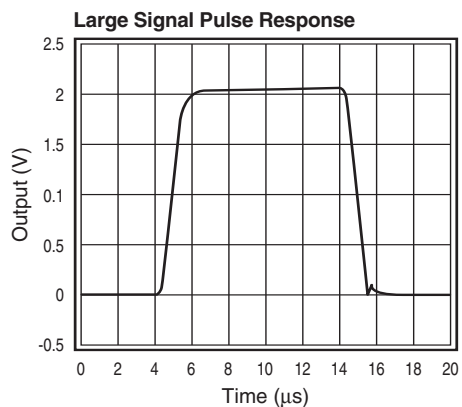
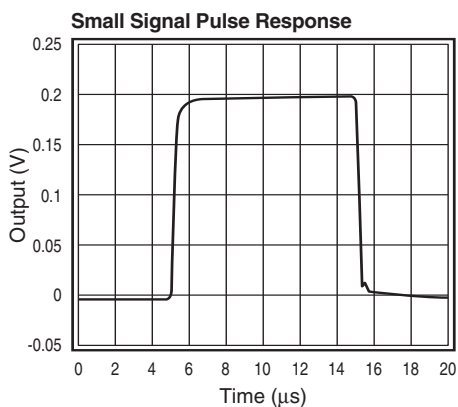
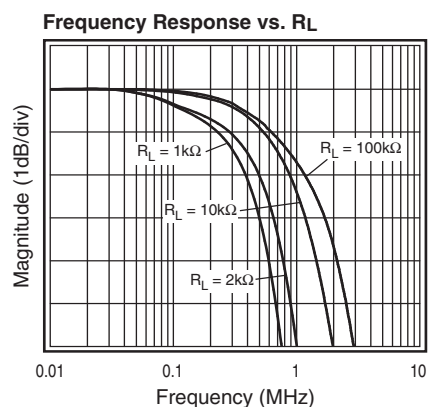
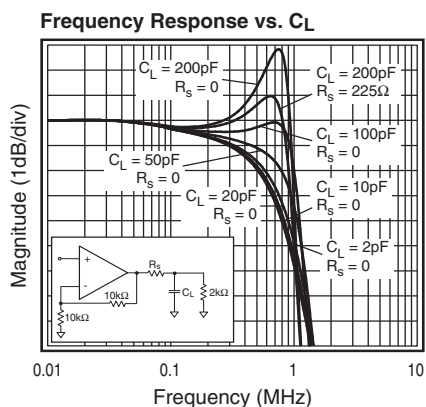
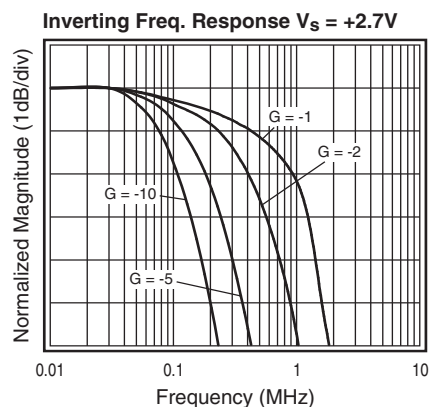
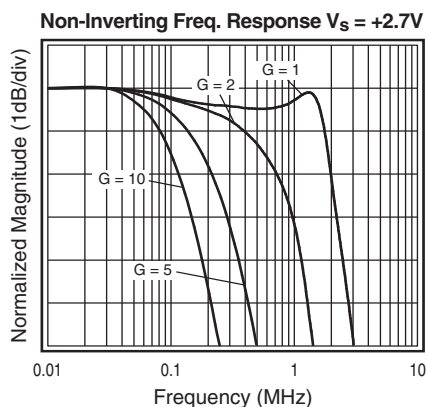
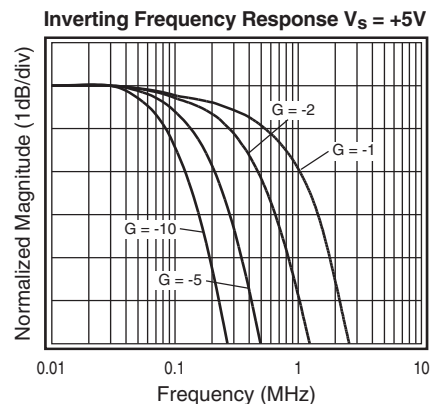
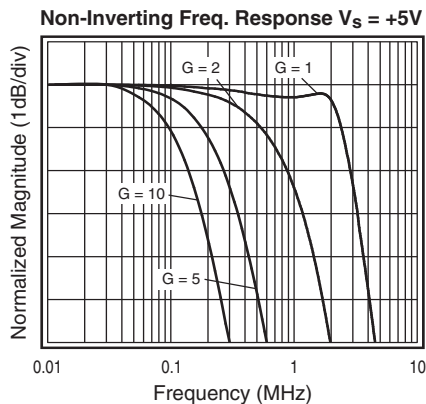
1. Guaranteed by testing or statistical analysis at  $+25^\circ\text{C}$ .
2. +IN and -IN are gates to CMOS transistors with typical input bias current of  $<1\text{nA}$ . CMOS leakage is too small to practically measure.

## Package Thermal Resistance

| Package       | $\theta_{JA}$ |
|---------------|---------------|
| 5 lead SC70   | 331.4°C/W     |
| 5 lead SOT23  | 256°C/W       |
| 8 lead SOIC   | 152°C/W       |
| 8 lead MSOP   | 206°C/W       |
| 14 lead TSSOP | 100°C/W       |
| 14 lead SOIC  | 88°C/W        |

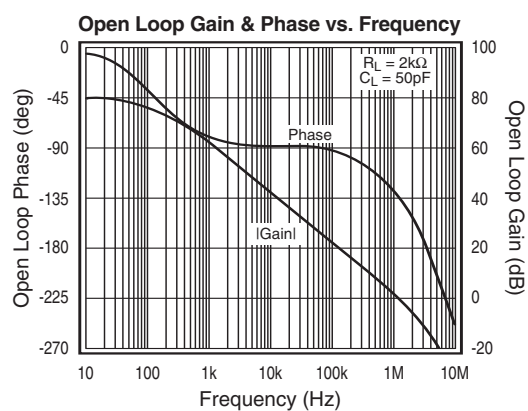
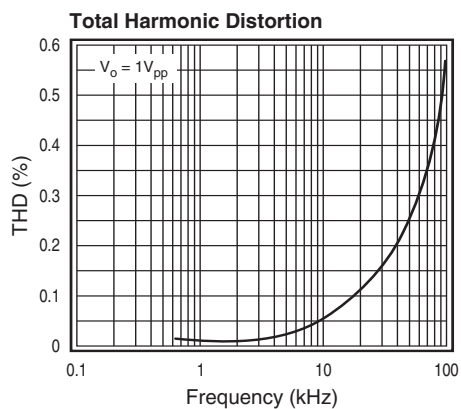
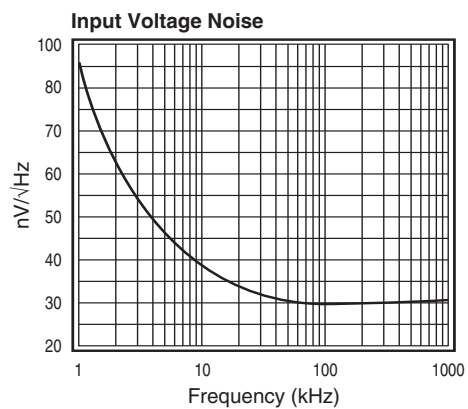
## Typical Operating Characteristics

( $T_C = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $G = 2$ ,  $R_L = 10\text{k}\Omega$  to  $V_S/2$ ,  $R_f = 10\text{k}\Omega$ ,  $V_O(\text{DC}) = V_{CC}/2$ ; unless otherwise noted)



## Typical Operating Characteristics

( $T_C = 25^\circ\text{C}$ ,  $V_S = +5\text{V}$ ,  $G = 2$ ,  $R_L = 10\text{k}\Omega$  to  $V_S/2$ ,  $R_f = 10\text{k}\Omega$ ,  $V_O(\text{DC}) = V_{CC}/2$ ; unless otherwise noted)

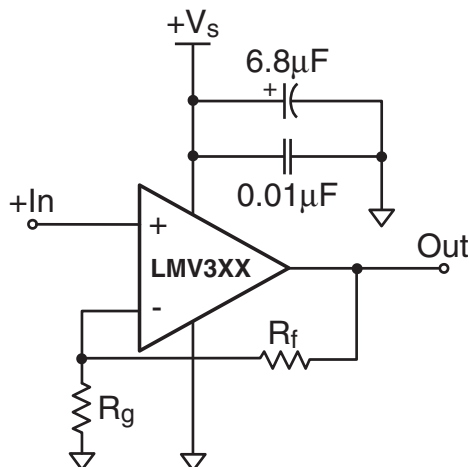


## Application Information

### General Description

The LMV3XX family are single supply, general purpose, voltage-feedback amplifiers that are pin-for-pin compatible and drop in replacements with other industry standard LMV321, LMV358, and LMV324 amplifiers. The LMV3XX family is fabricated on a CMOS process, features a rail-to-rail output, and is unity gain stable.

The typical non-inverting circuit schematic is shown in Figure



1.

**Figure 1: Typical Non-inverting configuration**

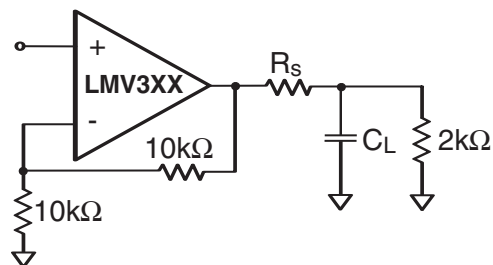
### Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, some performance degradation will occur. If the maximum junction temperature exceeds 175°C for an extended time, device failure may occur.

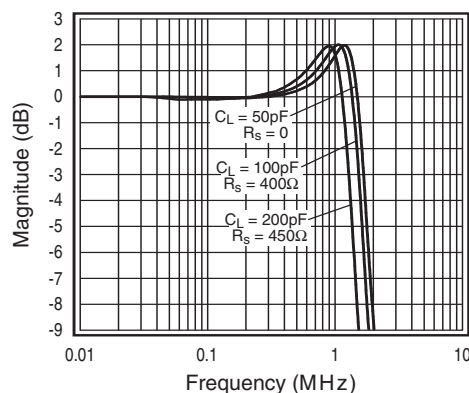
### Driving Capacitive Loads

The **Frequency Response vs  $C_L$**  plot on page 4, illustrates the response of the LMV3XX family. A small series resistance ( $R_s$ ) at the output of the amplifier, illustrated in Figure 2, will improve stability and settling performance.  $R_s$  values in the **Frequency Response vs  $C_L$**  plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger  $R_s$ . As the plot indicates, the LMV3XX family can easily drive a 200pF capacitive load without a series resistance. For comparison, the plot also shows the LMV321 driving a 200pF load with a 225Ω series resistance.

Driving a capacitive load introduces phase-lag into the output signal, which reduces phase margin in the amplifier. The unity gain follower is the most sensitive configuration. In a unity gain follower configuration, the LMV3XX family requires a 450Ω series resistor to drive a 200pF load. The response is illustrated in Figure 3.



**Figure 2: Typical Topology for driving a capacitive load**



**Figure 3: Frequency Response vs  $C_L$  for unity gain configuration**

### Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8μF and 0.01μF ceramic capacitors
- Place the 6.8μF capacitor within 0.75 inches of the power pin
- Place the 0.01μF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts shown in Figure 5 on page 8 for more information.

## Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of this device:

| Eval Bd | Description  | Products      |
|---------|--|---------------|
| KEB013  | Single Channel, Dual Supply, SOT23-5 for buffer-style pinout | LMV321AS5X    |
| KEB014  | Single Channel, Dual Supply, SC70-5 for buffer-style pinout  | LMV321AP5X    |
| KEB006  | Dual Channel, Dual Supply, 8 lead SOIC                       | LMV358AM8X    |
| KEB010  | Dual Channel, Dual Supply, 8 lead MSOP                       | LMV358AMU8X   |
| KEB012  | Quad Channel, Dual Supply, 14 lead TSSOP                     | LMV324AMTC14X |
| KEB018  | Quad Channel, Dual Supply, 14 lead SOIC                      | LMV324AM14X   |

Evaluation board schematics and layouts are shown in Figures 4 and 5.

## Evaluation Board Schematic Diagrams

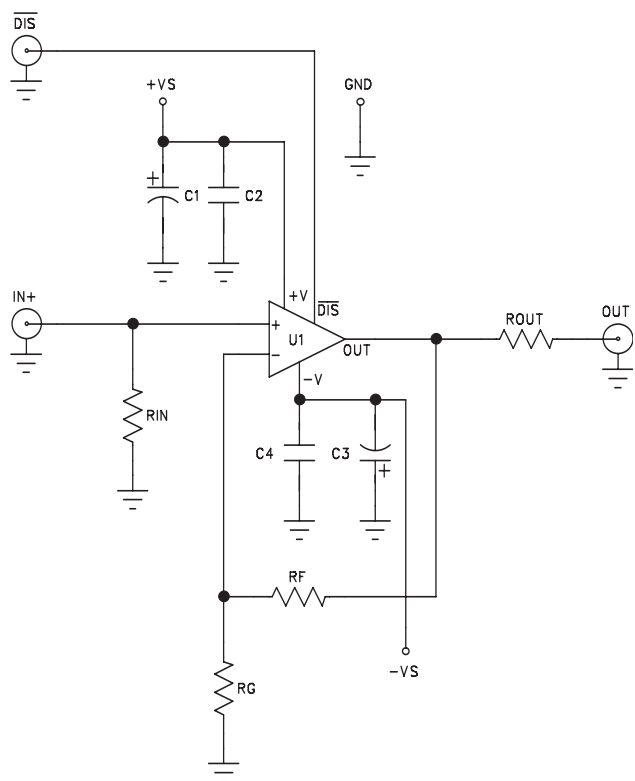


Figure 4a: LMV321 KEB013 schematic

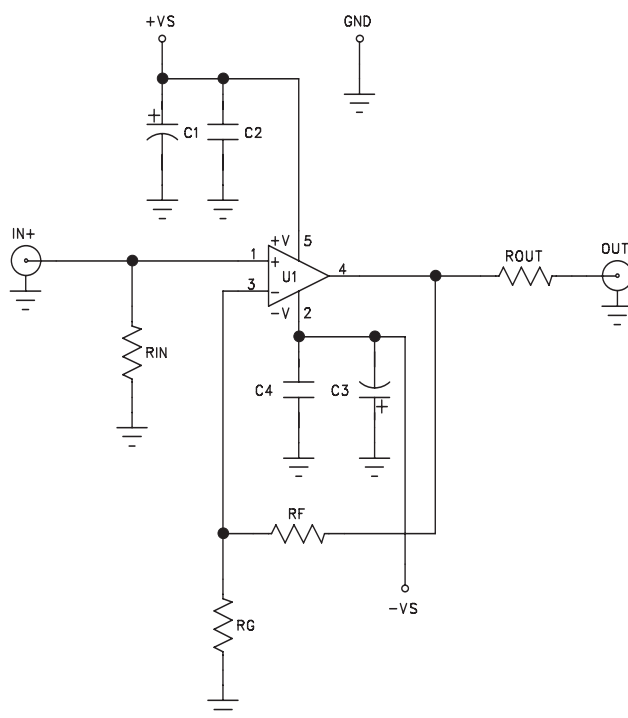


Figure 4b: LMV321 KEB014 schematic



## Evaluation Board Schematic Diagrams (Continued)

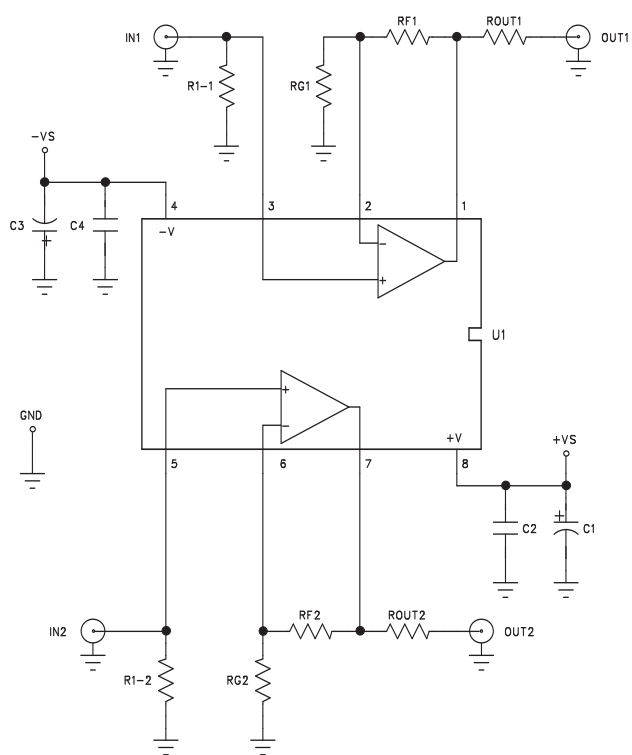


Figure 4c: LMV358 KEB006/KEB010 schematic

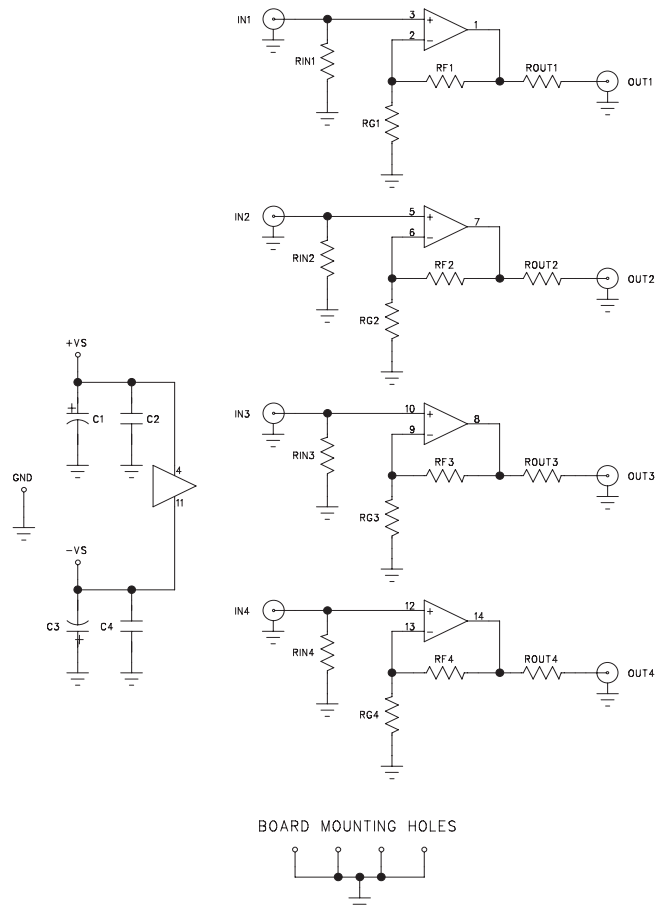


Figure 4d: LMV324 KEB012/KEB018 schematic

## LMV321 Evaluation Board Layout

FAIRCHILD SEMICONDUCTOR LAYER1 SILK

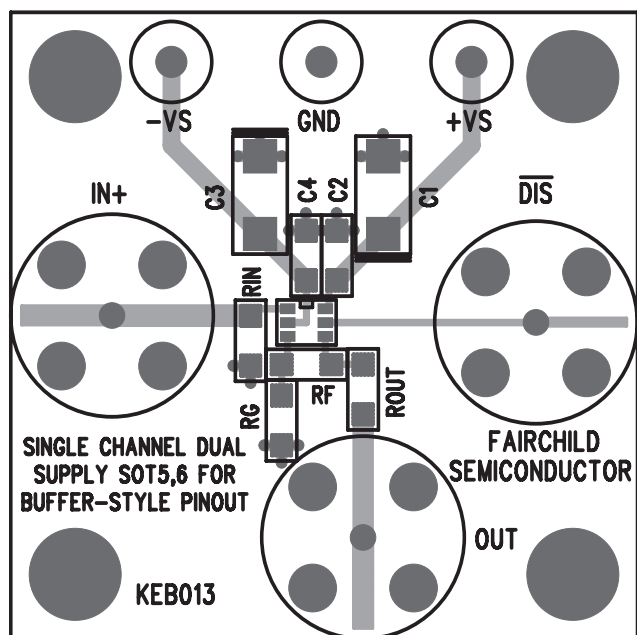


Figure 5a: KEB013 (top side)

FAIRCHILD SEMICONDUCTOR LAYER1 SILK

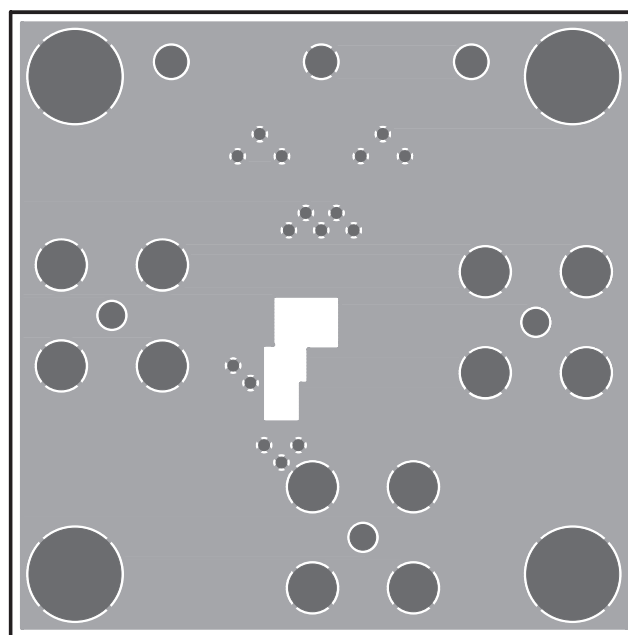


Figure 5b: KEB013 (bottom side)

FAIRCHILD SEMICONDUCTOR LAYER1 SILK

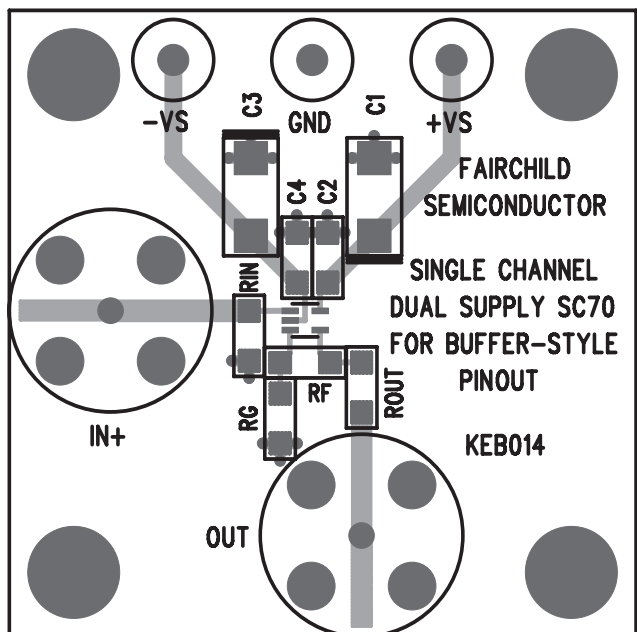


Figure 5c: KEB014 (top side)

FAIRCHILD SEMICONDUCTOR LAYER1 SILK

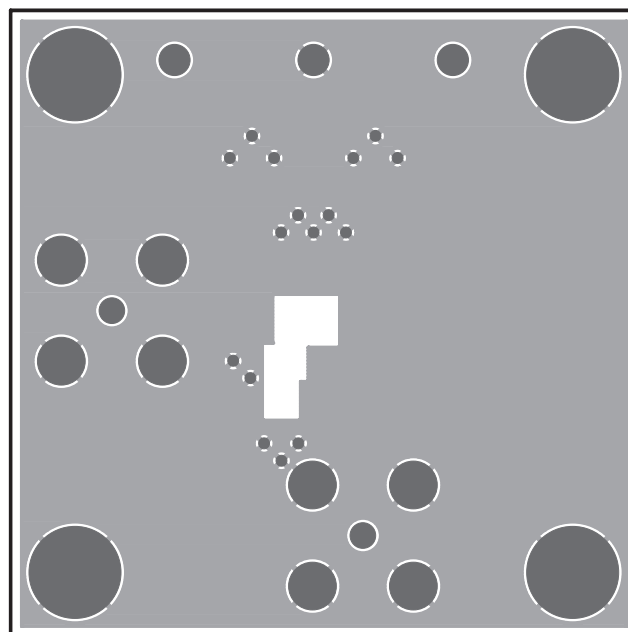


Figure 5d: KEB014 (bottom side)

## LMV358 Evaluation Board Layout

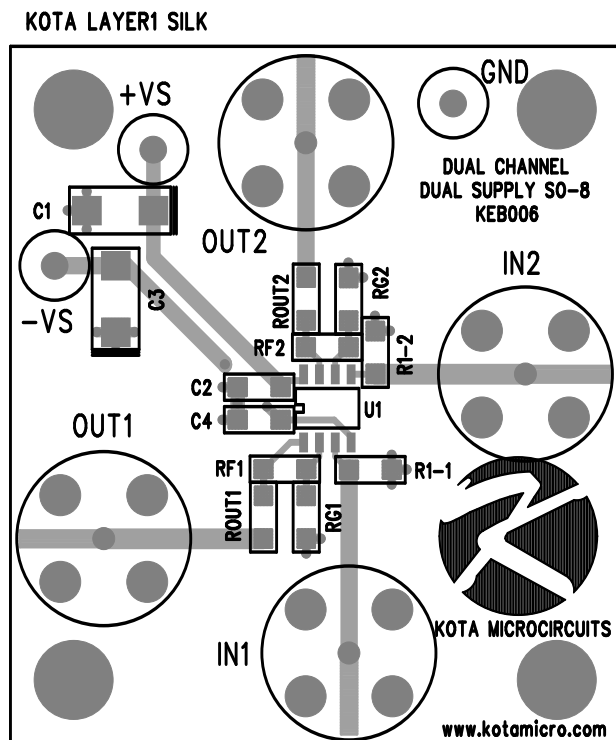


Figure 5e: KEB006 (top side)

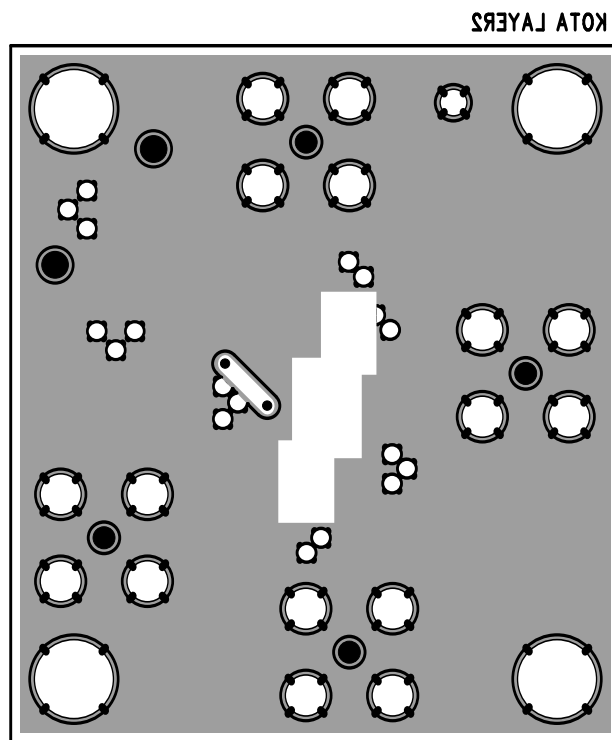


Figure 5f: KEB006 (bottom side)

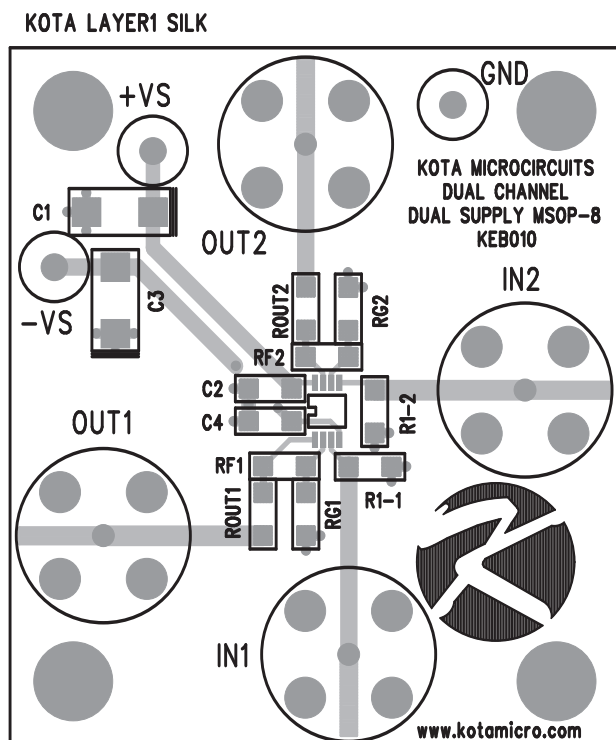


Figure 5g: KEB010 (top side)

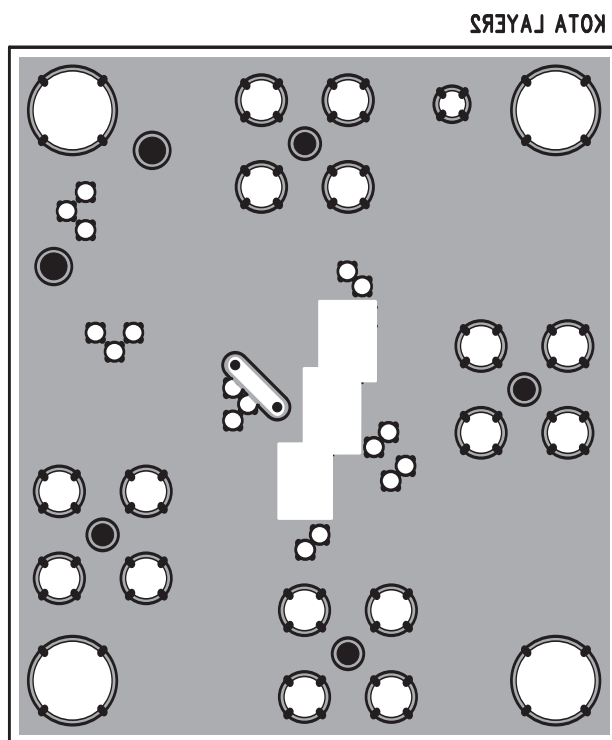


Figure 5h: KEB010 (bottom side)

## LMV324 Evaluation Board Layout

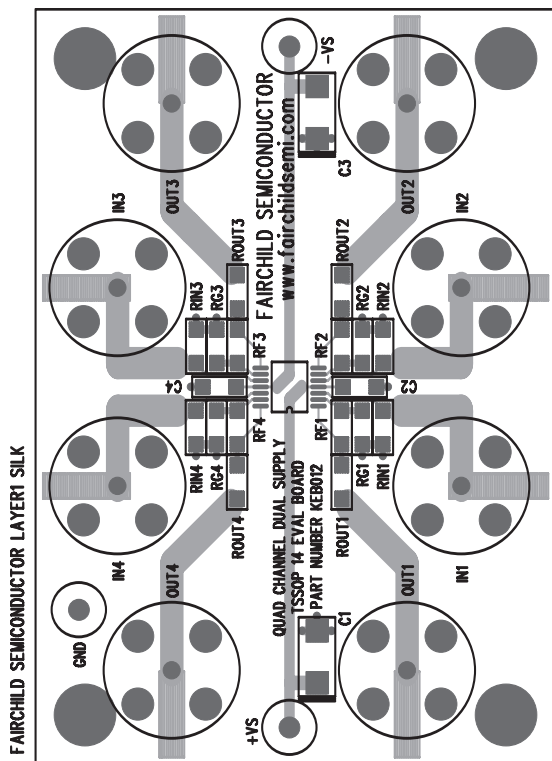


Figure 5i: KEB012 (top side)

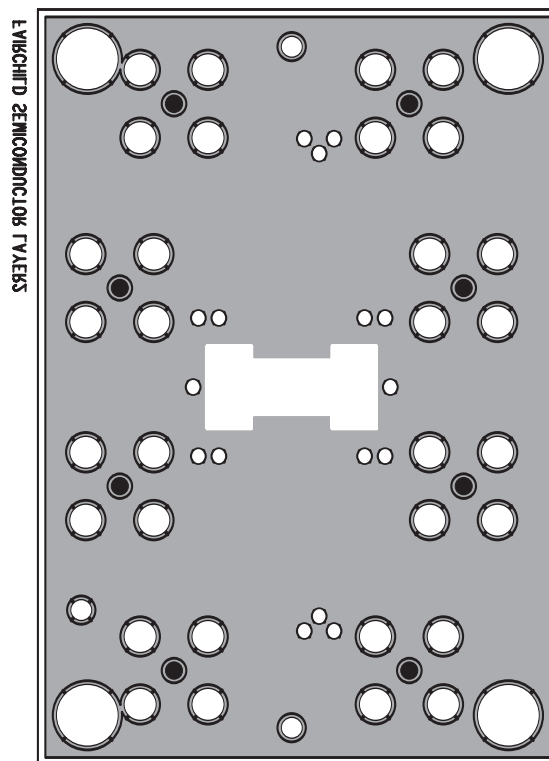


Figure 5j: KEB012 (bottom side)

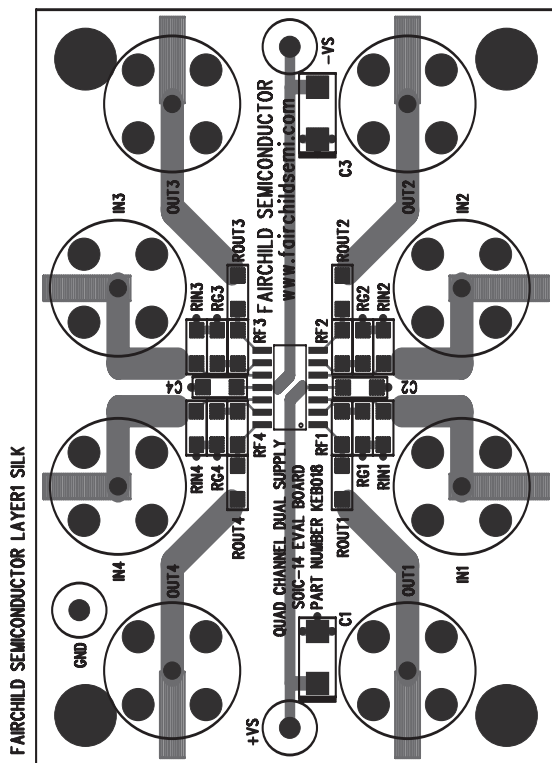


Figure 5k: KEB018 (top side)

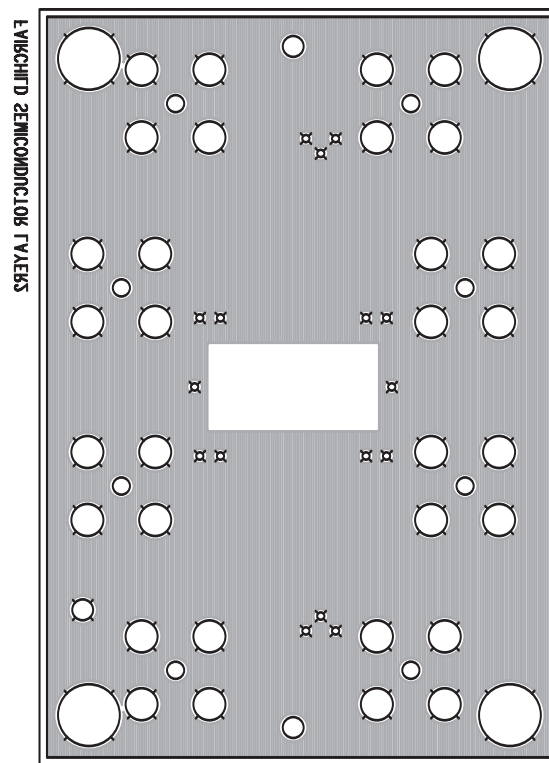
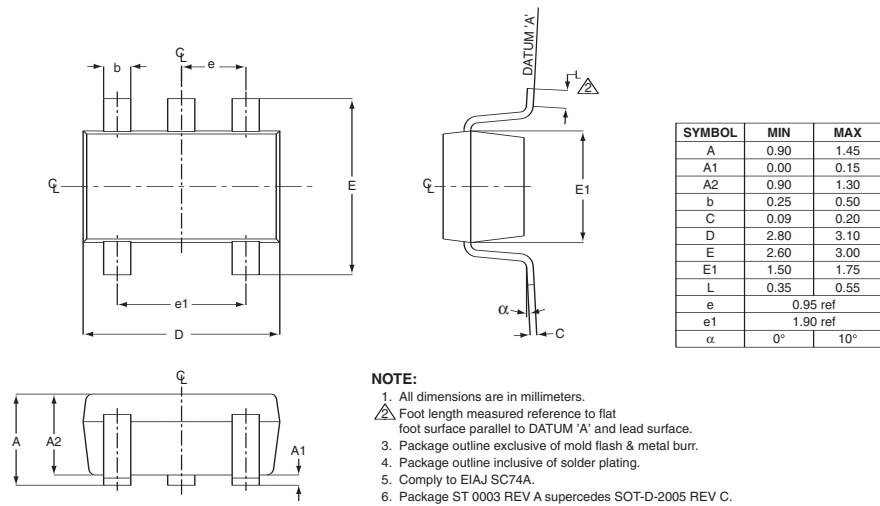


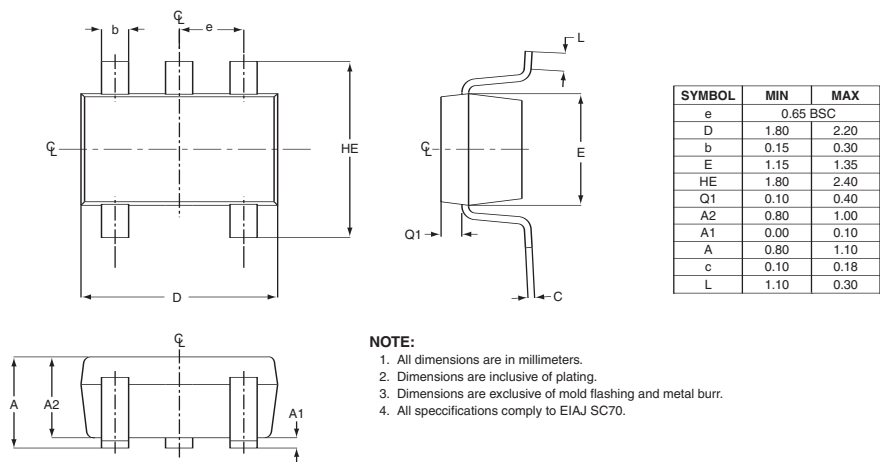
Figure 5l: KEB018 (bottom side)

# LMV321 Package Dimensions

## SOT23-5

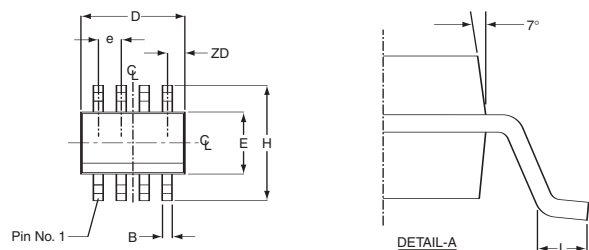


## SC70

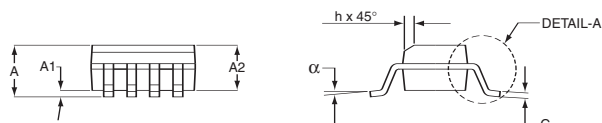


# LMV358 Package Dimensions

## SOIC



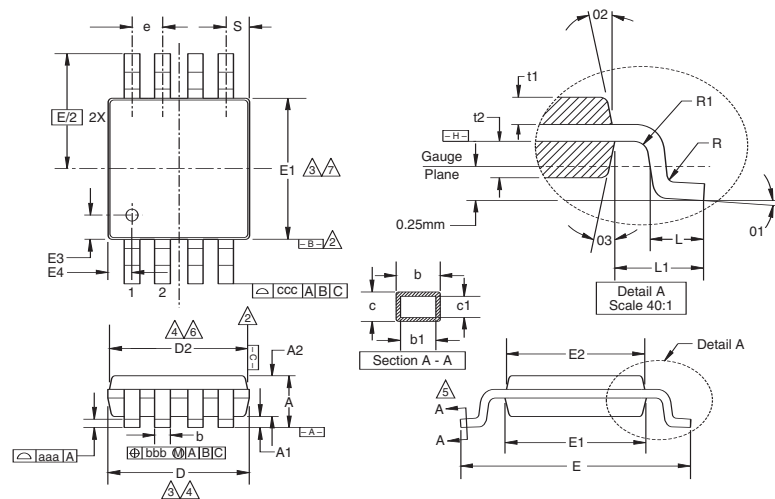
| SOIC-8 |          |      |
|--------|----------|------|
| SYMBOL | MIN      | MAX  |
| A1     | 0.10     | 0.25 |
| B      | 0.36     | 0.46 |
| C      | 0.19     | 0.25 |
| D      | 4.80     | 4.98 |
| E      | 3.81     | 3.99 |
| e      | 1.27 BSC |      |
| H      | 5.80     | 6.20 |
| h      | 0.25     | 0.50 |
| L      | 0.41     | 1.27 |
| A      | 1.52     | 1.72 |
|        | 0°       | 8°   |
| ZD     | 0.53 ref |      |
| A2     | 1.37     | 1.57 |



### NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.10mm (.004") max.
3. Package surface finishing:  
(2.1) Top: matte (charmilles #18-30).  
(2.2) All sides: matte (charmilles #18-30).  
(2.3) Bottom: smooth or matte (charmilles #18-30).
4. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.152mm (.006) per side(d).

## MSOP



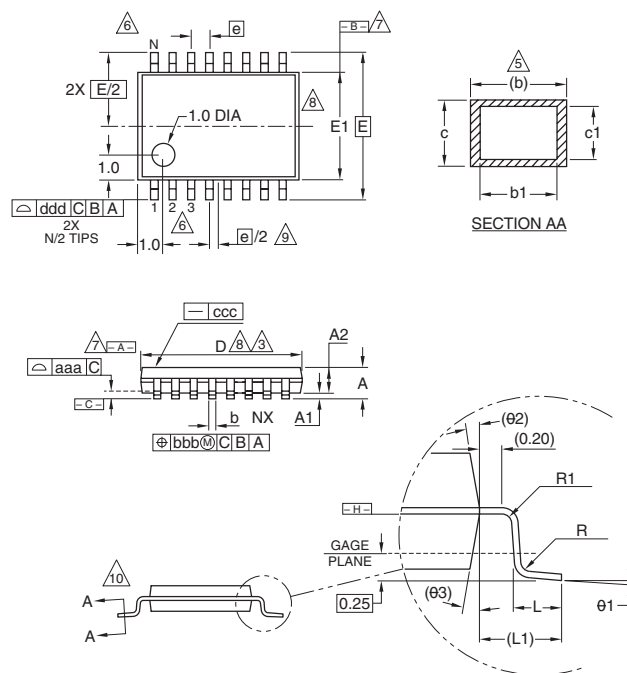
| MSOP-8 |           |             |
|--------|-----------|-------------|
| SYMBOL | MIN       | MAX         |
| A      | 1.10      | —           |
| A1     | 0.10      | ±0.05       |
| A2     | 0.86      | ±0.08       |
| D      | 3.00      | ±0.10       |
| D2     | 2.95      | ±0.10       |
| E      | 4.90      | ±0.15       |
| E1     | 3.00      | ±0.10       |
| E2     | 2.95      | ±0.10       |
| E3     | 0.51      | ±0.13       |
| E4     | 0.51      | ±0.13       |
| R      | 0.15      | +0.15/-0.06 |
| R1     | 0.15      | +0.15/-0.06 |
| t1     | 0.31      | ±0.08       |
| t2     | 0.41      | ±0.08       |
| b      | 0.33      | +0.07/-0.08 |
| b1     | 0.30      | ±0.05       |
| c      | 0.18      | ±0.05       |
| c1     | 0.15      | +0.03/-0.02 |
| 01     | 3.0°      | ±3.0°       |
| 02     | 12.0°     | ±3.0°       |
| 03     | 12.0°     | ±3.0°       |
| L      | 0.55      | ±0.15       |
| L1     | 0.95 BSC  | —           |
| aaa    | 0.10      | —           |
| bbb    | 0.08      | —           |
| ccc    | 0.25      | —           |
| e      | 0.65 BSC  | —           |
| S      | 0.525 BSC | —           |

### NOTE:

1. All dimensions are in millimeters (angle in degrees), unless otherwise specified.
- △ Datums  $\overline{B}$  and  $\overline{C}$  to be determined at datum plane  $\overline{H}$ .
- △ Dimensions "D" and "E1" are to be determined at datum  $\overline{H}$ .
- △ Dimensions "D2" and "E2" are for top package and dimensions "D" and "E1" are for bottom package.
- △ Cross sections A – A to be determined at 0.13 to 0.25mm from the leadtip.
- △ Dimension "D" and "D2" does not include mold flash, protrusion or gate burrs.
- △ Dimension "E1" and "E2" does not include interlead flash or protrusion.

# LMV324 Package Dimensions

## TSSOP

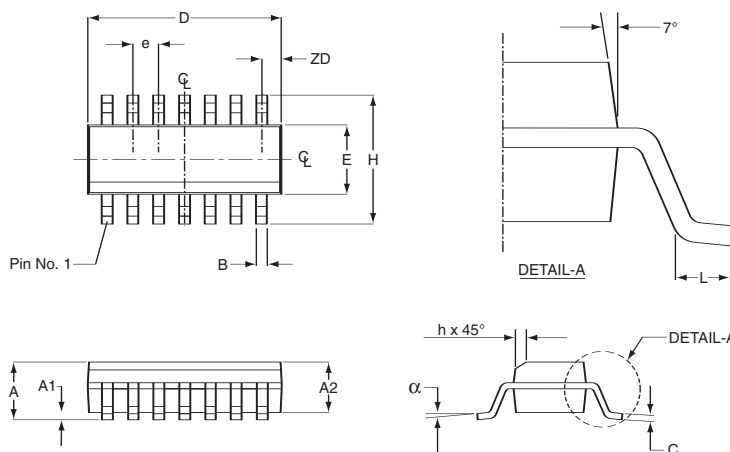


| TSSOP-14 |          |      |      |
|----------|----------|------|------|
| SYMBOL   | MIN      | NOM  | MAX  |
| A        | —        | —    | 1.10 |
| A1       | 0.05     | —    | 0.15 |
| A2       | 0.85     | 0.90 | 0.95 |
| L        | 0.50     | 0.60 | 0.75 |
| R        | 0.09     | —    | —    |
| R1       | 0.09     | —    | —    |
| b        | 0.19     | —    | 0.30 |
| b1       | 0.19     | 0.22 | 0.25 |
| c        | 0.09     | —    | 0.20 |
| c1       | 0.09     | —    | 0.16 |
| θ1       | 0°       | —    | 8°   |
| L1       | 1.0 REF  |      |      |
| aaa      | 0.10     |      |      |
| bbb      | 0.10     |      |      |
| ccc      | 0.05     |      |      |
| ddd      | 0.20     |      |      |
| e        | 0.65 BSC |      |      |
| θ2       | 12° REF  |      |      |
| θ3       | 12° REF  |      |      |
| D        | 4.90     | 5.00 | 5.10 |
| E1       | 4.30     | 4.40 | 4.50 |
| E        | 6.4 BSC  |      |      |
| e        | 0.65 BSC |      |      |
| N        | 14       |      |      |

### NOTES:

- All dimensions are in millimeters (angle in degrees).
- Dimensioning and tolerancing per ASME Y14.5–1994.
- Dimensions "D" does not include mold flash, protusions or gate burrs. Mold flash protusions or gate burrs shall not exceed 0.15 per side.
- Dimension "E1" does not include interlead flash or protusion. Interlead flash or protusion shall not exceed 0.25 per side.
- Dimension "b" does not include dambar protusion. Allowable dambar protusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protusion and adjacent lead is 0.07mm for 0.5mm pitch packages.
- Terminal numbers are shown for reference only.
- Datums  $\overline{A}$  and  $\overline{B}$  to be determined at datum plane  $\overline{H}$ .
- Dimensions "D" and "E1" to be determined at datum plane  $\overline{H}$ .
- This dimensions applies only to variations with an even number of leads per side. For variation with an odd number of leads per side, the "center" lead must be coincident with the package centerline, Datum A.
- Cross sections A – A to be determined at 0.10 to 0.25mm from the leadtip.

## SOIC



| SOIC-14 |          |       |
|---------|----------|-------|
| SYMBOL  | MIN      | MAX   |
| A1      | .0040    | .0098 |
| B       | .014     | .018  |
| C       | .0075    | .0098 |
| D       | .337     | .344  |
| E       | .150     | .157  |
| e       | .050 BSC |       |
| H       | .2284    | .2440 |
| h       | .0099    | .0196 |
| L       | .016     | .050  |
| A       | .060     | .068  |
|         | 0°       | 8°    |
| ZD      | 0.20 ref |       |
| A2      | .054     | .062  |

### NOTE:

- All dimensions are in inches.
- Lead coplanarity should be 0 to 0.10mm (.004") max.
- Package surface finishing:
  - Top: matte (charmilles #18–30).
  - All sides: matte (charmilles #18–30).
  - Bottom: smooth or matte (charmilles #18–30).
- All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.152mm (.006) per side (d).

## Ordering Information

| Model  | Part Number   | Lead Free   | Package  | Container | Pack Qty |
|--------|---------------|---|----------|-----------|----------|
| LMV321 | LMV321AP5X    |   | SC70-5   | Reel      | 3000     |
| LMV321 | LMV321AP5X_NL |  | SC70-5   | Reel      | 3000     |
| LMV321 | LMV321AS5X    |   | SOT23-5  | Reel      | 3000     |
| LMV358 | LMV358AM8X    |   | SOIC-8   | Reel      | 3000     |
| LMV358 | LMV358AMU8X   |   | MSOP-8   | Reel      | 3000     |
| LMV324 | LMV324AMTC14X |   | TSSOP-14 | Reel      | 2500     |
| LMV324 | LMV324AM14X   |   | SOIC-14  | Reel      | 2500     |

Temperature range for all parts: -40°C to +125°C.

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.