

## 18A, 200V, 0.180 Ohm, N-Channel Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17422.

## Ordering Information

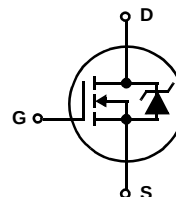
| PART NUMBER | PACKAGE  | BRAND   |
|-------------|----------|---------|
| IRF640      | TO-220AB | IRF640  |
| RF1S640     | TO-262AA | RF1S640 |
| RF1S640SM   | TO-263AB | RF1S640 |

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in the tape and reel, i.e., RF1S640SM9A.

## Features

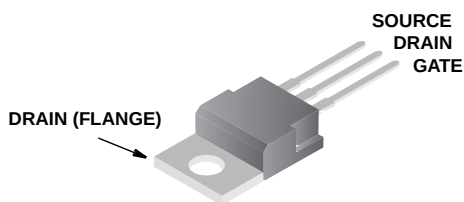
- 18A, 200V
- $r_{DS(ON)} = 0.180\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speed
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

## Symbol

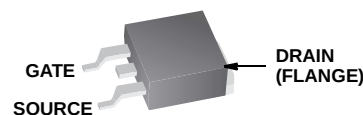


## Packaging

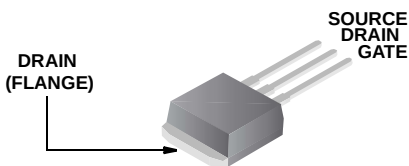
**JEDEC TO-220AB**



**JEDEC TO-263AB**



**JEDEC TO-262AA**



# IRF640, RF1S640, RF1S640SM

## Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

|                                                                          | IRF640, RF1S640, RF1S640SM | UNITS                       |
|--------------------------------------------------------------------------|----------------------------|-----------------------------|
| Drain to Source Breakdown Voltage (Note 1) . . . . .                     | $V_{DS}$ 200               | V                           |
| Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ ) (Note 1) . . . . . | $V_{DGR}$ 200              | V                           |
| Continuous Drain Current . . . . .                                       | $I_D$ 18                   | A                           |
| $T_C = 100^{\circ}\text{C}$ . . . . .                                    | $I_D$ 11                   | A                           |
| Pulsed Drain Current (Note 3) . . . . .                                  | $I_{DM}$ 72                | A                           |
| Gate to Source Voltage . . . . .                                         | $V_{GS}$ $\pm 20$          | V                           |
| Maximum Power Dissipation . . . . .                                      | $P_D$ 125                  | W                           |
| Dissipation Derating Factor . . . . .                                    | 1.0                        | $\text{W}/^{\circ}\text{C}$ |
| Single Pulse Avalanche Energy Rating (Note 4) . . . . .                  | $E_{AS}$ 580               | mJ                          |
| Operating and Storage Temperature . . . . .                              | $T_J, T_{STG}$ -55 to 150  | $^{\circ}\text{C}$          |
| Maximum Temperature for Soldering                                        |                            |                             |
| Leads at 0.063in (1.6mm) from Case for 10s. . . . .                      | $T_L$ 300                  | $^{\circ}\text{C}$          |
| Package Body for 10s, See TB334. . . . .                                 | $T_{pkg}$ 260              | $^{\circ}\text{C}$          |

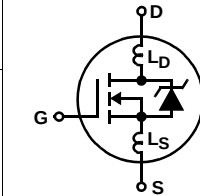
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $T_J = 25^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

## Electrical Specifications $T_C = 25^{\circ}\text{C}$ , Unless Otherwise Specified

| PARAMETER                                             | SYMBOL          | TEST CONDITIONS                                                                                                                                                                                                  | MIN | TYP  | MAX       | UNITS                       |
|-------------------------------------------------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----------|-----------------------------|
| Drain to Source Breakdown Voltage                     | $BV_{DSS}$      | $I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$ , (Figure 10)                                                                                                                                                      | 200 | -    | -         | V                           |
| Gate Threshold Voltage                                | $V_{GS(TH)}$    | $V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$                                                                                                                                                                       | 2   | -    | 4         | V                           |
| Zero Gate Voltage Drain Current                       | $I_{DSS}$       | $V_{DS} = \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$                                                                                                                                                         | -   | -    | 25        | $\mu\text{A}$               |
|                                                       |                 | $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ , $V_{GS} = 0\text{V}$ , $T_J = 125^{\circ}\text{C}$                                                                                                                | -   | -    | 250       | $\mu\text{A}$               |
| On-State Drain Current (Note 1)                       | $I_{D(ON)}$     | $V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$ , $V_{GS} = 10\text{V}$ (Figure 7)                                                                                                                                     | 18  | -    | -         | A                           |
| Gate to Source Leakage Current                        | $I_{GSS}$       | $V_{GS} = \pm 20\text{V}$                                                                                                                                                                                        | -   | -    | $\pm 100$ | nA                          |
| Drain to Source On Resistance (Note 1)                | $r_{DS(ON)}$    | $I_D = 10\text{A}$ , $V_{GS} = 10\text{V}$ (Figures 8, 9)                                                                                                                                                        | -   | 0.14 | 0.18      | $\Omega$                    |
| Forward Transconductance (Note 1)                     | $g_{fs}$        | $V_{DS} \geq 10\text{V}$ , $I_D = 11\text{A}$ (Figure 12)                                                                                                                                                        | 6.7 | 10   | -         | S                           |
| Turn-On Delay Time                                    | $t_{d(ON)}$     | $V_{DD} = 100\text{V}$ , $I_D \approx 18\text{A}$ , $R_{GS} = 9.1\Omega$ , $R_L = 5.4\Omega$ ,<br>MOSFET Switching Times are Essentially<br>Independent of Operating Temperature                                 | -   | 13   | 21        | ns                          |
| Rise Time                                             | $t_r$           |                                                                                                                                                                                                                  | -   | 50   | 77        | ns                          |
| Turn-Off Delay Time                                   | $t_{d(OFF)}$    |                                                                                                                                                                                                                  | -   | 46   | 68        | ns                          |
| Fall Time                                             | $t_f$           |                                                                                                                                                                                                                  | -   | 35   | 54        | ns                          |
| Total Gate Charge<br>(Gate to Source + Gate to Drain) | $Q_{g(TOT)}$    | $V_{GS} = 10\text{V}$ , $I_D \approx 18\text{A}$ , $V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$<br>(Figure 14) Gate Charge is Essentially Independent<br>of Operating Temperature<br>$I_{G(REF)} = 1.5\text{mA}$ | -   | 43   | 64        | nC                          |
| Gate to Source Charge                                 | $Q_{gs}$        |                                                                                                                                                                                                                  | -   | 8    | -         | nC                          |
| Gate to Drain "Miller" Charge                         | $Q_{gd}$        |                                                                                                                                                                                                                  | -   | 22   | -         | nC                          |
| Input Capacitance                                     | $C_{ISS}$       | $V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$ (Figure 11)                                                                                                                                     | -   | 1275 | -         | pF                          |
| Output Capacitance                                    | $C_{OSS}$       |                                                                                                                                                                                                                  | -   | 400  | -         | pF                          |
| Reverse Transfer Capacitance                          | $C_{RSS}$       |                                                                                                                                                                                                                  | -   | 100  | -         | pF                          |
| Internal Drain Inductance                             | $L_D$           | Measured From the<br>Contact Screw on Tab to<br>Center of Die                                                                                                                                                    | -   | 3.5  | -         | nH                          |
|                                                       |                 | Measured From the Drain<br>Lead, 6mm (0.25in) From<br>Package to Center of Die                                                                                                                                   |     |      |           |                             |
| Internal Source Inductance                            | $L_S$           | Measured From the<br>Source Lead, 6mm<br>(0.25in) from Header to<br>Source Bonding Pad                                                                                                                           |     |      |           | nH                          |
| Thermal Resistance Junction to Case                   | $R_{\theta JC}$ |                                                                                                                                                                                                                  | -   | -    | 1         | $^{\circ}\text{C}/\text{W}$ |
| Thermal Resistance Junction to<br>Ambient             | $R_{\theta JA}$ | Free Air Operation, IRF640                                                                                                                                                                                       | -   | -    | 62        | $^{\circ}\text{C}/\text{W}$ |
|                                                       | $R_{\theta JA}$ | RF1S640SM Mounted on FR-4 Board with Minimum<br>Mounting Pad                                                                                                                                                     | -   | -    | 62        | $^{\circ}\text{C}/\text{W}$ |



## Source to Drain Diode Specifications

| PARAMETER                              | SYMBOL    | TEST CONDITIONS                                                                             | MIN | TYP | MAX | UNITS         |
|----------------------------------------|-----------|---------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| Continuous Source to Drain Current     | $I_{SD}$  | Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode                      | -   | -   | 18  | A             |
| Pulse Source to Drain Current (Note 2) | $I_{SDM}$ |                                                                                             | -   | -   | 72  | A             |
| Source to Drain Diode Voltage (Note 2) | $V_{SD}$  | $T_J = 25^{\circ}\text{C}$ , $I_{SD} = 18\text{A}$ , $V_{GS} = 0\text{V}$ , (Figure 13)     | -   | -   | 2.0 | V             |
| Reverse Recovery Time                  | $t_{rr}$  | $T_J = 25^{\circ}\text{C}$ , $I_{SD} = 18\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | 120 | 240 | 530 | ns            |
| Reverse Recovery Charge                | $Q_{RR}$  | $T_J = 25^{\circ}\text{C}$ , $I_{SD} = 18\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | 1.3 | 2.8 | 5.6 | $\mu\text{C}$ |

### NOTES:

- Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
- $V_{DD} = 50\text{V}$ , starting  $T_J = 25^{\circ}\text{C}$ ,  $L = 3.37\text{mH}$ ,  $R_G = 25\Omega$ , peak  $I_{AS} = 18\text{A}$ .

## Typical Performance Curves Unless Otherwise Specified

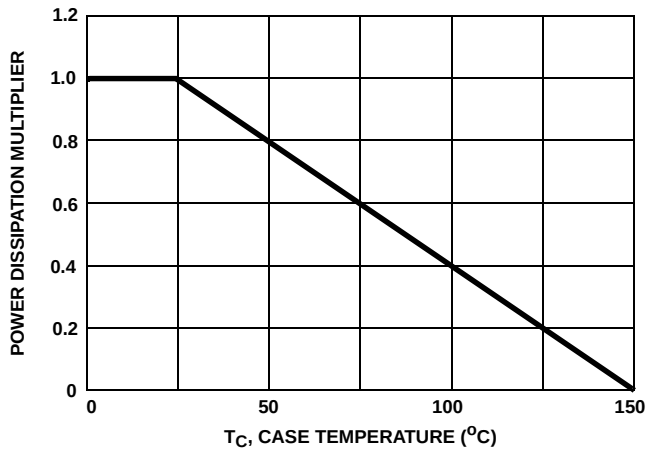


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

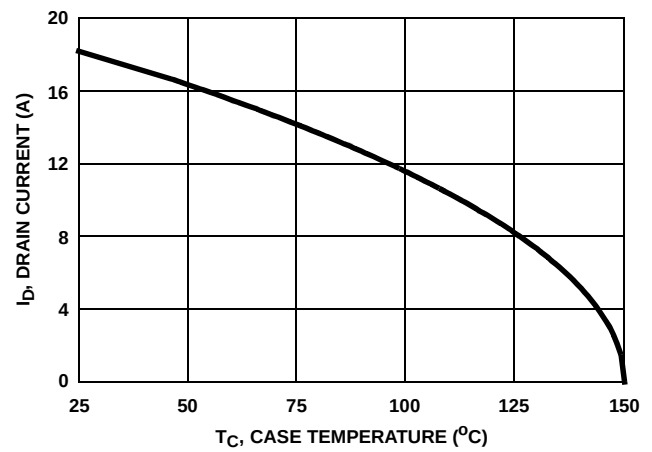


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

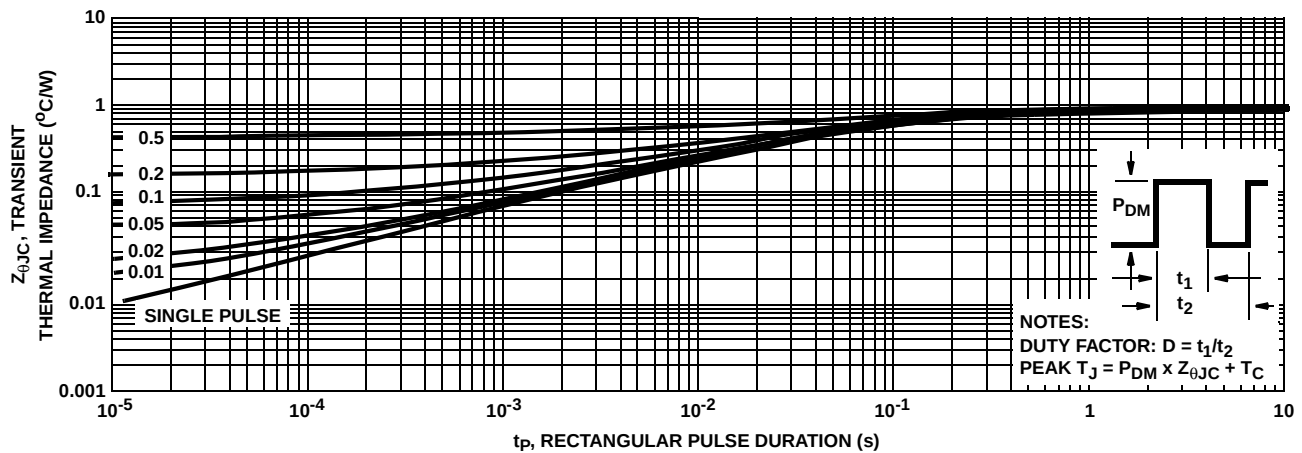


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

**Typical Performance Curves** Unless Otherwise Specified (Continued)

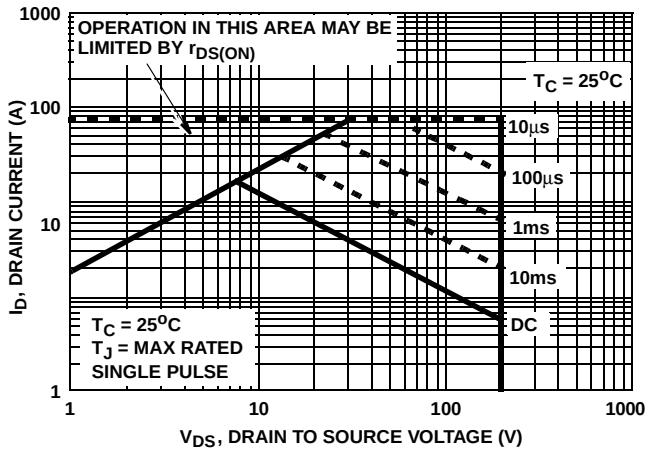


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

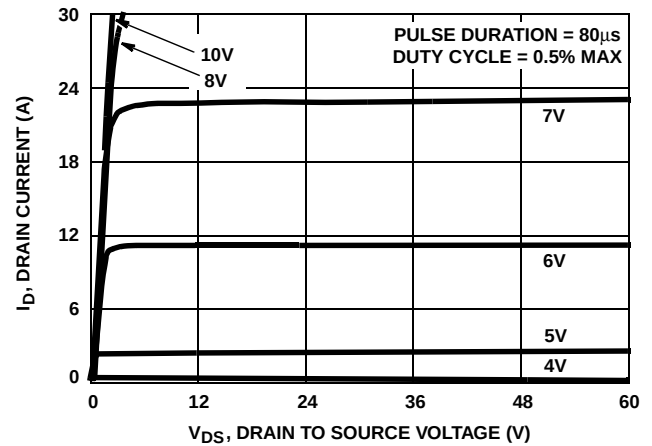


FIGURE 5. OUTPUT CHARACTERISTICS

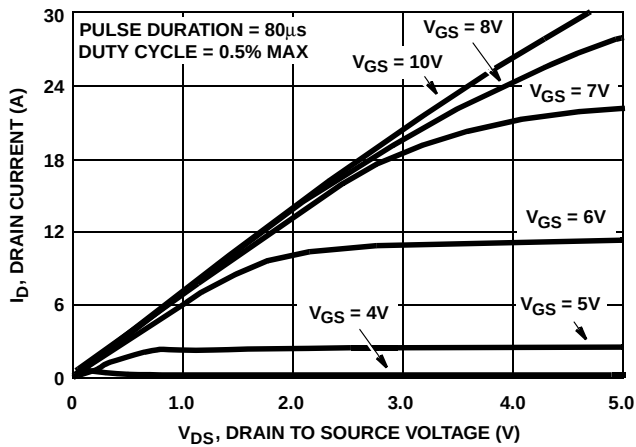


FIGURE 6. SATURATION CHARACTERISTICS

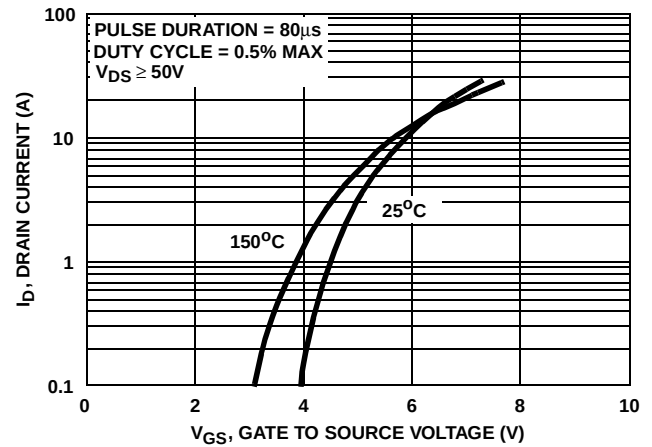


FIGURE 7. TRANSFER CHARACTERISTICS

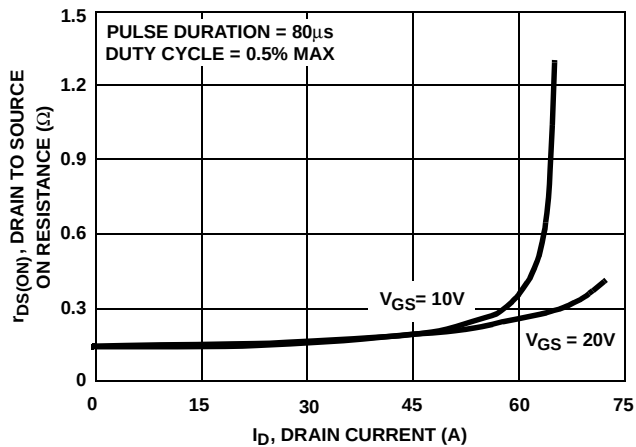


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

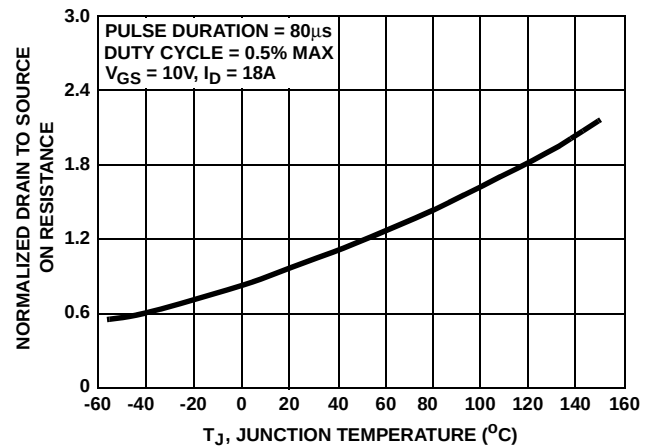


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

**Typical Performance Curves** Unless Otherwise Specified (Continued)

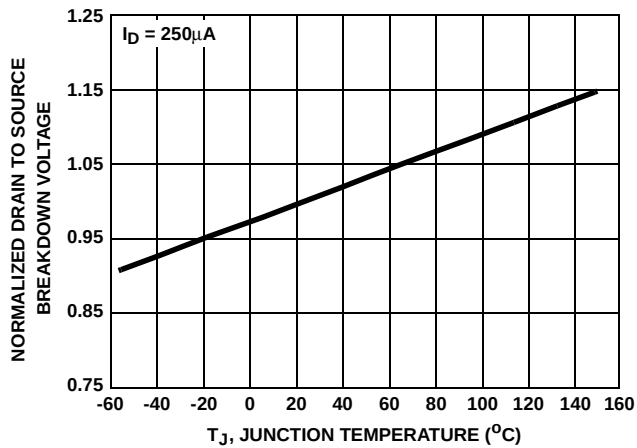


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

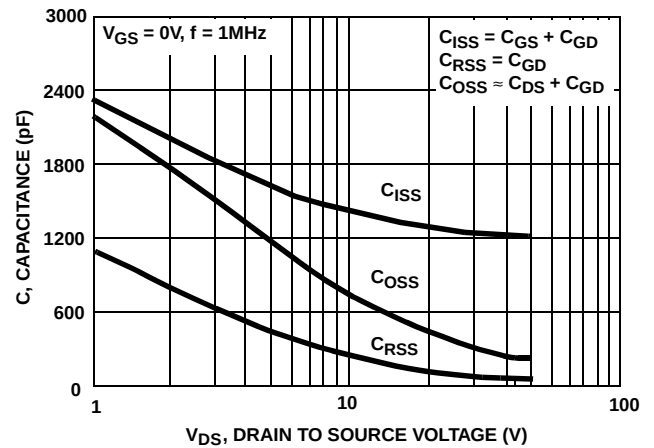


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

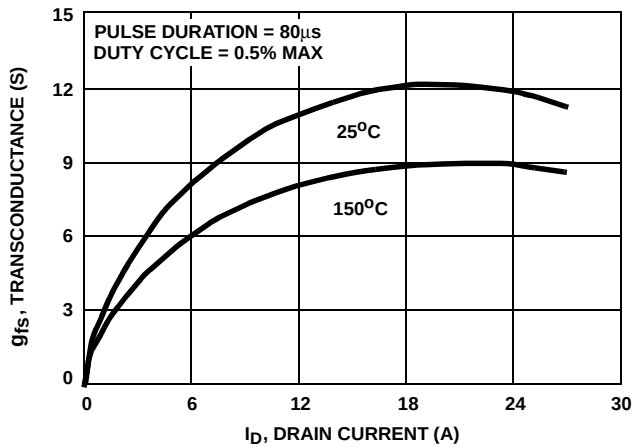


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

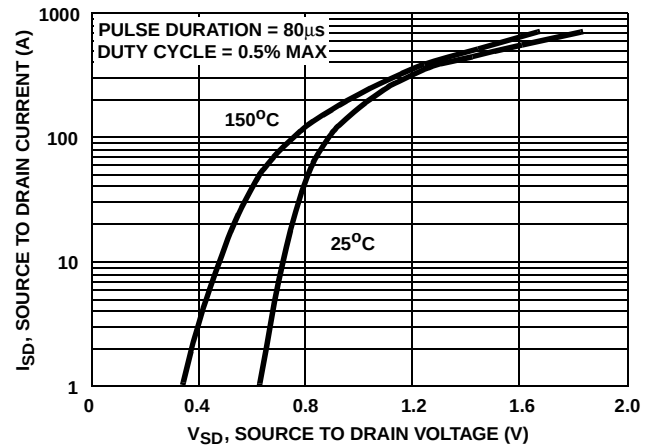


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

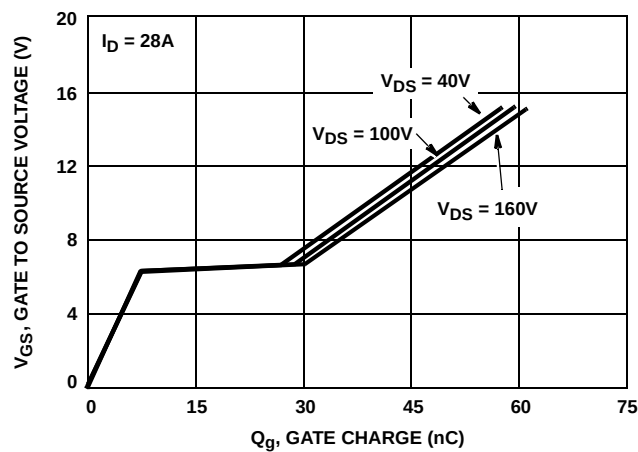


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

## Test Circuits and Waveforms

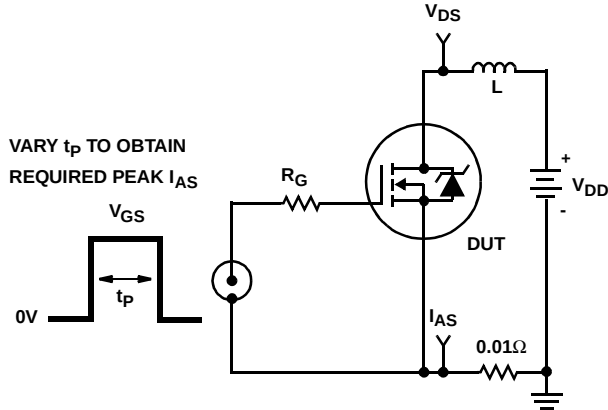


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

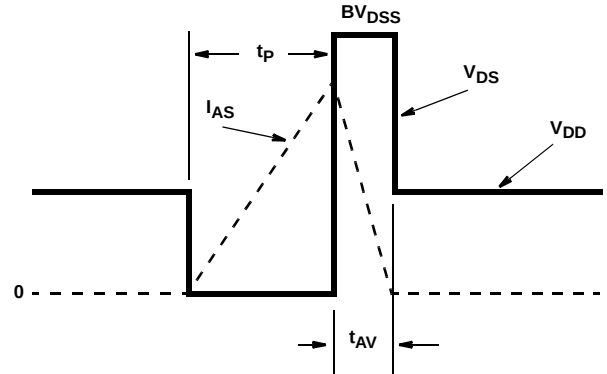


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

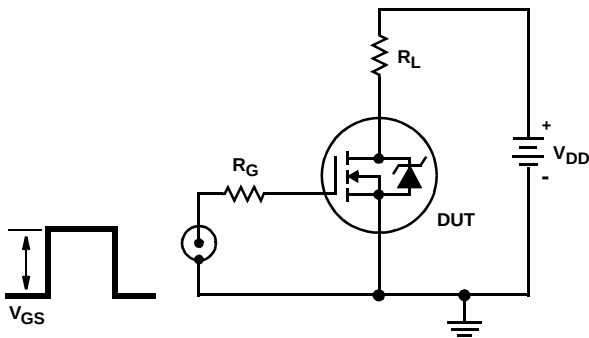


FIGURE 17. SWITCHING TIME TEST CIRCUIT

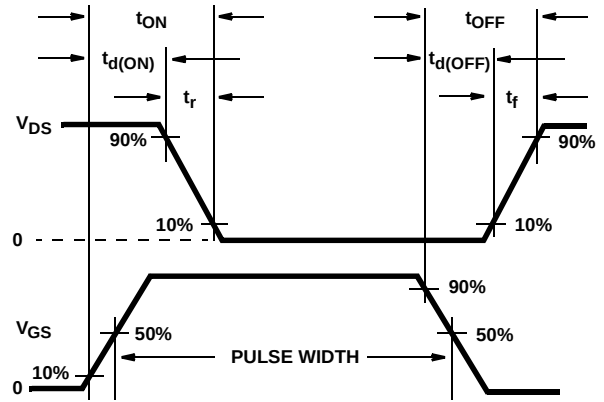


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

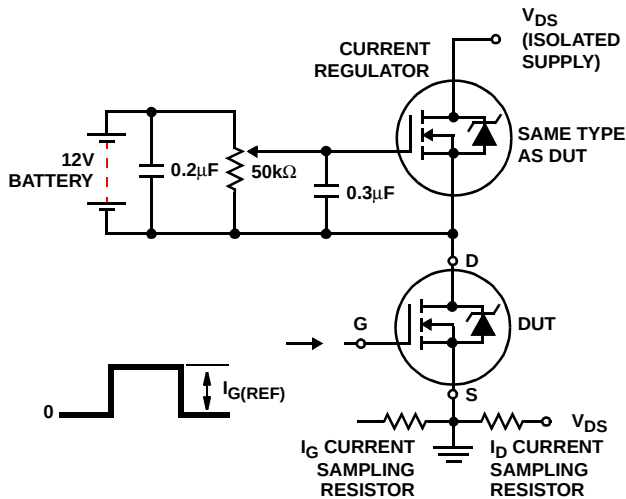


FIGURE 19. GATE CHARGE TEST CIRCUIT

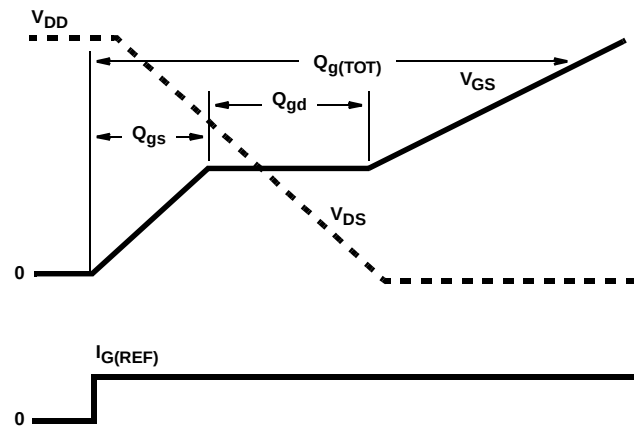


FIGURE 20. GATE CHARGE WAVEFORMS

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| Bottomless <sup>TM</sup>          | FAST <sup>r</sup> <sup>TM</sup>  | OPTOPLANAR <sup>TM</sup>         | STAR*POWER <sup>TM</sup>     |                   |
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| DenseTrench <sup>TM</sup>         | GTO <sup>TM</sup>                | Power247 <sup>TM</sup>           | SuperSOT <sup>TM</sup> -6    |                   |
| DOME <sup>TM</sup>                | HiSeC <sup>TM</sup>              | PowerTrench <sup>®</sup>         | SuperSOT <sup>TM</sup> -8    |                   |
| EcoSPARK <sup>TM</sup>            | ISOPLANAR <sup>TM</sup>          | QFET <sup>TM</sup>               | SyncFET <sup>TM</sup>        |                   |
| E <sup>2</sup> CMOS <sup>TM</sup> | LittleFET <sup>TM</sup>          | QS <sup>TM</sup>                 | TinyLogic <sup>TM</sup>      |                   |
| EnSigna <sup>TM</sup>             | MicroFET <sup>TM</sup>           | QT Optoelectronics <sup>TM</sup> | TruTranslation <sup>TM</sup> |                   |
| FACT <sup>TM</sup>                | MicroPak <sup>TM</sup>           | Quiet Series <sup>TM</sup>       | UHC <sup>TM</sup>            |                   |
| FACT Quiet Series <sup>TM</sup>   | MICROWIRE <sup>TM</sup>          | SILENT SWITCHER <sup>®</sup>     | UltraFET <sup>®</sup>        |                   |

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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status         | Definition                                                                                                                                                                                                            |
|--------------------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Advance Information      | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.                                                                                    |
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