

RGP10A - RGP10M

Features

- 1.0 ampere operation at $T_A = 55^\circ\text{C}$ with no thermal runaway.
- High temperature metallurgically bonded construction.
- Glass passivated cavity-free junction.
- Typical I_R less than $1\mu\text{A}$.
- Fast switching for high efficiency.



DO-41
COLOR BAND DENOTES CATHODE

Fast Rectifiers (Glass Passivated)

Absolute Maximum Ratings*

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value							Units
		10A	10B	10D	10G	10J	10K	10M	
V_{RRM}	Maximum Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, .375" lead length @ $T_L = 55^\circ\text{C}$	1.0							A
I_{FSM}	Non-repetitive Peak Forward Surge Current 8.3 ms Single Half-Sine-Wave	30							A
T_{stg}	Storage Temperature Range	-65 to +175							$^\circ\text{C}$
T_J	Operating Junction Temperature	-65 to +175							$^\circ\text{C}$

*These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	3.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	50	$^\circ\text{C}/\text{W}$

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Device							Units
		10A	10B	10D	10G	10J	10K	10M	
V_F	Forward Voltage @ 1.0 A	1.3							V
t_{rr}	Reverse Recovery Time $I_F = 0.5\text{ A}$, $I_R = 1.0\text{ A}$, $I_{tr} = 0.25\text{ A}$	150			250	500		ns	
I_R	Reverse Current @ rated V_R $T_A = 25^\circ\text{C}$ $T_A = 150^\circ\text{C}$	5.0 200							μA μA
C_T	Total Capacitance $V_R = 4.0\text{ V}$, $f = 1.0\text{ MHz}$	15							pF

Typical Characteristics

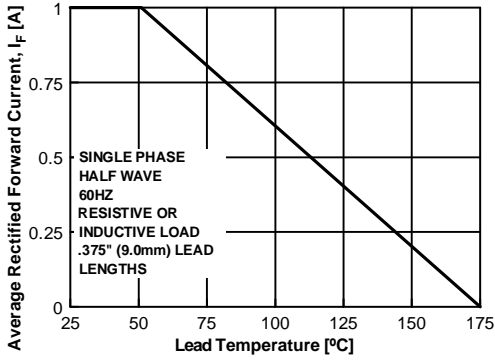


Figure 1. Forward Current Derating Curve

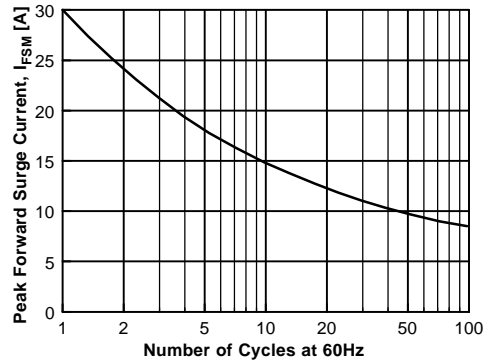


Figure 2. Non-Repetitive Surge Current

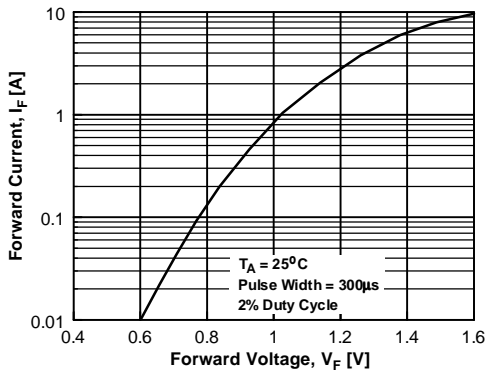


Figure 3. Forward Voltage Characteristics

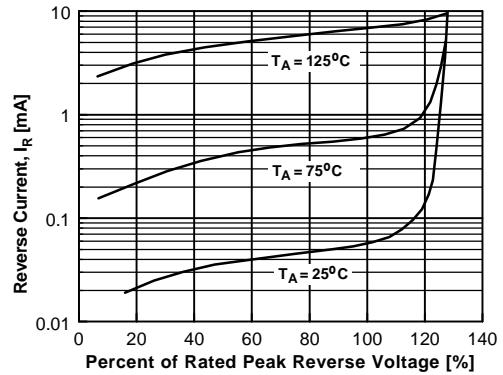


Figure 4. Reverse Current vs Reverse Voltage

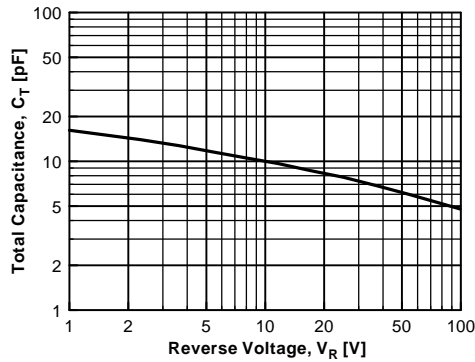
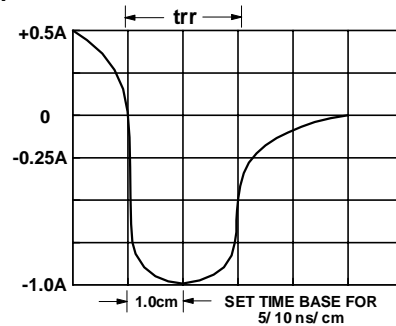
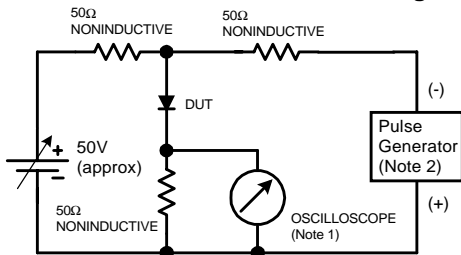


Figure 5. Total Capacitance



Reverse Recovery Time Characteristic and Test Circuit Diagram

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