

FEATURES

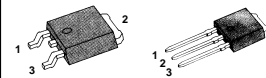
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μ A (Max.) @ $V_{DS} = -100V$
- Lower $R_{DS(ON)}$: 0.912 Ω (Typ.)

$$BV_{DSS} = -100 V$$

$$R_{DS(on)} = 1.2 \Omega$$

$$I_D = -2.8 A$$

D-PAK **I-PAK**



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

| Symbol | Characteristic | Value | Units |
|----------------|---|--------------|---------------|
| V_{DSS} | Drain-to-Source Voltage | -100 | V |
| I_D | Continuous Drain Current ($T_C=25^\circ C$) | -2.8 | A |
| | Continuous Drain Current ($T_C=100^\circ C$) | -2.0 | |
| I_{DM} | Drain Current-Pulsed ① | 11 | A |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulsed Avalanche Energy ② | 31 | mJ |
| I_{AR} | Avalanche Current ① | -2.8 | A |
| E_{AR} | Repetitive Avalanche Energy ① | 2.0 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | -6.5 | V/ns |
| P_D | Total Power Dissipation ($T_A=25^\circ C$) * | 2.5 | W |
| | Total Power Dissipation ($T_C=25^\circ C$) | 20 | W |
| | Linear Derating Factor | 0.16 | W/ $^\circ C$ |
| T_J, T_{STG} | Operating Junction and Storage Temperature Range | - 55 to +150 | $^\circ C$ |
| T_L | Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds | 300 | |

Thermal Resistance

| Symbol | Characteristic | Typ. | Max. | Units |
|-----------------|-----------------------|------|------|--------------|
| $R_{\theta JC}$ | Junction-to-Case | -- | 6.25 | $^\circ C/W$ |
| $R_{\theta JA}$ | Junction-to-Ambient * | -- | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient | -- | 110 | |

* When mounted on the minimum pad size recommended (PCB Mount).

Rev. B

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

| Symbol | Characteristic | Min. | Typ. | Max. | Units | Test Condition |
|------------------------|---|------|------|------|---------------------|--|
| BV_{DSS} | Drain-Source Breakdown Voltage | -100 | -- | -- | V | $V_{GS}=0V, I_D=-250\mu A$ |
| $\Delta BV/\Delta T_J$ | Breakdown Voltage Temp. Coeff. | -- | -0.1 | -- | V/ $^\circ\text{C}$ | $I_D=-250\mu A$ See Fig 7 |
| $V_{GS(th)}$ | Gate Threshold Voltage | -2.0 | -- | -4.0 | V | $V_{DS}=-5V, I_D=-250\mu A$ |
| I_{GSS} | Gate-Source Leakage, Forward | -- | -- | -100 | nA | $V_{GS}=-20V$ |
| | Gate-Source Leakage, Reverse | -- | -- | 100 | | $V_{GS}=20V$ |
| I_{DSS} | Drain-to-Source Leakage Current | -- | -- | -10 | μA | $V_{DS}=-100V$ |
| | | -- | -- | -100 | | $V_{DS}=-80V, T_C=125^\circ\text{C}$ |
| $R_{DS(on)}$ | Static Drain-Source On-State Resistance | -- | -- | 1.2 | Ω | $V_{GS}=-10V, I_D=-1.4A$ ④ |
| g_{fs} | Forward Transconductance | -- | 1.7 | -- | Ω | $V_{DS}=-40V, I_D=-1.4A$ ④ |
| C_{iss} | Input Capacitance | -- | 260 | 335 | pF | $V_{GS}=0V, V_{DS}=-25V, f=1\text{MHz}$ See Fig 5 |
| C_{oss} | Output Capacitance | -- | 50 | 80 | | |
| C_{rss} | Reverse Transfer Capacitance | -- | 17 | 25 | | |
| $t_{d(on)}$ | Turn-On Delay Time | -- | 10 | 30 | ns | $V_{DD}=-50V, I_D=-3.6A,$ $R_G=24\Omega$ See Fig 13 ④⑤ |
| t_r | Rise Time | -- | 20 | 50 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | -- | 25 | 60 | | |
| t_f | Fall Time | -- | 12 | 35 | | |
| Q_g | Total Gate Charge | -- | 9 | 10 | nC | $V_{DS}=-80V, V_{GS}=-10V,$ $I_D=-3.6A$ See Fig 6 & Fig 12 ④⑤ |
| Q_{gs} | Gate-Source Charge | -- | 1.5 | -- | | |
| Q_{gd} | Gate-Drain("Miller") Charge | -- | 4.3 | -- | | |

Source-Drain Diode Ratings and Characteristics

| Symbol | Characteristic | Min. | Typ. | Max. | Units | Test Condition |
|----------|---------------------------|------|------|------|---------------|--|
| I_S | Continuous Source Current | -- | -- | -2.8 | A | Integral reverse pn-diode in the MOSFET |
| I_{SM} | Pulsed-Source Current ① | -- | -- | -11 | | |
| V_{SD} | Diode Forward Voltage ④ | -- | -- | -3.8 | V | $T_J=25^\circ\text{C}, I_S=-2.8A, V_{GS}=0V$ |
| t_{rr} | Reverse Recovery Time | -- | 100 | -- | ns | $T_J=25^\circ\text{C}, I_F=-3.6A$ |
| Q_{rr} | Reverse Recovery Charge | -- | 0.35 | -- | μC | $di_F/dt=100A/\mu\text{s}$ ④ |

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
- ② $L=6.0\text{mH}, I_{AS}=-2.8A, V_{DD}=-25V, R_G=27\Omega^*,$ Starting $T_J=25^\circ\text{C}$
- ③ $I_{SD} \leq -3.6A, di/dt \leq 300A/\mu\text{s}, V_{DD} \leq BV_{DSS},$ Starting $T_J=25^\circ\text{C}$
- ④ Pulse Test : Pulse Width = 250 μs , Duty Cycle $\leq 2\%$
- ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

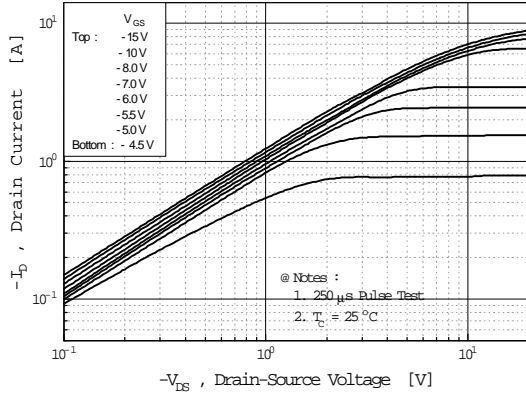


Fig 2. Transfer Characteristics

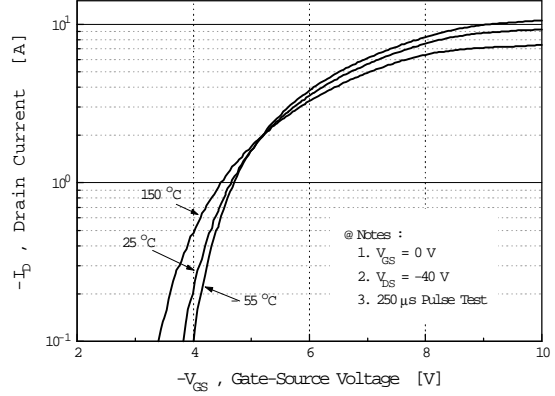


Fig 3. On-Resistance vs. Drain Current

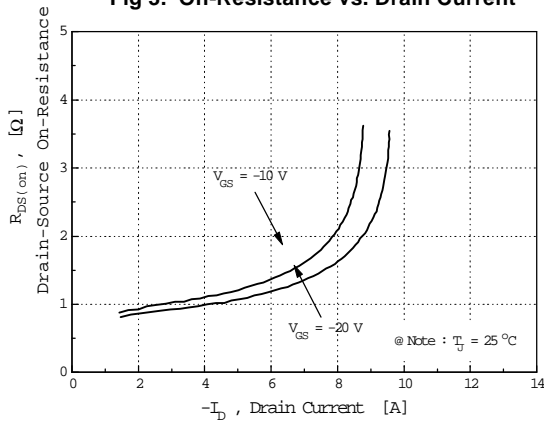


Fig 4. Source-Drain Diode Forward Voltage

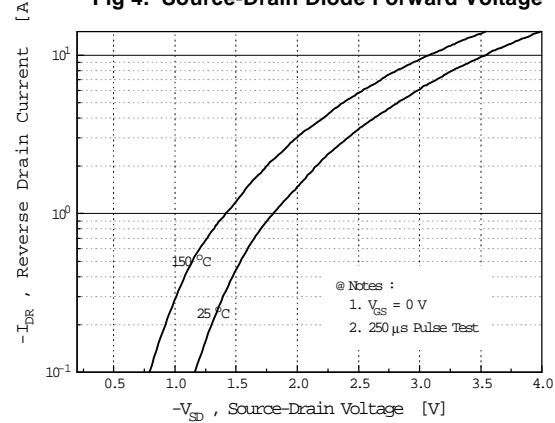


Fig 5. Capacitance vs. Drain-Source Voltage

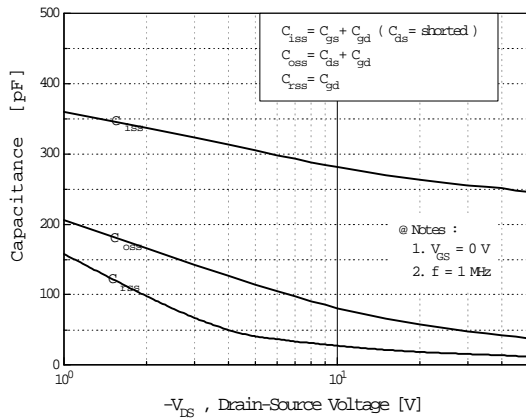
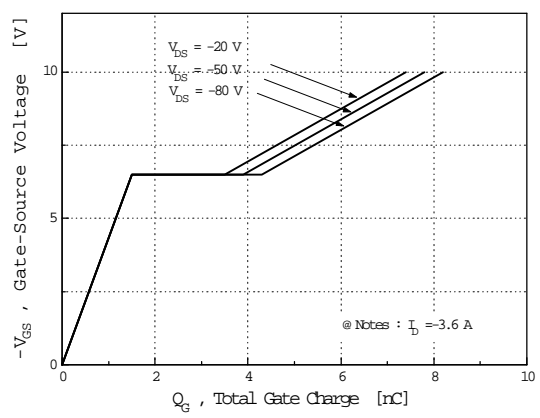


Fig 6. Gate Charge vs. Gate-Source Voltage



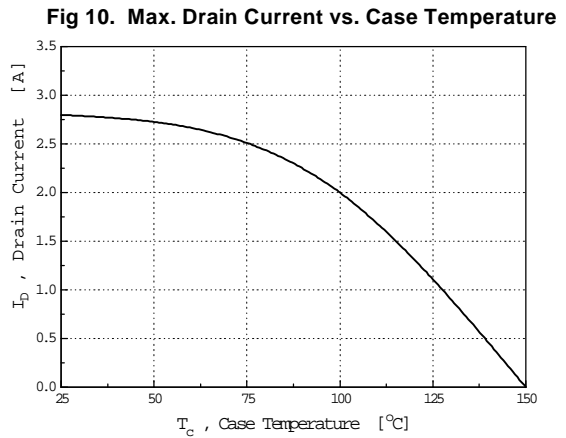
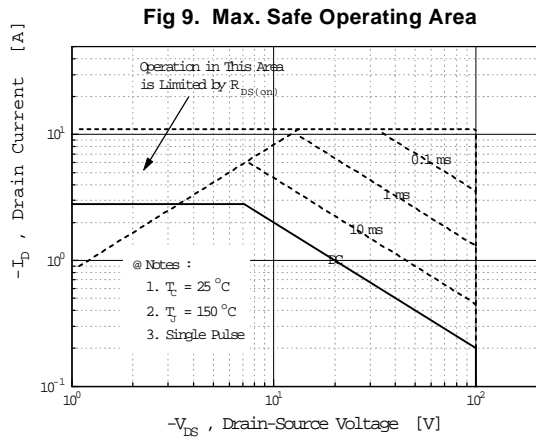
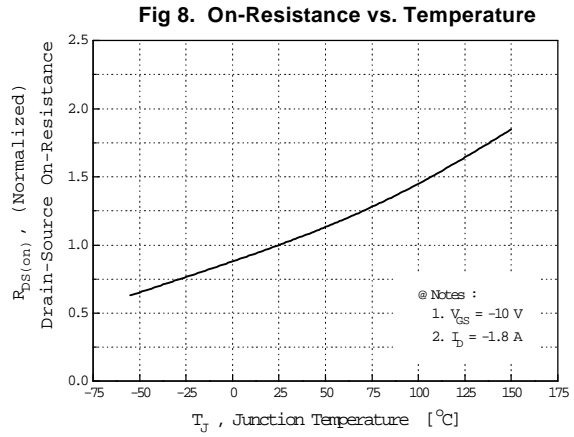
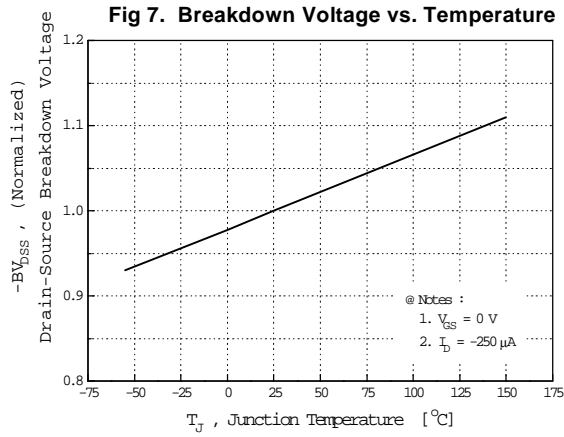


Fig 11. Thermal Response

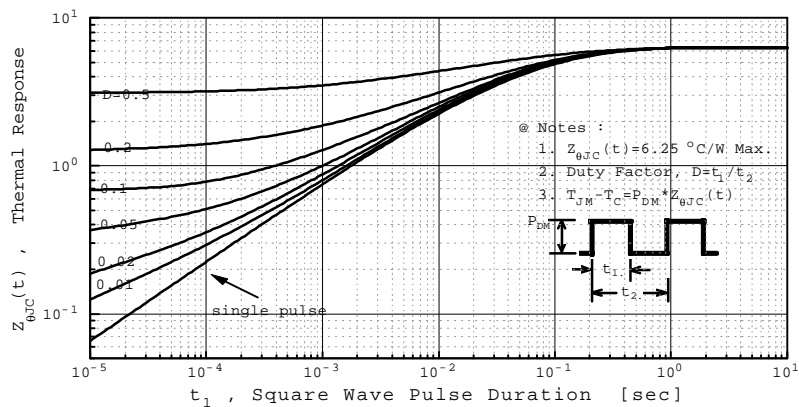


Fig 12. Gate Charge Test Circuit & Waveform

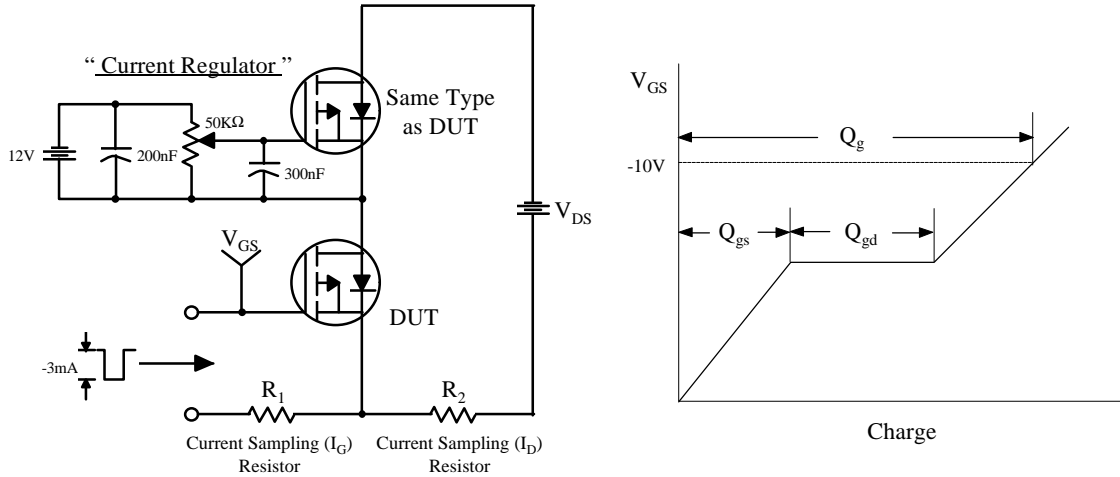


Fig 13. Resistive Switching Test Circuit & Waveforms

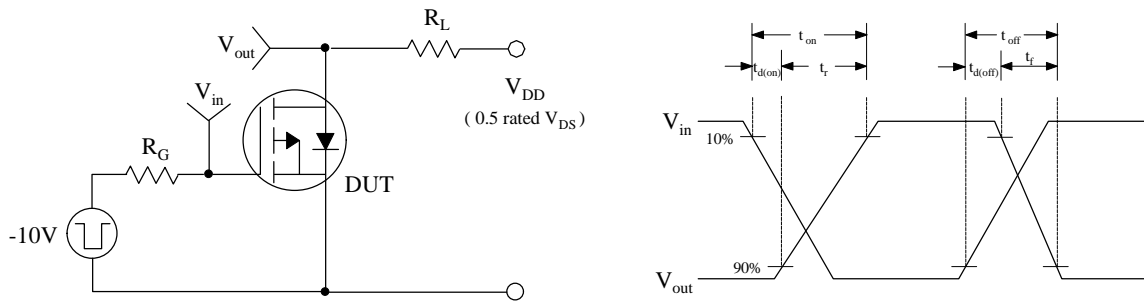


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

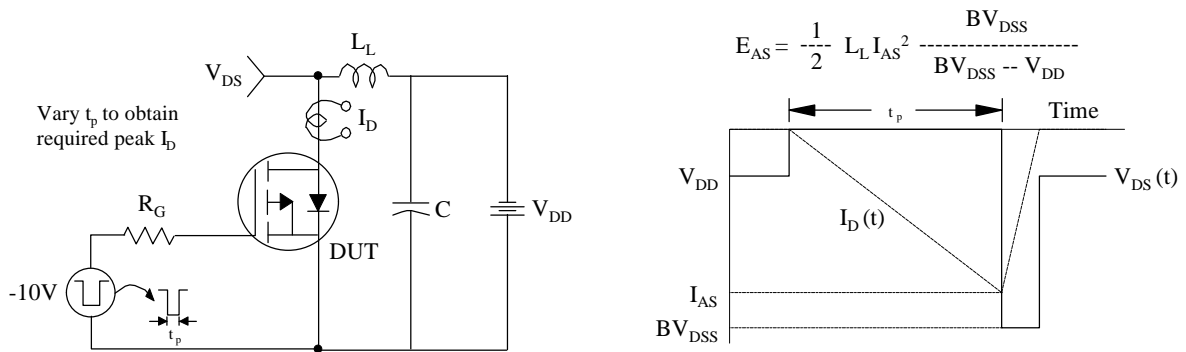
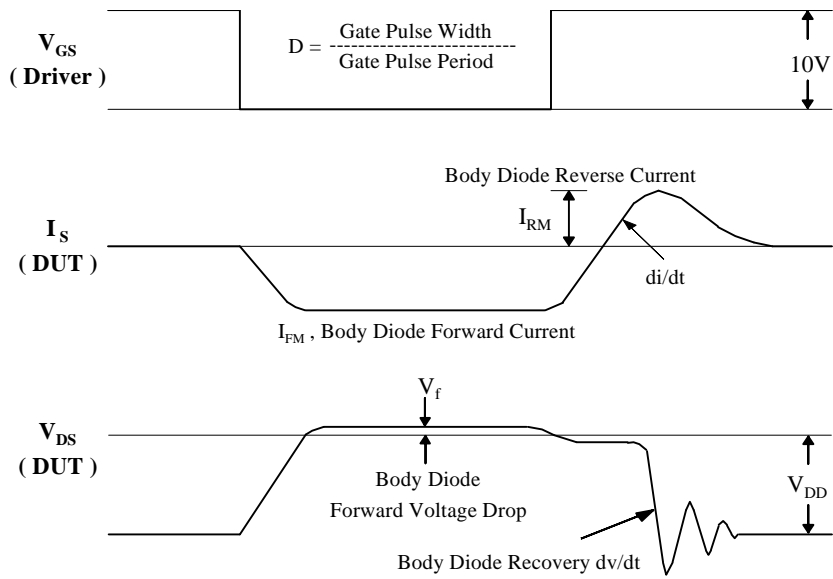
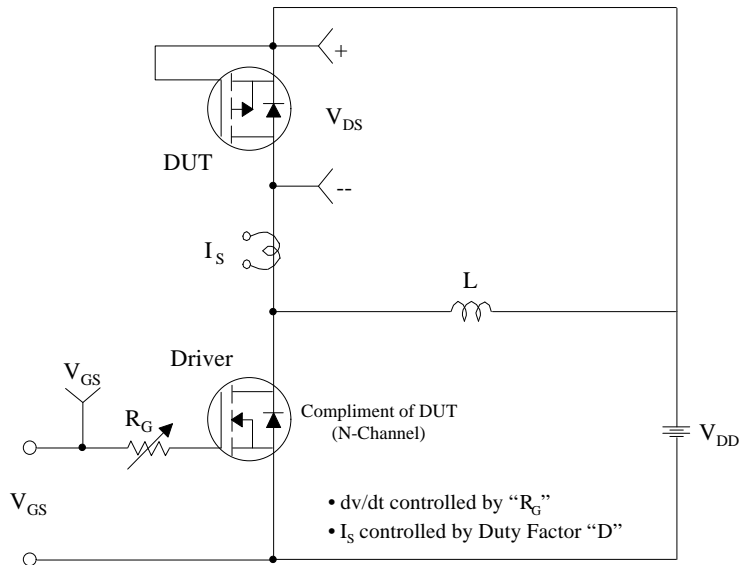


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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