

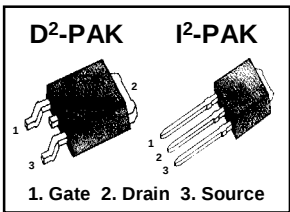
FEATURES

- n Avalanche Rugged Technology
- n Rugged Gate Oxide Technology
- n Lower Input Capacitance
- n Improved Gate Charge
- n Extended Safe Operating Area
- n 175°C Operating Temperature
- n Lower Leakage Current : 10 μA (Max.) @ V_{DS} = -100V
- n Low R_{DS(ON)} : 0.444 Ω (Typ.)

$BV_{DSS} = -100\text{ V}$

$R_{DS(on)} = 0.6\Omega$

$I_D = -6.0\text{ A}$



Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V _{DSS}	Drain-to-Source Voltage	-100	V
I _D	Continuous Drain Current (T _C =25°C)	-6.0	A
	Continuous Drain Current (T _C =100°C)	-4.0	
I _{DM}	Drain Current-Pulsed ①	-24	A
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS}	Single Pulsed Avalanche Energy ②	144	mJ
I _{AR}	Avalanche Current ①	-6.0	A
E _{AR}	Repetitive Avalanche Energy ①	4.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-6.5	V/ns
P _D	Total Power Dissipation (T _A =25°C) *	3.8	W
	Total Power Dissipation (T _C =25°C)	49	W
	Linear Derating Factor	0.33	W/°C
T _J , T _{STG}	Operating Junction and Storage Temperature Range	- 55 to +175	°C
T _L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	--	3.06	°C/W
R _{θJA}	Junction-to-Ambient *	--	40	
R _{θJA}	Junction-to-Ambient	--	62.5	

* When mounted on the minimum pad size recommended (PCB Mount).

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	-100	--	--	V	$V_{GS}=0V, I_D=-250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	-0.1	--	$V/^\circ\text{C}$	$I_D=-250\mu A$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	--	-4.0	V	$V_{DS}=-5V, I_D=-250\mu A$
I_{GSS}	Gate-Source Leakage, Forward	--	--	-100	nA	$V_{GS}=-20V$
	Gate-Source Leakage, Reverse	--	--	100		$V_{GS}=20V$
I_{DSS}	Drain-to-Source Leakage Current	--	--	-10	μA	$V_{DS}=-100V$
		--	--	-100		$V_{DS}=-80V, T_C=150^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.6	Ω	$V_{GS}=-10V, I_D=-3A$ ④
g_{fs}	Forward Transconductance	--	3.6	--	S	$V_{DS}=-40V, I_D=-3A$ ④
C_{iss}	Input Capacitance	--	425	550	pF	$V_{GS}=0V, V_{DS}=-25V, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	--	90	135		
C_{rss}	Reverse Transfer Capacitance	--	31	45		
$t_{d(on)}$	Turn-On Delay Time	--	11	30	ns	$V_{DD}=-50V, I_D=-6A,$ $R_G=18\Omega$ See Fig 13 ④⑤
t_r	Rise Time	--	21	50		
$t_{d(off)}$	Turn-Off Delay Time	--	34	80		
t_f	Fall Time	--	18	45		
Q_g	Total Gate Charge	--	16	20	nC	$V_{DS}=-80V, V_{GS}=-10V,$ $I_D=-6A$ See Fig 6 & Fig 12 ④⑤
Q_{gs}	Gate-Source Charge	--	3.1	--		
Q_{gd}	Gate-Drain("Miller") Charge	--	6.3	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	-6	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	-24		
V_{SD}	Diode Forward Voltage ④	--	--	-3.8	V	$T_J=25^\circ\text{C}, I_S=-6A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	105	--	ns	$T_J=25^\circ\text{C}, I_F=-6A$
Q_{rr}	Reverse Recovery Charge	--	0.4	--	μC	$di_F/dt=100A/\mu s$ ④

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② $L=6.0\text{mH}$, $I_{AS}=-6A$, $V_{DD}=-25V$, $R_G=27\Omega^*$, Starting $T_J=25^\circ\text{C}$ ③ $I_{SD}\leq -6A$, $di/dt\leq 350A/\mu s$, $V_{DD}\leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$ ④ Pulse Test : Pulse Width = $250\mu s$, Duty Cycle $\leq 2\%$

⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

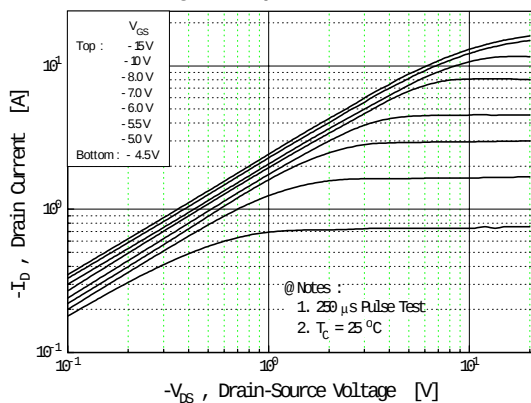


Fig 2. Transfer Characteristics

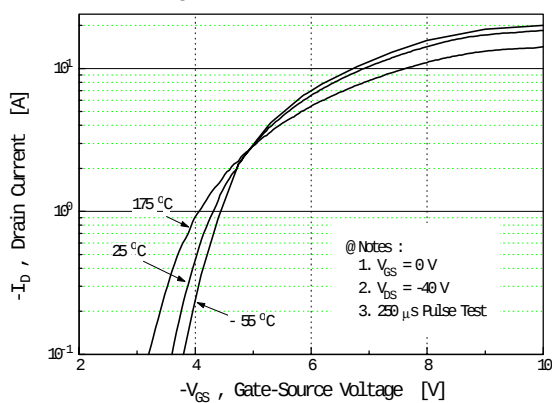


Fig 3. On-Resistance vs. Drain Current

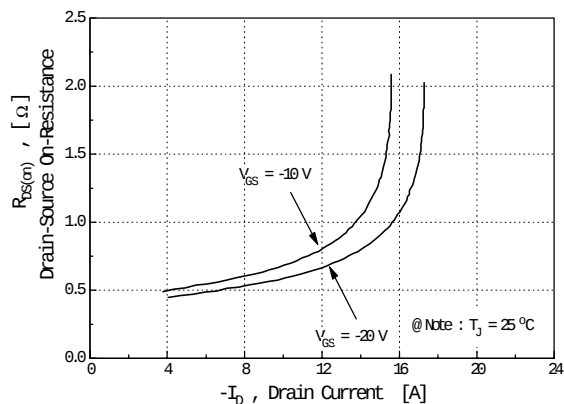


Fig 4. Source-Drain Diode Forward Voltage

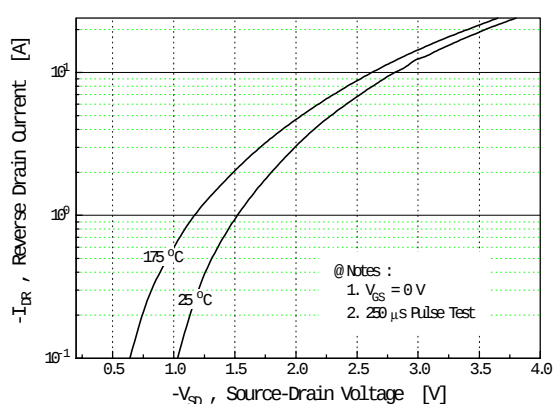


Fig 5. Capacitance vs. Drain-Source Voltage

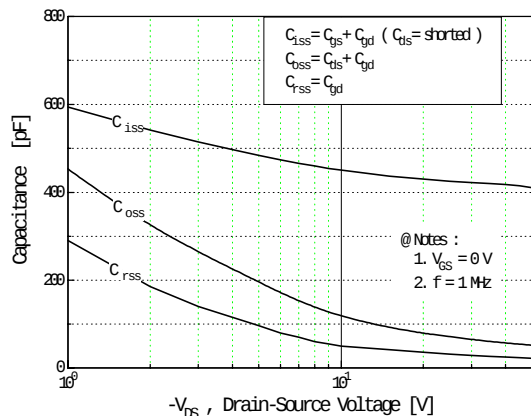


Fig 6. Gate Charge vs. Gate-Source Voltage

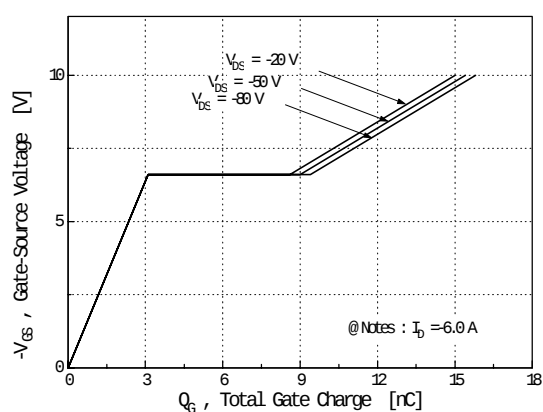


Fig 7. Breakdown Voltage vs. Temperature

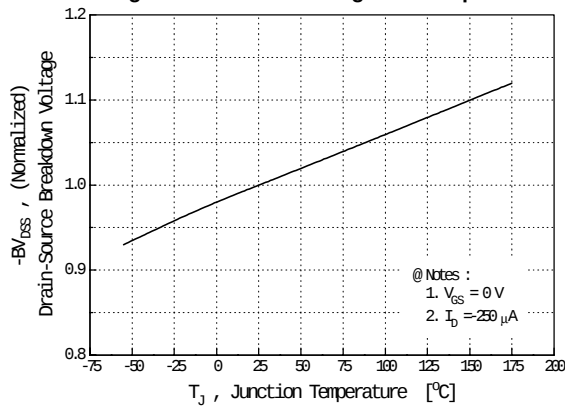


Fig 8. On-Resistance vs. Temperature

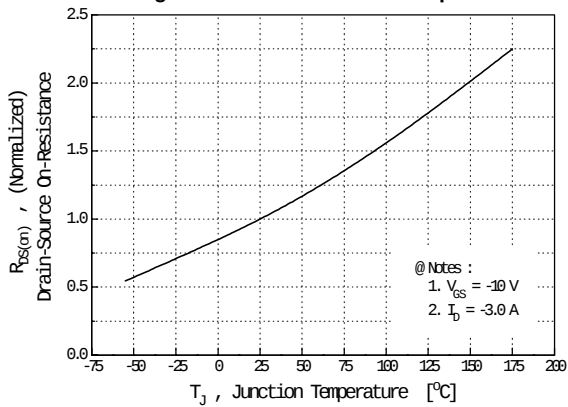


Fig 9. Max. Safe Operating Area

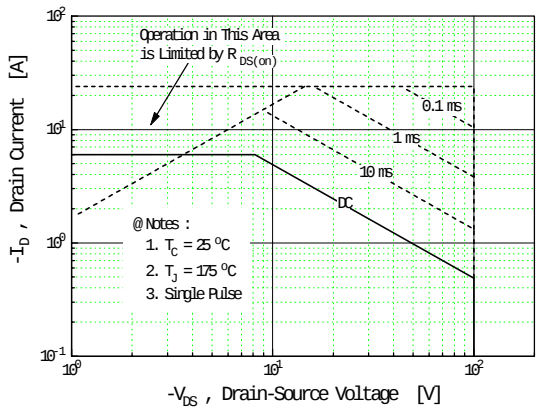


Fig 10. Max. Drain Current vs. Case Temperature

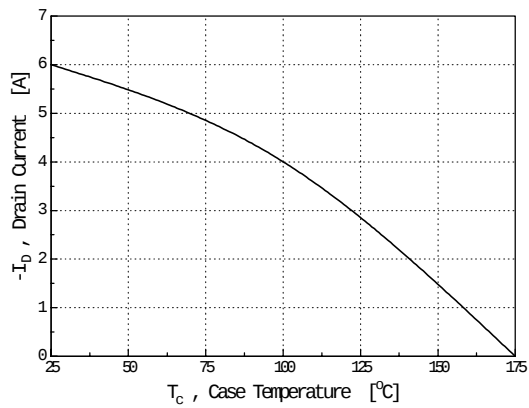
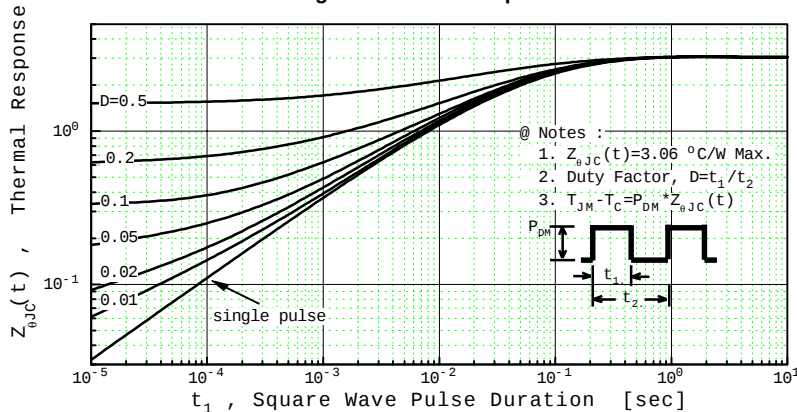
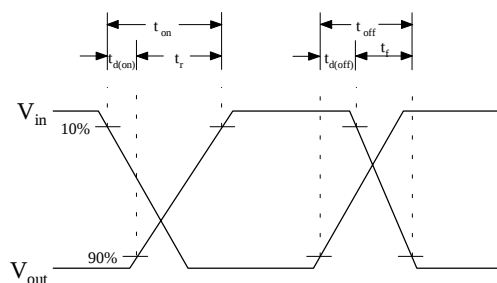
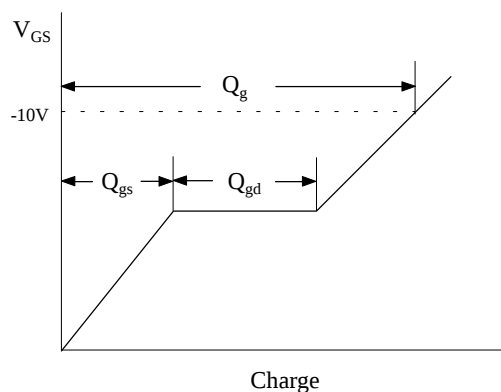


Fig 11. Thermal Response



The diagram shows a circuit for characterizing a Device Under Test (DUT). A 12V DC source is connected to a network of components: a 200nF capacitor, a 50KΩ resistor, and a 300nF capacitor. The output of this network is connected to the gate of a MOSFET labeled "Current Regulator". The drain of this MOSFET is connected to the gate of the DUT MOSFET. The DUT MOSFET's drain is connected to a positive supply V_{DS} through a resistor R_2 . The source of the DUT MOSFET is connected to ground through a resistor R_1 . A pulse generator, indicated by a square wave symbol and labeled "-3mA", is connected to the source of the DUT MOSFET. The current through R_1 is labeled "Current Sampling (I_G) Resistor", and the current through R_2 is labeled "Current Sampling (I_D) Resistor".



Vary t_p to obtain required peak I_D

$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 - \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

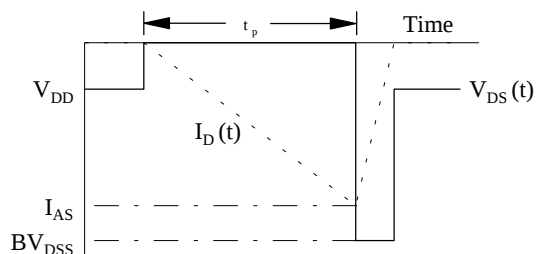
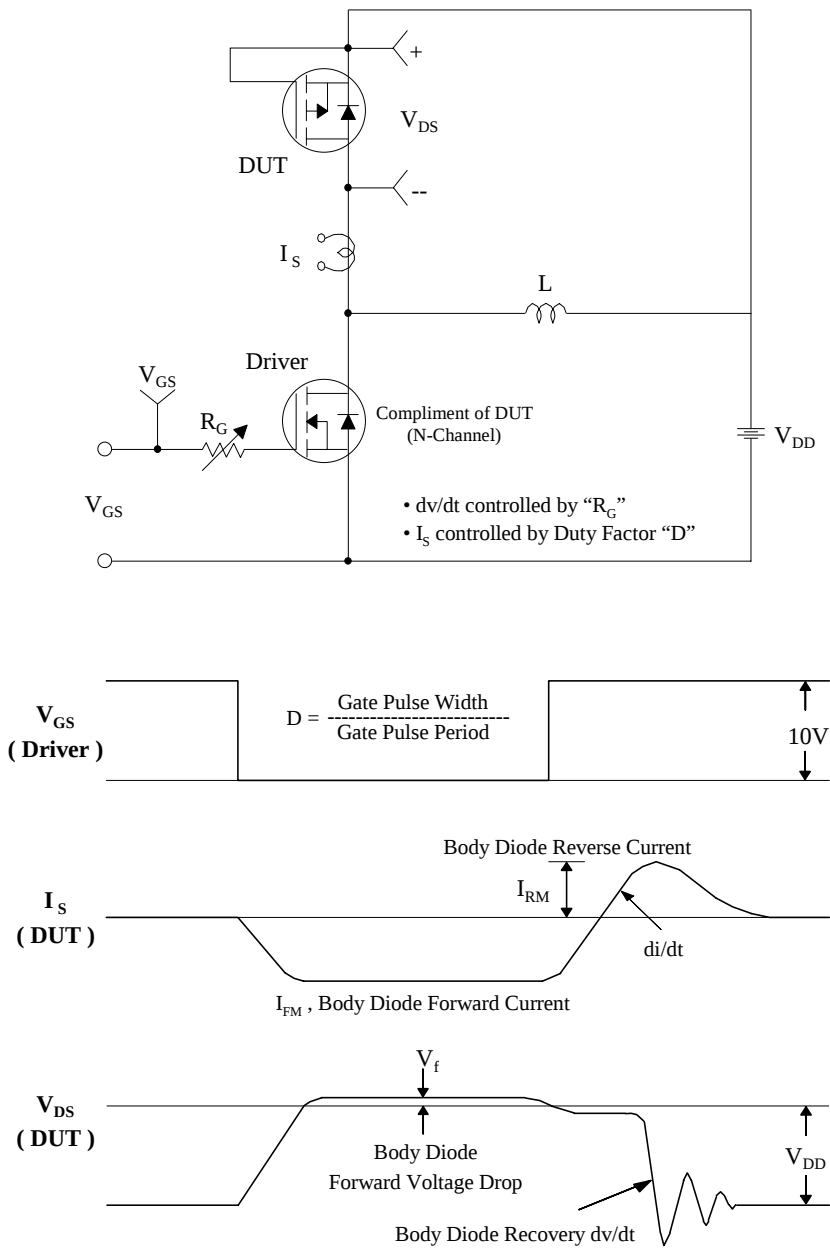


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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