

Si4822DY Single N-Channel, Logic Level, PowerTrench™ MOSFET

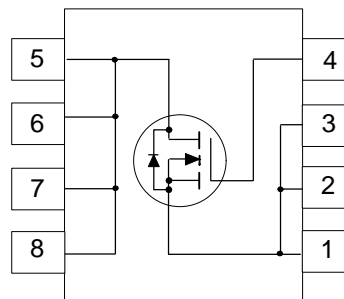
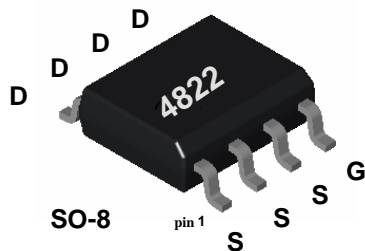
General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 12.5 A, 30 V. $R_{DS(ON)} = 0.0095 \Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 0.013 \Omega @ V_{GS} = 4.5 \text{ V}$.
- Fast switching speed.
- Low gate charge.
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and current handling capability.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Si4822DY	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note 1a)	12.5	A
	- Pulsed	50	
P_D	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

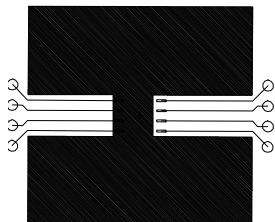
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

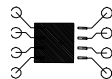
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V	
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$		33		mV / $^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA	
					10	μA	
		$T_J = 55\text{ }^\circ\text{C}$					
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA	
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA	
ON CHARACTERISTICS (Note 2)							
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$		-4.5		mV / $^\circ\text{C}$	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1	1.6	3	V
				0.8	1.3	2.4	
		$T_J = 125\text{ }^\circ\text{C}$					
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 12.5\text{ A}$		0.008	0.0095	Ω	
				0.012	0.016		
				0.0105	0.013		
		$T_J = 125\text{ }^\circ\text{C}$					
		$V_{GS} = 4.5\text{ V}, I_D = 10.5\text{ A}$					
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	25			A	
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 12.5\text{ A}$		35		S	
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2180		pF	
C_{oss}	Output Capacitance			500		pF	
C_{rss}	Reverse Transfer Capacitance			255		pF	
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DS} = 10\text{ V}, I_D = 1\text{ A}$		13	24	ns	
t_r	Turn - On Rise Time		$V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		14	26	ns
$t_{D(off)}$	Turn - Off Delay Time			43	70	ns	
t_f	Turn - Off Fall Time		15	27	ns		
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 12.5\text{ A},$ $V_{GS} = 5\text{ V}$		23	33	nC	
Q_{gs}	Gate-Source Charge			7		nC	
Q_{gd}	Gate-Drain Charge			11		nC	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.1	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.72	1.2	V	

Notes:

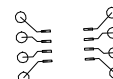
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50\text{ }^\circ\text{C/W}$ on a 1 in^2 pad of 2oz copper.



b. $105\text{ }^\circ\text{C/W}$ on a 0.04 in^2 pad of 2oz copper.



c. $125\text{ }^\circ\text{C/W}$ on a 0.006 in^2 pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

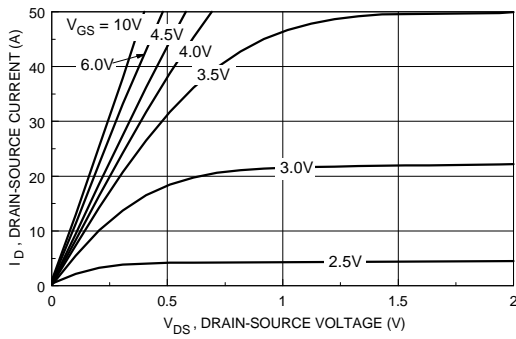


Figure 1. On-Region Characteristics.

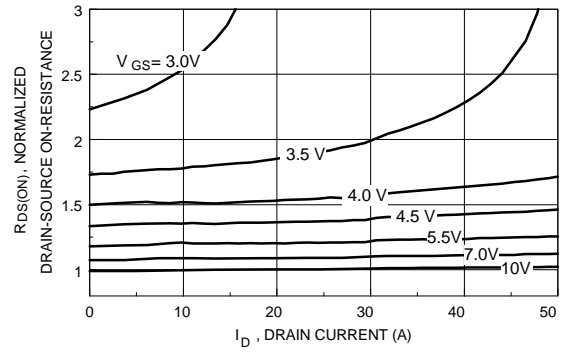


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

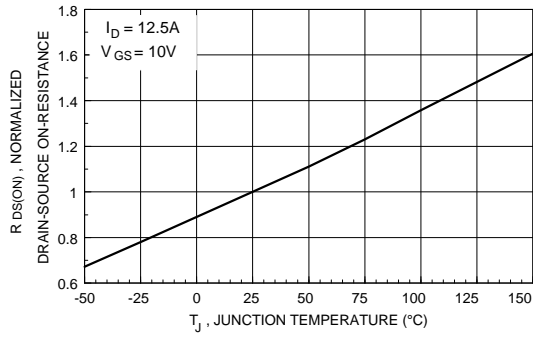


Figure 3. On-Resistance Variation with Temperature.

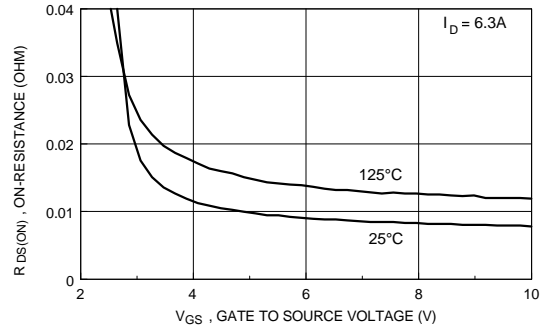


Figure 4. On Resistance Variation with Gate-to-Source Voltage.

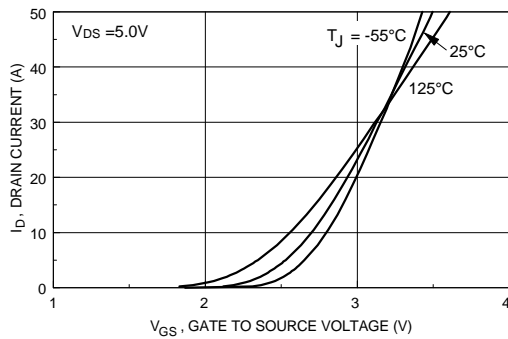


Figure 5. Transfer Characteristics.

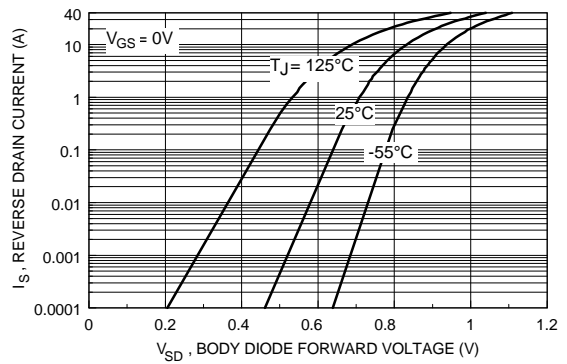


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical And Thermal Characteristics

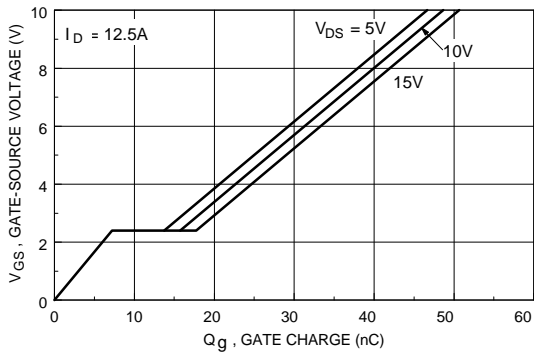


Figure 7. Gate Charge Characteristics.

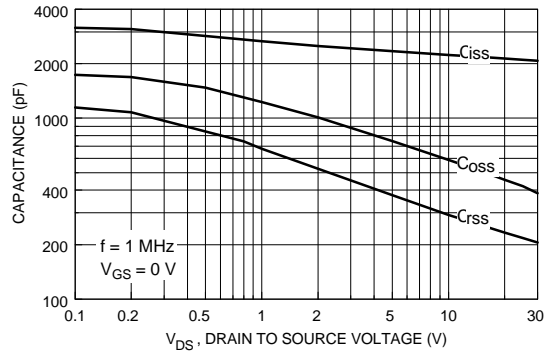


Figure 8. Capacitance Characteristics.

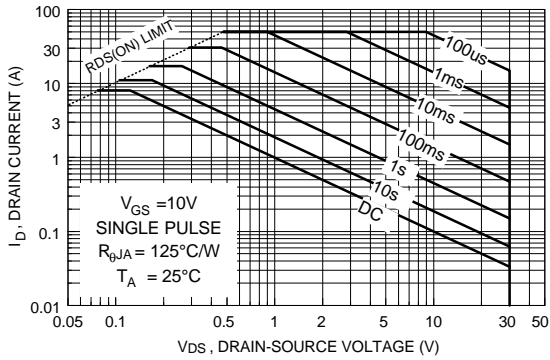


Figure 9. Maximum Safe Operating Area.

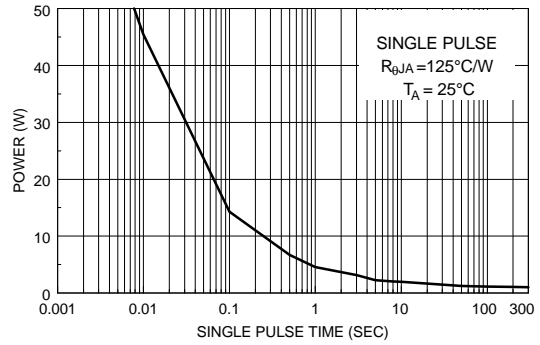


Figure 10. Single Pulse Maximum Power Dissipation.

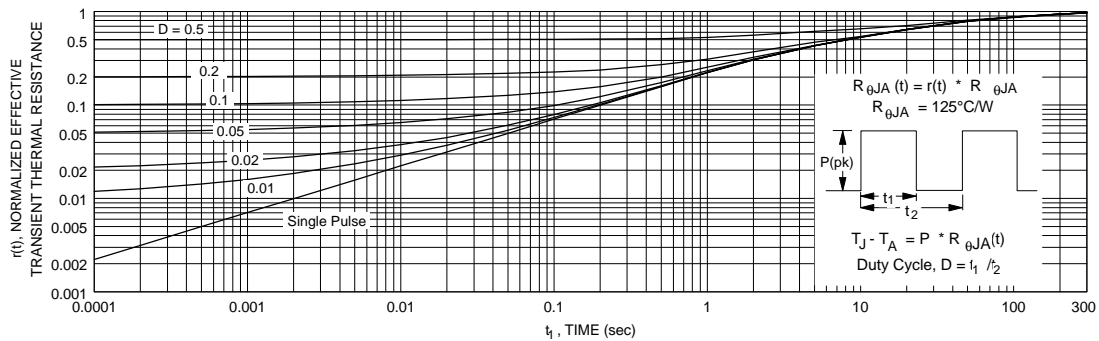


Figure 11. Transient Thermal Response Curve .

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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