

SI6928DQ

Dual 30V N-Channel PowerTrench® MOSFET

General Description

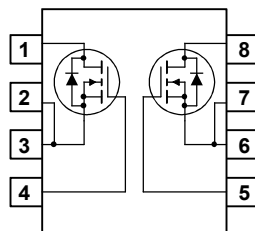
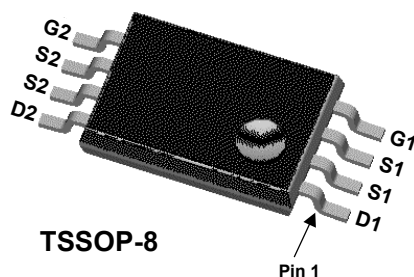
This N-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V to 20V).

Applications

- Load switch
- Motor drive
- DC/DC conversion
- Power management

Features

- 4 A, 30 V. $R_{DS(ON)} = 35\text{ m}\Omega @ V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 50\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- Extended V_{GSS} range ($\pm 20\text{V}$) for battery applications
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1a)	4.0	A
	– Pulsed	20	
P_D	Maximum Power Dissipation (Note 1a) (Note 1b)	1.3	W
		1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a) (Note 1b)	100	$^\circ\text{C/W}$
		125	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
6928	SI6928DQ	13"	12mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		20		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			1 5	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C		-5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 4.0\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 3.4\text{ A}$		20 26	35 50	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	20			A
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 4.0\text{ A}$		26		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		830		pF
C_{oss}	Output Capacitance			183		pF
C_{rss}	Reverse Transfer Capacitance			78		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		6	12	ns
t_r	Turn–On Rise Time			10	20	ns
$t_{d(off)}$	Turn–Off Delay Time			18	32	ns
t_f	Turn–Off Fall Time			5	10	ns
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = 1.25\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$		17	60	ns
Q_g	Gate Charge	$V_{DS} = 15\text{ V}, V_{GS} = 5\text{ V}, I_D = 4.0\text{ A}$		8	14	nC
Q_{gt}	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 4.0\text{ A},$ $V_{GS} = 10\text{ V}$		15	30	nC
Q_{gs}	Gate–Source Charge			2.8		nC
Q_{gd}	Gate–Drain Charge			3		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current				1.25	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.25\text{ A}$ (Note 2)		0.73	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

- a) $R_{\theta JA}$ is $100^\circ\text{C}/\text{W}$ (steady state) when mounted on a 1 inch² copper pad on FR-4.
b) $R_{\theta JA}$ is $125^\circ\text{C}/\text{W}$ (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

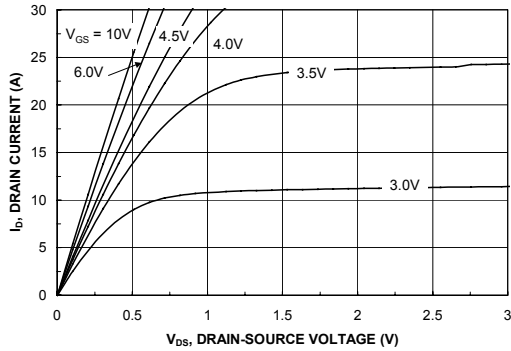


Figure 1. On-Region Characteristics.

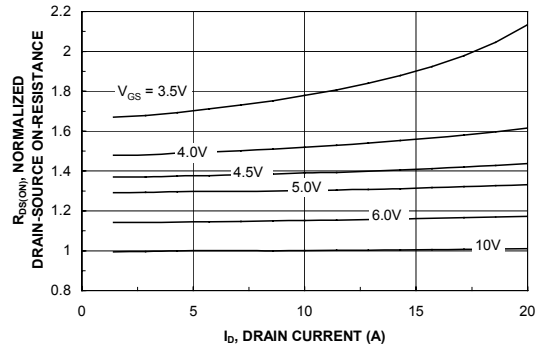


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

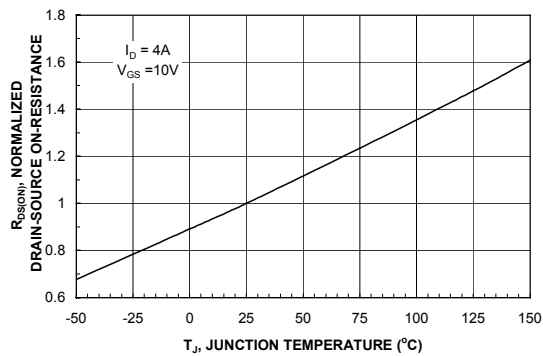


Figure 3. On-Resistance Variation with Temperature.

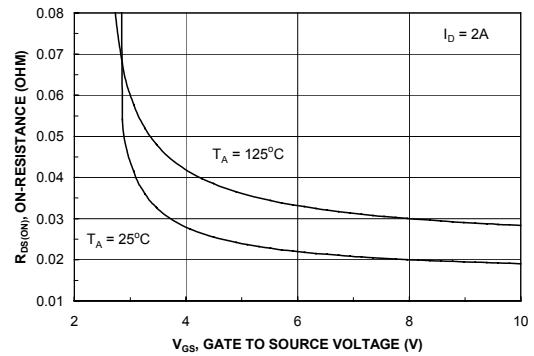


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

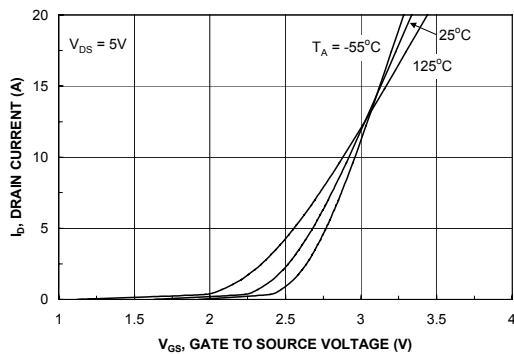


Figure 5. Transfer Characteristics.

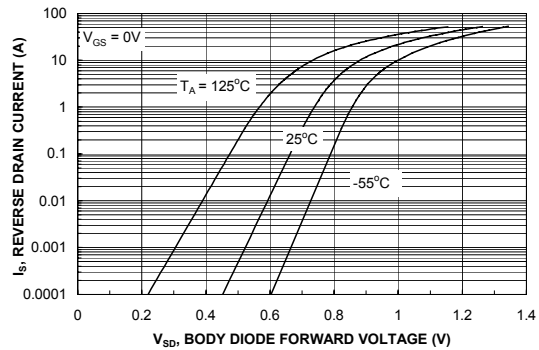


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

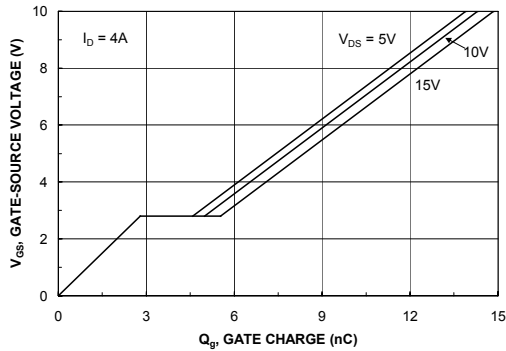


Figure 7. Gate Charge Characteristics.

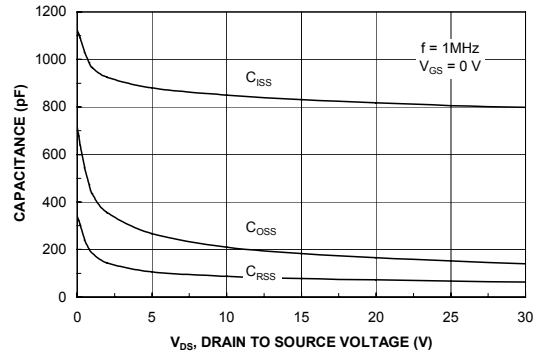


Figure 8. Capacitance Characteristics.

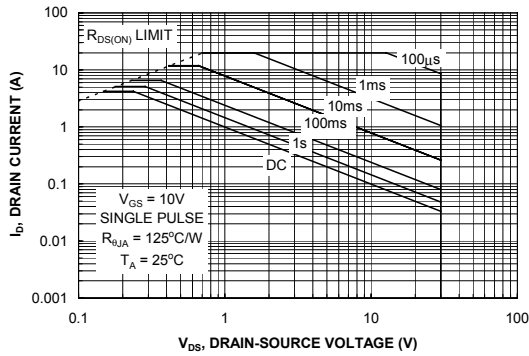


Figure 9. Maximum Safe Operating Area.

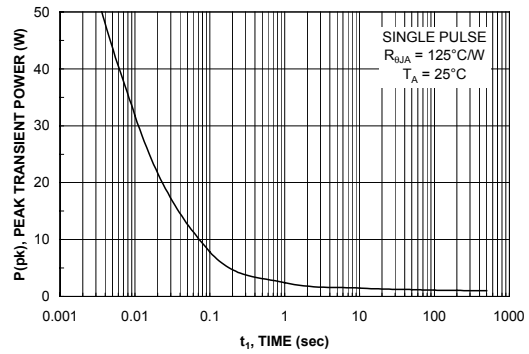


Figure 10. Single Pulse Maximum Power Dissipation.

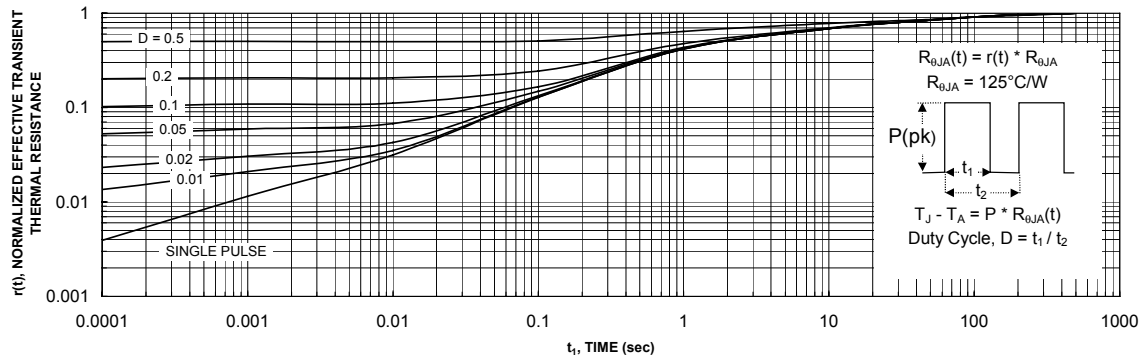


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
 Transient thermal response will change depending on the circuit board design.

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