

Si6953DQ

Dual 20V P-Channel PowerTrench® MOSFET

General Description

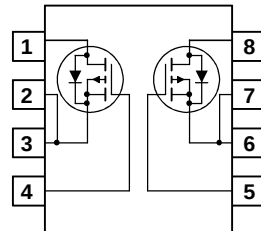
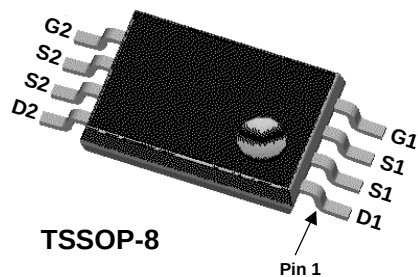
This P-Channel MOSFET is a rugged gate version of Fairchild's Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 20V).

Applications

- Load switch
- Battery protection
- DC/DC conversion
- Power management

Features

- –1.9 A, –20 V, $R_{DS(ON)} = 170\text{ m}\Omega$ @ $V_{GS} = -10\text{ V}$.
 $R_{DS(ON)} = 320\text{ m}\Omega$ @ $V_{GS} = -4.5\text{ V}$.
- Extended V_{GSS} range ($\pm 20\text{ V}$) for battery applications
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	–20	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1)	–1.9	A
	– Pulsed	–15	
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.0	W
		0.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$

Thermal Characteristic

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a) (Note 1b)	100	$^\circ\text{C/W}$
		125	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
6953	Si6953DQ	13"	12mm	2500 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = –250 μA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C		–22		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = –20 V, V _{GS} = 0 V			–1	μA
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = –20 V, V _{DS} = 0 V			–100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
On Characteristics (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = –250 μA	–1	–1.8	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C		4		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = –10 V, I _D = –1.9 A V _{GS} = –4.5 V, I _D = –1.3 A V _{GS} = –10 V, I _D = –1.9 A, T _J =125°C		96 151 134	170 320 254	mΩ
I _{D(on)}	On–State Drain Current	V _{GS} = –10 V, V _{DS} = –5 V	–10			A
g _{FS}	Forward Transconductance	V _{DS} = –15 V, I _D = –1.9 A		4		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = –10 V, V _{GS} = 0 V, f = 1.0 MHz		218		pF
C _{oss}	Output Capacitance			65		pF
C _{rss}	Reverse Transfer Capacitance			31		pF
Switching Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	V _{DD} = –10V, I _D = –1 A, V _{GS} = –10 V, R _{GEN} = 6 Ω		6	20	ns
t _r	Turn–On Rise Time			15	25	ns
t _{d(off)}	Turn–Off Delay Time			12	30	ns
t _f	Turn–Off Fall Time			1.5	15	ns
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _F = 1.5 A, dI _F /dt = 100A/μs		11	70	ns
Q _g	Total Gate Charge	V _{DS} = –10V, I _D = –1.9 A, V _{GS} = –10 V		4	10	nC
Q _{gs}	Gate–Source Charge			0.9		nC
Q _{gd}	Gate–Drain Charge			0.7		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain–Source Diode Forward Current				–1.25	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –1.25 A (Note 2)		–0.8	–1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

- a) $R_{\theta JA}$ is 100°C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.
b) $R_{\theta JA}$ is 125°C/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

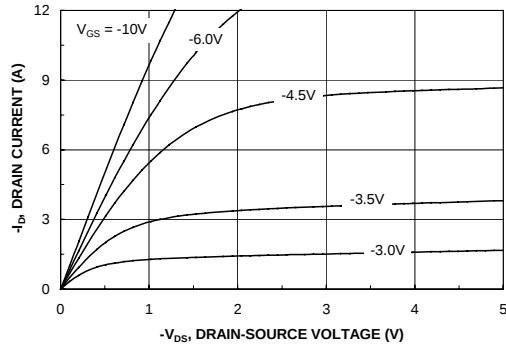


Figure 1. On-Region Characteristics.

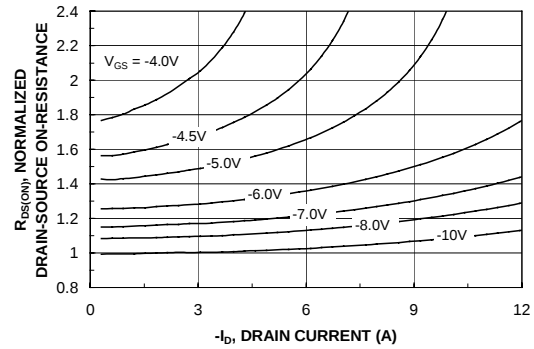


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

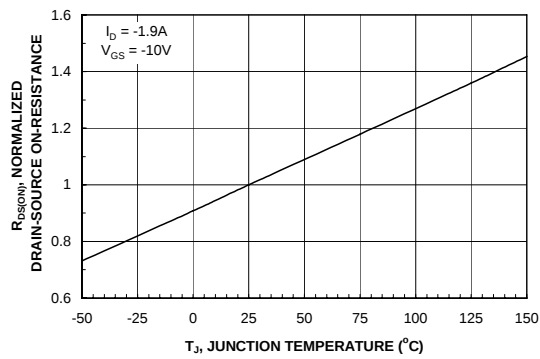


Figure 3. On-Resistance Variation with Temperature.

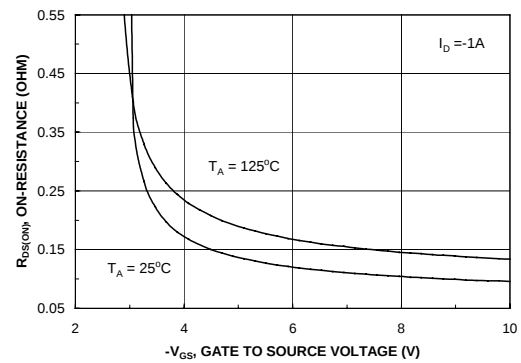


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

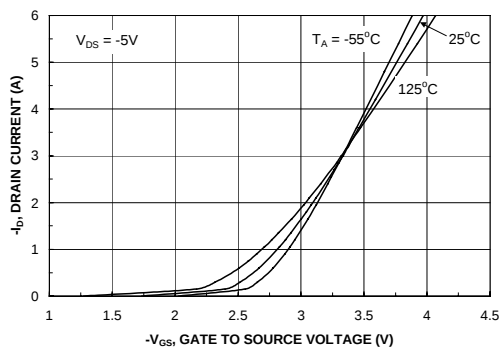


Figure 5. Transfer Characteristics.

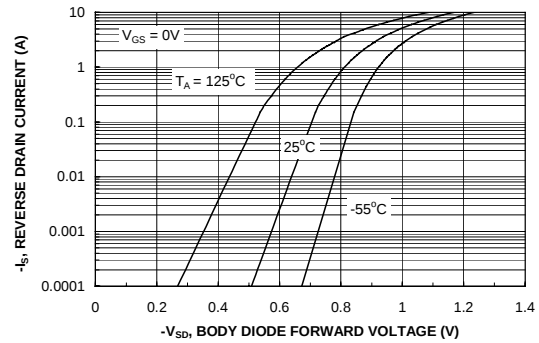


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

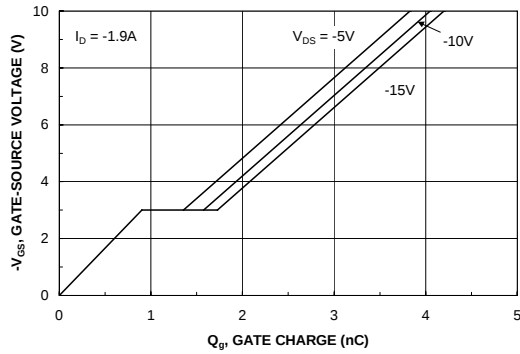


Figure 7. Gate Charge Characteristics.

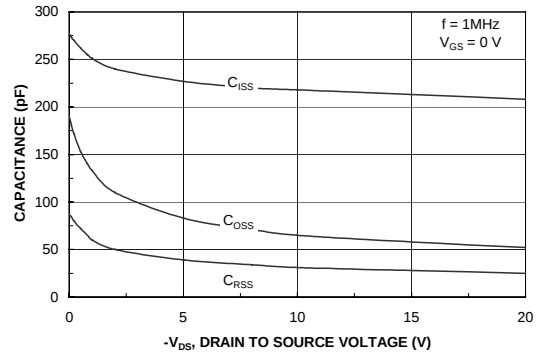


Figure 8. Capacitance Characteristics.

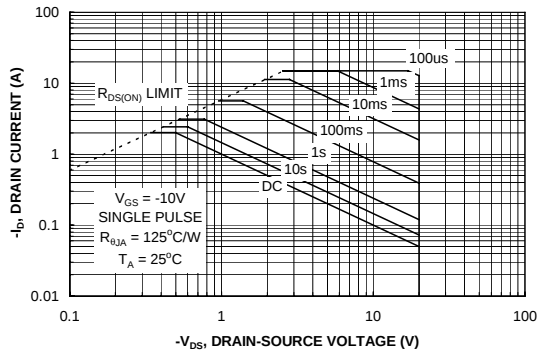


Figure 9. Maximum Safe Operating Area.

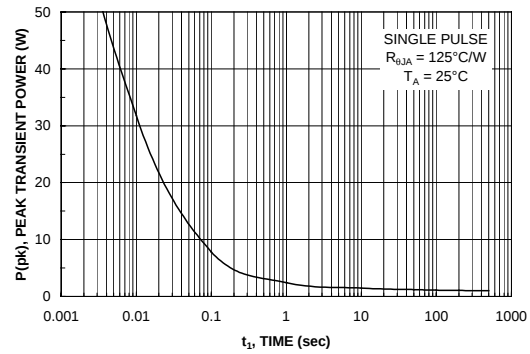


Figure 10. Single Pulse Maximum Power Dissipation.

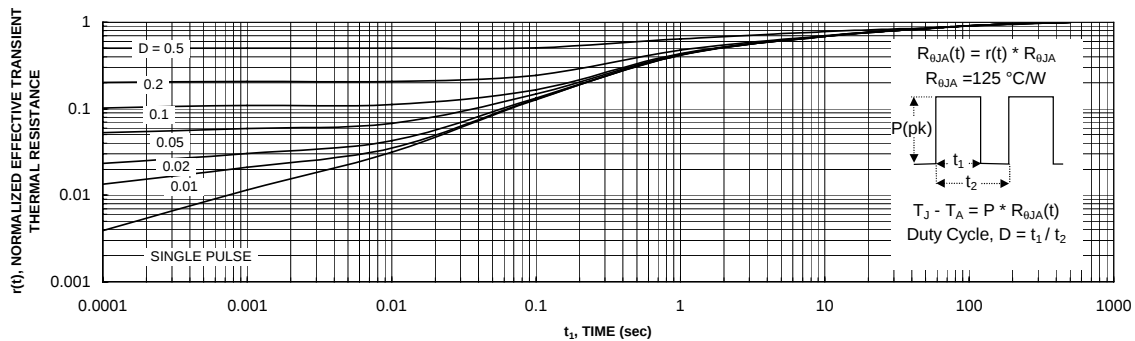


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE ^{Ex} TM	FAST [®]	OPTOLOGIC TM	SMART START TM	VCX TM
Bottomless TM	FAST ^r TM	OPTOPLANAR TM	STAR*POWER TM	
CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POP TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.