

SSW10N60B / SSI10N60B

600V N-Channel MOSFET

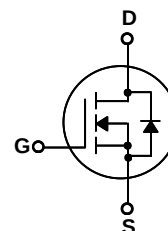
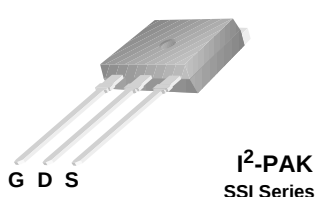
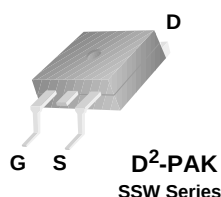
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Features

- 9.0A, 600V, $R_{DS(on)} = 0.8\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 54 nC)
- Low C_{rss} (typical 32 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SSW10N60B / SSI10N60B	Units
V_{DSS}	Drain-Source Voltage	600	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	9.0	A
	- Continuous ($T_C = 100^\circ\text{C}$)	5.7	A
I_{DM}	Drain Current - Pulsed (Note 1)	36	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	520	mJ
I_{AR}	Avalanche Current (Note 1)	9.0	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	15.6	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.13	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	156	W
	- Derate above 25°C	1.25	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.8	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C/W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.65	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$	--	0.65	0.8	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 4.5\text{ A}$ (Note 4)	--	10.3	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2100	2700	pF
C_{oss}	Output Capacitance		--	175	230	pF
C_{rss}	Reverse Transfer Capacitance		--	32	42	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 10\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	35	80	ns
t_r	Turn-On Rise Time		--	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		--	185	380	ns
t_f	Turn-Off Fall Time		--	115	240	ns
Q_g	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 10\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	54	70	nC
Q_{gs}	Gate-Source Charge		--	9.3	--	nC
Q_{gd}	Gate-Drain Charge		--	21	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	9.0	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	36	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 9.0 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 10 A, dI _F / dt = 100 A/μs (Note 4)	--	470	--	ns
Q _{rr}	Reverse Recovery Charge		--	6.25	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 11.8\text{ mH}, I_{AS} = 9.0\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 10\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

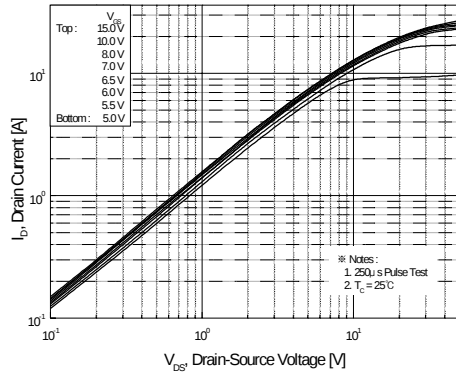


Figure 1. On-Region Characteristics

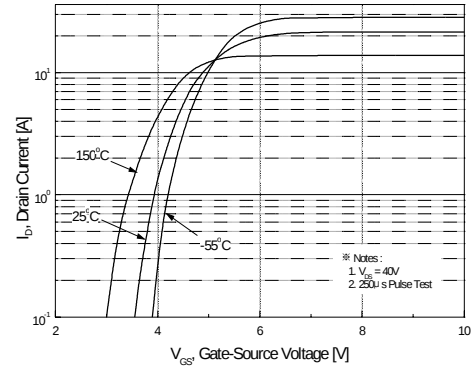


Figure 2. Transfer Characteristics

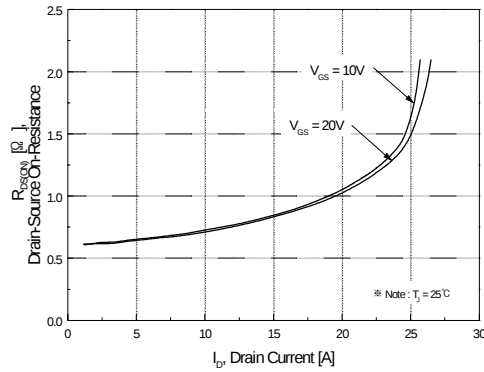


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

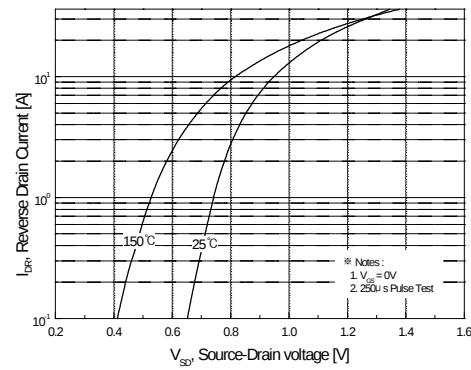


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

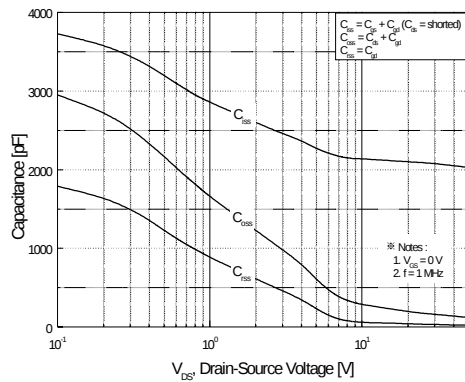


Figure 5. Capacitance Characteristics

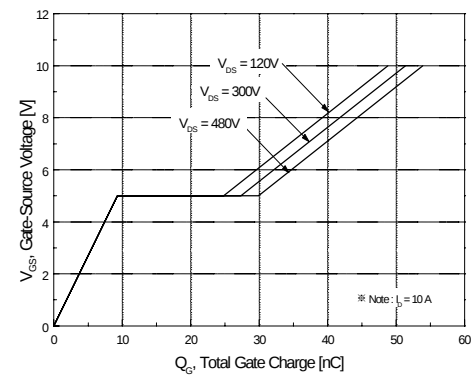


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

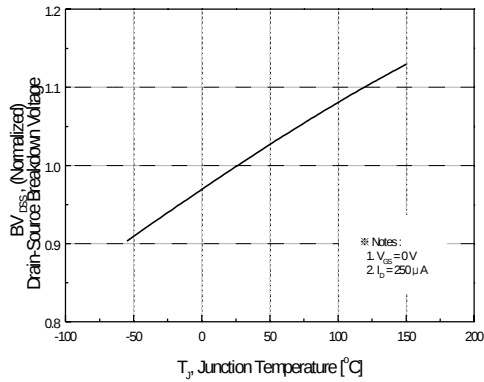


Figure 7. Breakdown Voltage Variation vs Temperature

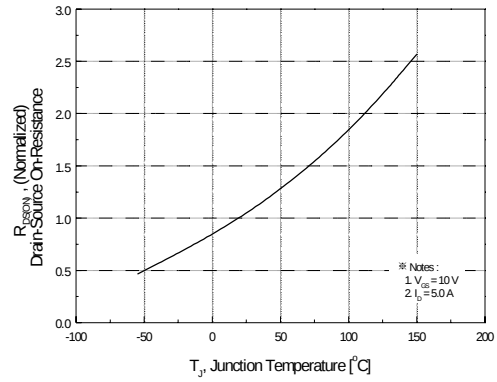


Figure 8. On-Resistance Variation vs Temperature

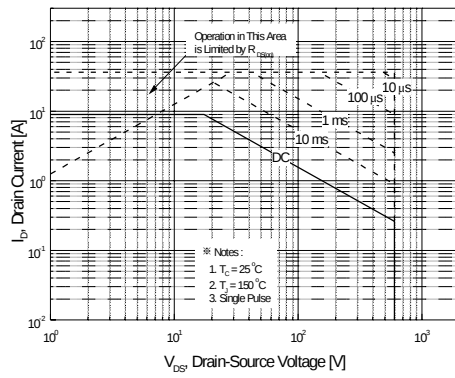


Figure 9. Maximum Safe Operating Area

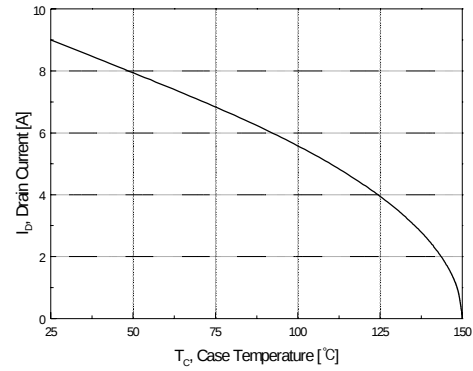


Figure 10. Maximum Drain Current vs Case Temperature

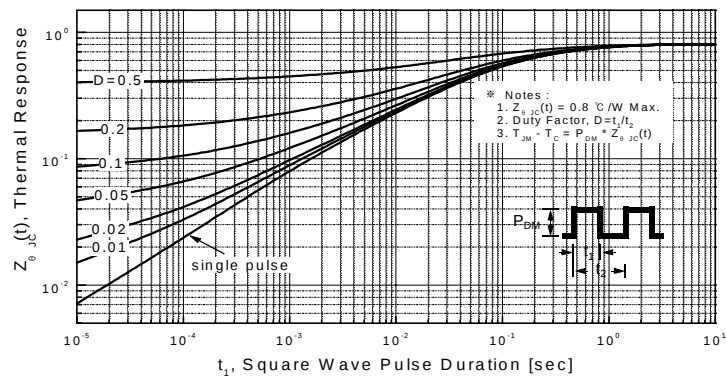
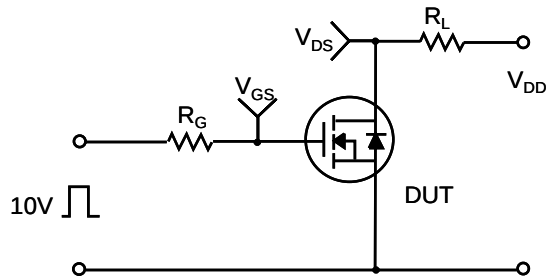


Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform



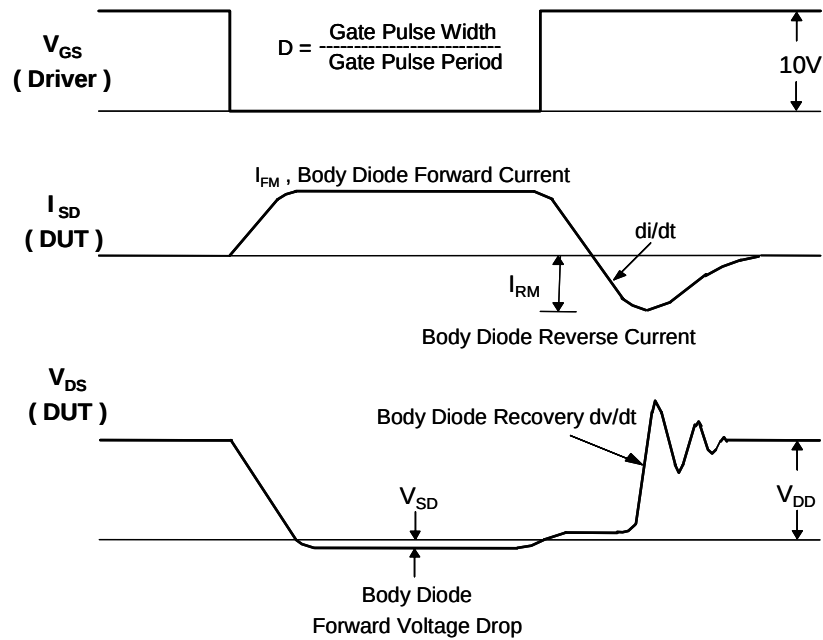
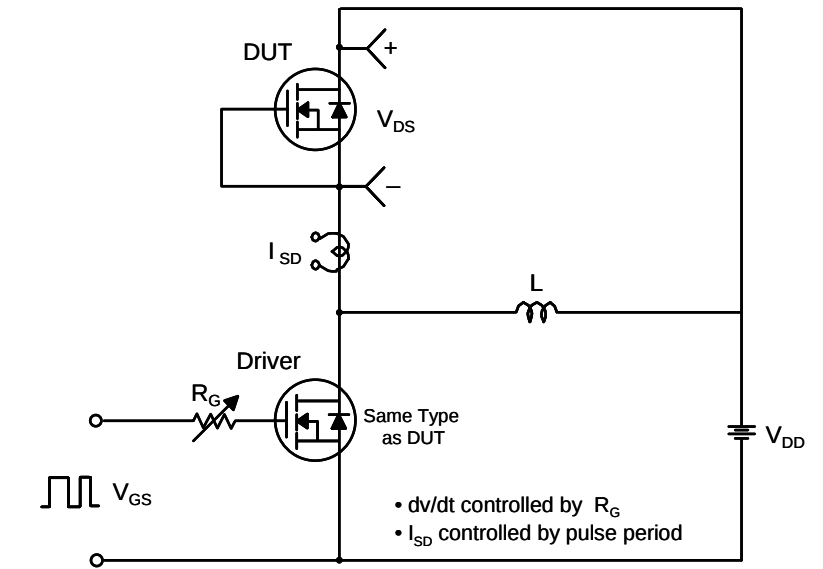
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



SSW10N60B / SSI10N60B

Technical drawing of a 10-pin D-sub connector showing front, side, and top views with dimensions in millimeters (mm) and inches (in).

Front View (Top Left):

- Overall Width: 9.90 ± 0.20 mm (0.40 in)
- Overall Height: 15.30 ± 0.30 mm
- Pin Height (from base): 4.90 ± 0.20 mm
- Pin Spacing (Typical): 2.54 mm (0.10 in)
- Pin Diameter: 0.80 ± 0.10 mm
- Pin Length (from base): 1.27 ± 0.10 mm
- Top Flange Height: 1.40 ± 0.20 mm (0.05 in)
- Internal Pin Spacing: 1.20 ± 0.20 mm

Side View (Top Right):

- Overall Width: 4.50 ± 0.20 mm
- Pin Height (from base): 2.00 ± 0.10 mm
- Pin Spacing (Typical): 2.54 ± 0.30 mm
- Pin Diameter: 0.50 ± 0.10 mm
- Pin Length (from base): 0.75 mm (0.03 in)
- Top Flange Height: 1.30 ± 0.10 mm
- Internal Pin Spacing: 0.10 ± 0.15 mm
- Pin Angle: $0^\circ - 3^\circ$

Top View (Bottom Left):

- Overall Width: 10.00 ± 0.20 mm

Bottom View (Bottom Right):

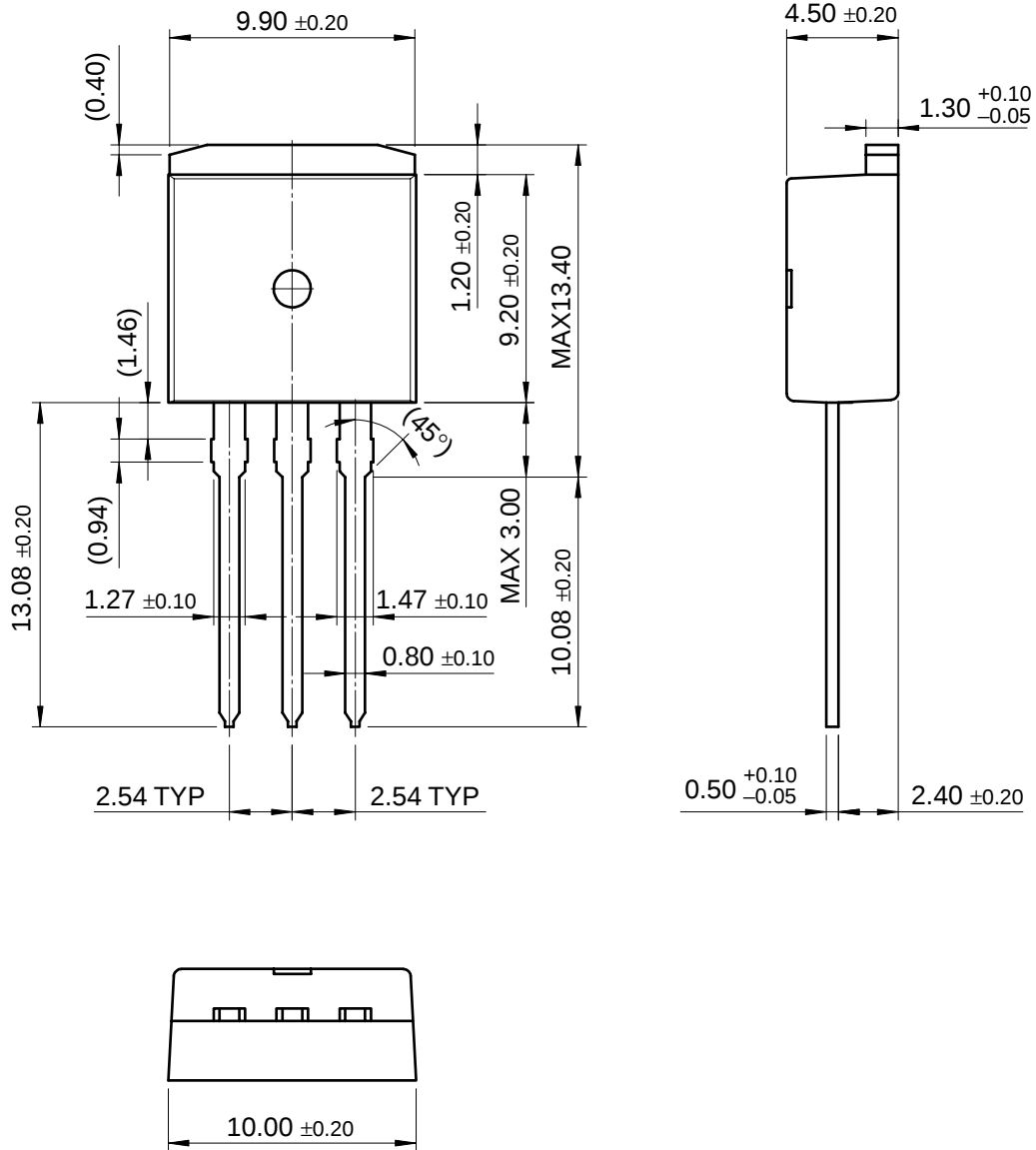
- Overall Width: 10.00 ± 0.20 mm
- Overall Height: 15.30 ± 0.30 mm
- Pin Height (from base): 4.90 ± 0.20 mm
- Pin Spacing (Typical): 2.54 mm (0.10 in)
- Pin Diameter: 0.80 ± 0.10 mm
- Pin Length (from base): 1.27 ± 0.10 mm
- Top Flange Height: 1.40 ± 0.20 mm (0.05 in)
- Internal Pin Spacing: 1.20 ± 0.20 mm
- Top Flange Width: 8.00 mm (0.31 in)
- Top Flange Radius: $(2 \times R0.45)$
- Top Flange Thickness: 0.72 mm (0.03 in)
- Top Flange Height: 7.20 mm (0.28 in)
- Top Flange Width (from center): 4.40 mm (0.17 in)
- Top Flange Height (from center): 1.75 mm (0.07 in)

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Package Dimensions (Continued)

I²-PAK



Dimensions in Millimeters

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