

SSP2N60B/SSS2N60B

600V N-Channel MOSFET

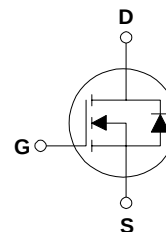
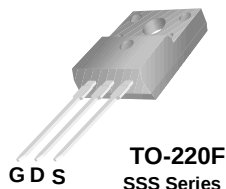
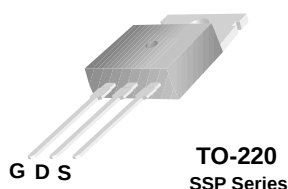
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Features

- 2.0A, 600V, $R_{DS(on)} = 5.0\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 12.5 nC)
- Low C_{rss} (typical 7.6 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SSP2N60B	SSS2N60B	Units
V_{DSS}	Drain-Source Voltage	600		V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	2.0	2.0 *	A
	- Continuous ($T_C = 100^\circ\text{C}$)	1.3	1.3 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	6.0	6.0 *	A
V_{GSS}	Gate-Source Voltage	± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	120		mJ
I_{AR}	Avalanche Current (Note 1)	2.0		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	5.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	54	23	W
	- Derate above 25°C	0.43	0.18	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SSP2N60B	SSS2N60B	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case Max.	2.32	5.5	$^\circ\text{C/W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Max.	62.5	62.5	$^\circ\text{C/W}$

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.65	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.0\text{ A}$	--	3.8	5.0	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 1.0\text{ A}$ (Note 4)	--	2.05	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	380	490	pF
C_{oss}	Output Capacitance		--	35	46	pF
C_{rss}	Reverse Transfer Capacitance		--	7.6	9.9	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 2.0\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	16	40	ns
t_r	Turn-On Rise Time		--	50	110	ns
$t_{d(off)}$	Turn-Off Delay Time		--	40	90	ns
t_f	Turn-Off Fall Time		--	40	90	ns
Q_g	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 2.0\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	12.5	17	nC
Q_{gs}	Gate-Source Charge		--	2.2	--	nC
Q_{gd}	Gate-Drain Charge		--	5.4	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2.0	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	6.0	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.0 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 2.0 A, dI _F / dt = 100 A/μs (Note 4)	--	250	--	ns
Q _{rr}	Reverse Recovery Charge		--	1.31	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 55\text{ mH}, I_{AS} = 2.0\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 2.0\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

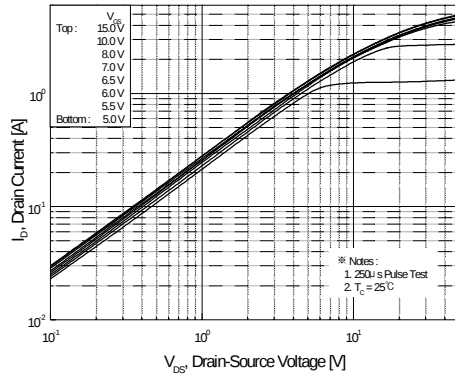


Figure 1. On-Region Characteristics

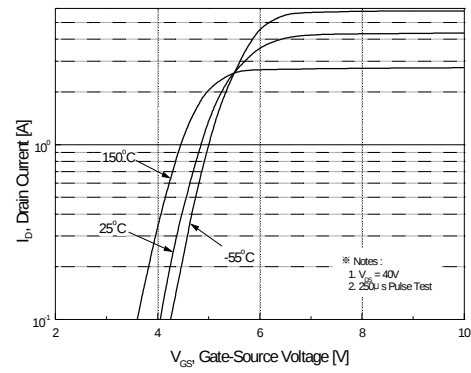


Figure 2. Transfer Characteristics

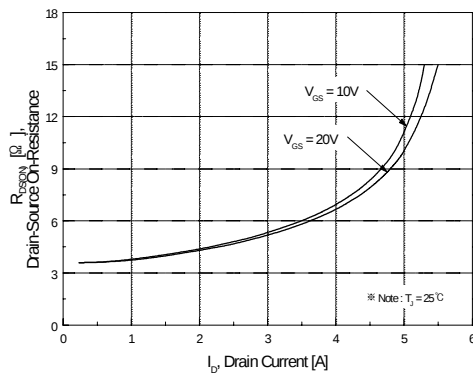


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

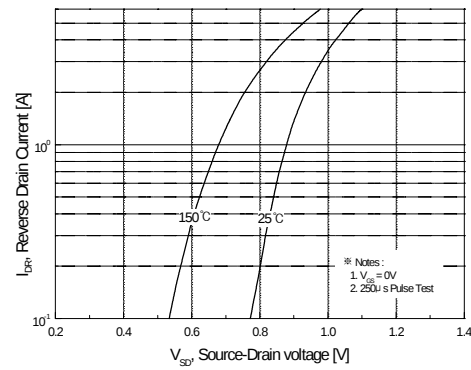


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

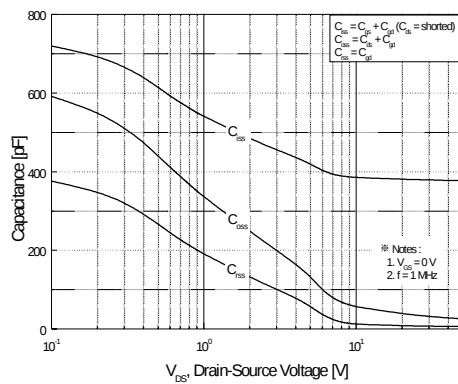


Figure 5. Capacitance Characteristics

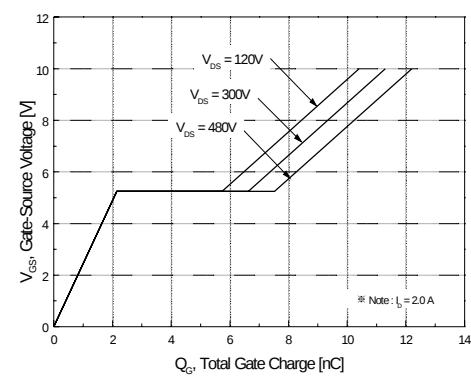


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

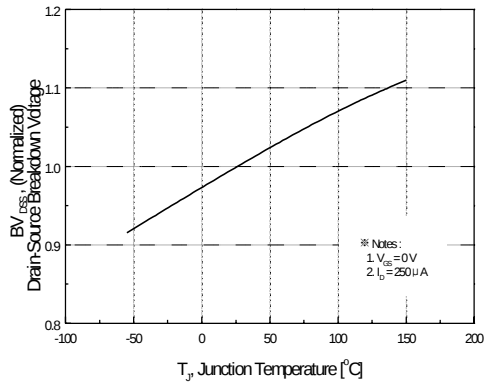


Figure 7. Breakdown Voltage Variation vs Temperature

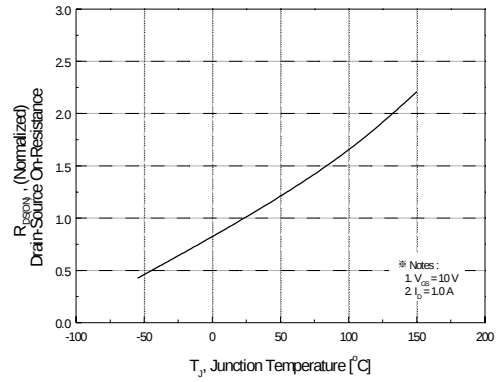


Figure 8. On-Resistance Variation vs Temperature

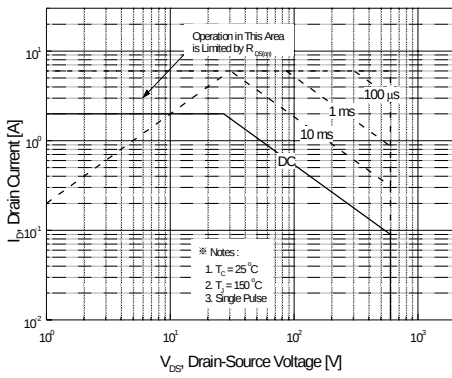


Figure 9-1. Maximum Safe Operating Area for SSP2N60B

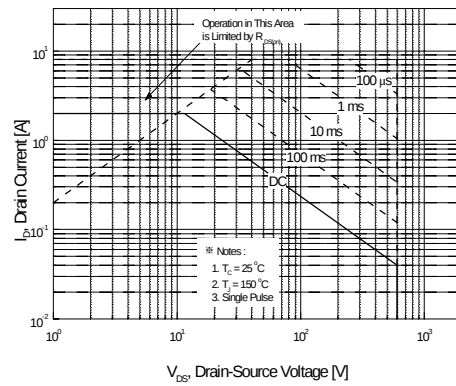


Figure 9-2. Maximum Safe Operating Area for SSS2N60B

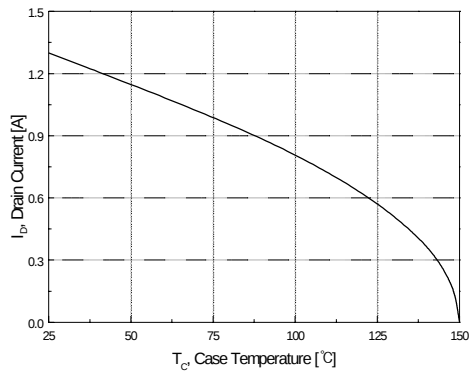


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

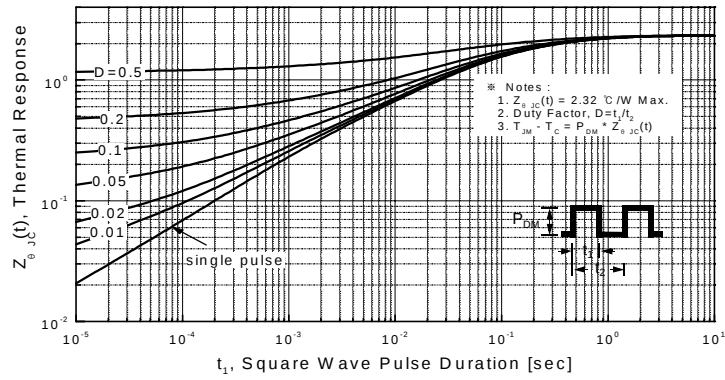


Figure 11-1. Transient Thermal Response Curve for SSP2N60B

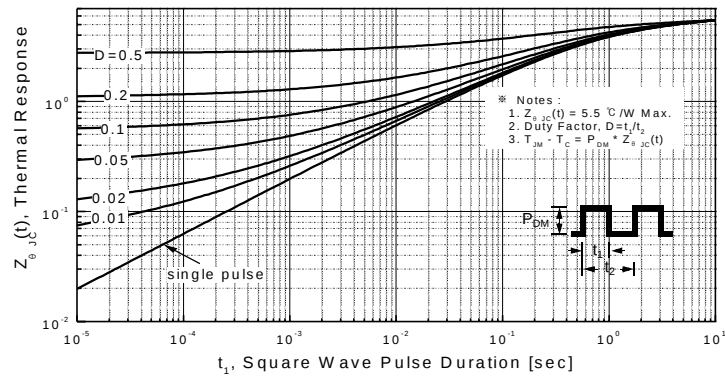
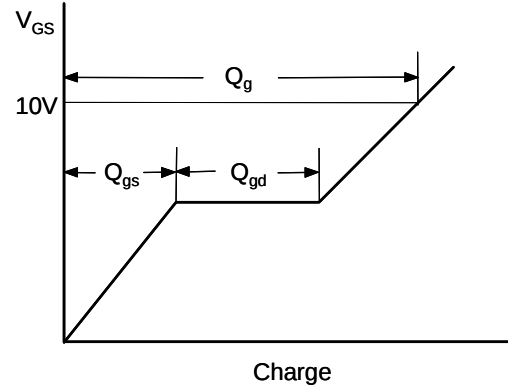
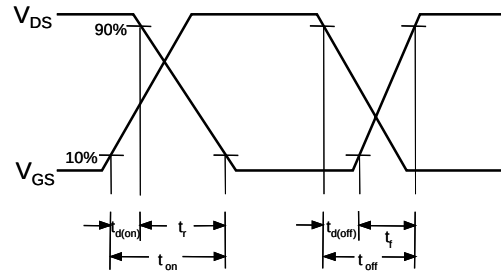
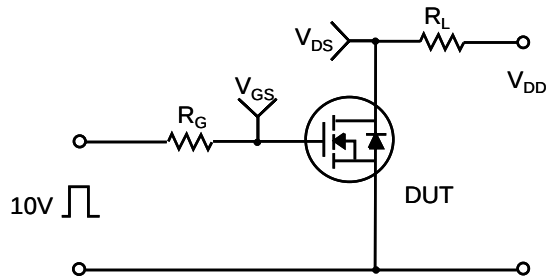


Figure 11-2. Transient Thermal Response Curve for SSS2N60B

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



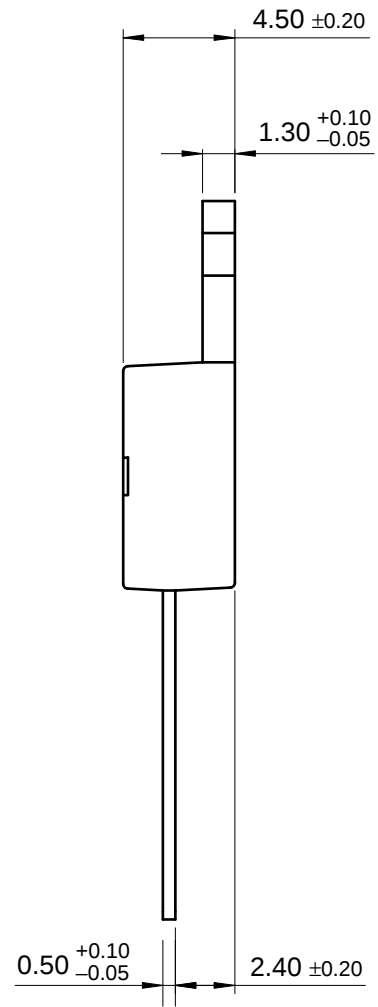
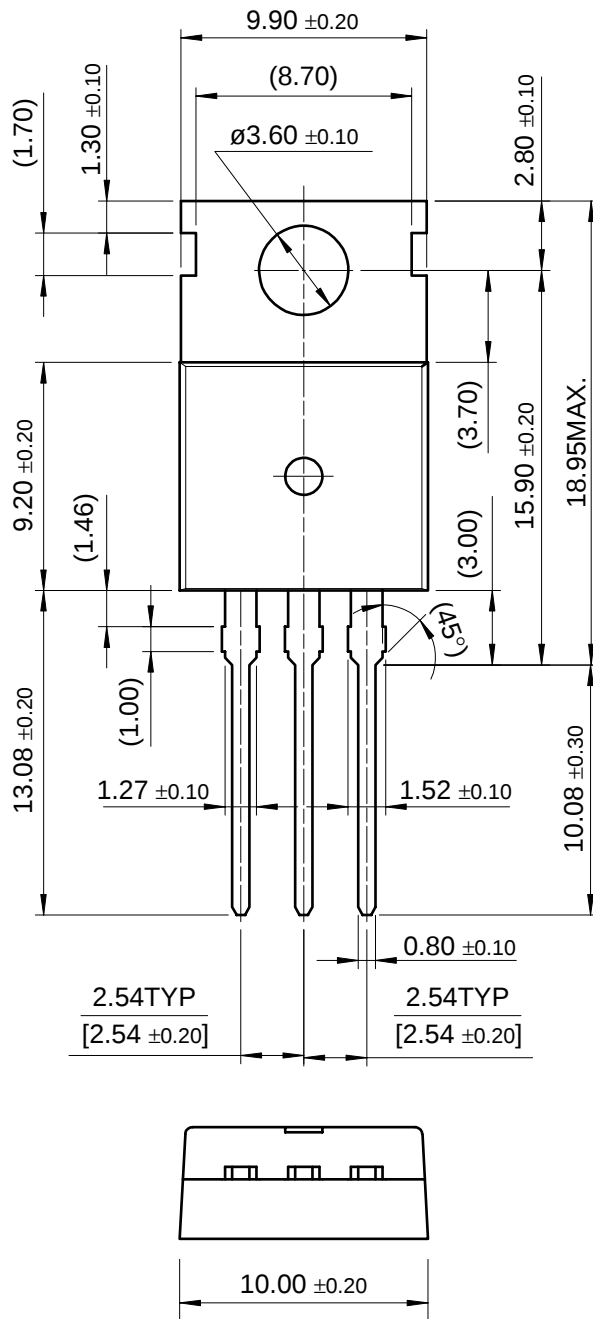
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

Package Dimensions

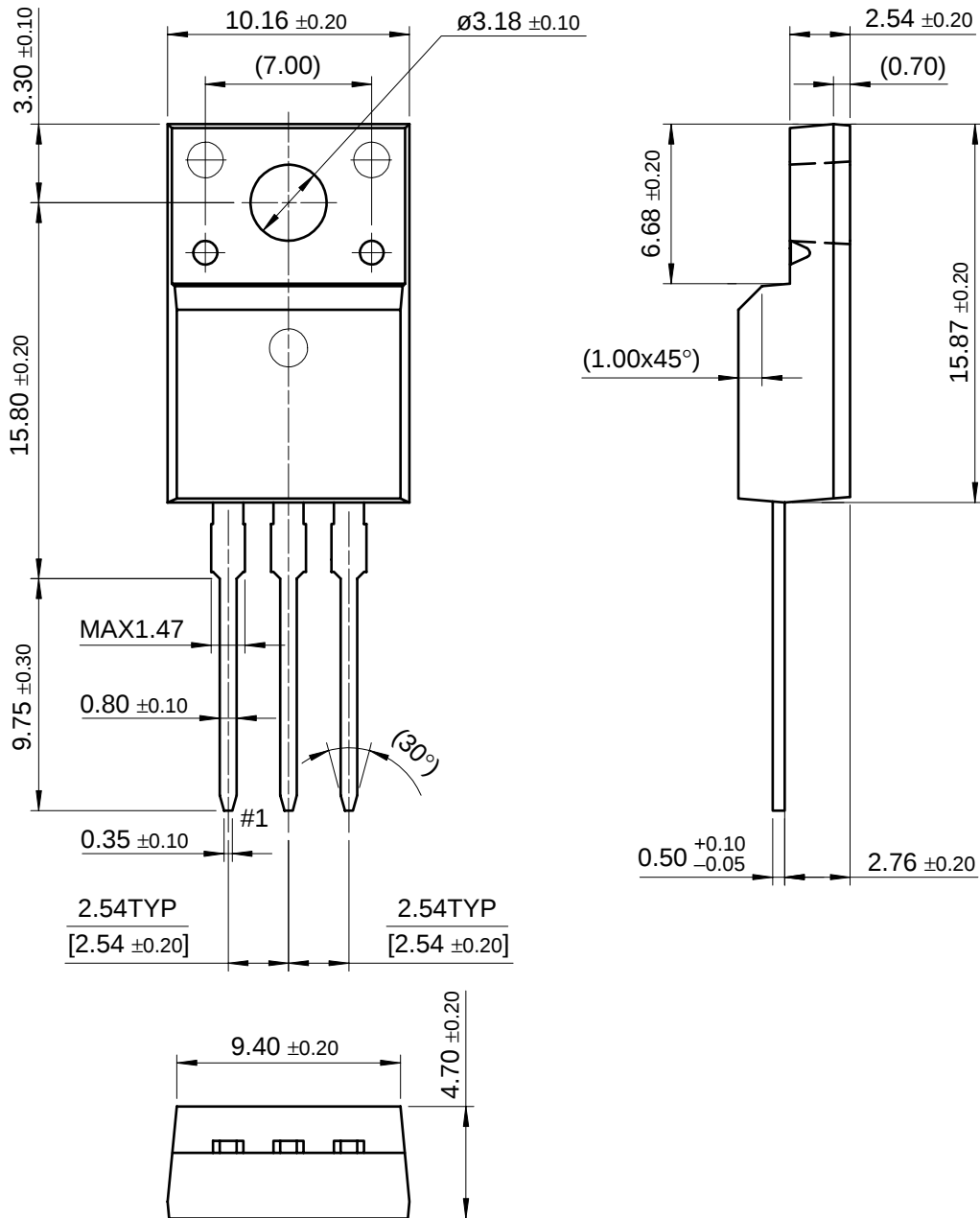
TO-220



SSP2N60B/SSS2N60B

Dimensions in Millimeters

TO-220F



Dimensions in Millimeters

SSP2N60B/SSS2N60B

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