FAIRCHILD SEMICONDUCTOR™

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SSTV16857
14-Bit Register with SSTL-2 Compatible I/O and Reset

General Description

The SSTV16857 is a 14-bit register designed for use with 184 and 232 pin DDR-I memory modules. The device has a differential input clock, SSTL-2 compatible data inputs and a LVCMOS compatible $\overline{\text{RESET}}$ input. The device has been designed for compliance with the JEDEC DDR module and register specifications.

The device is fabricated on an advanced submicron CMOS process and is designed to operate at power supplies of less than 3.6V's.

Features

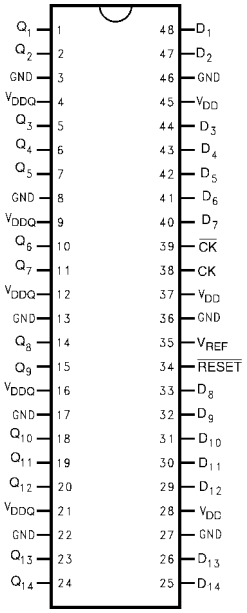
- Compliant with DDR-I registered module specifications
- Operates at 2.5V ± 0.2V V_{DD}
- SSTL-2 compatible input and output structure
- Differential SSTL-2 compatible clock inputs
- Low power mode when device is reset
- Industry standard 48 pin TSSOP package

Ordering Code:

Order Number	Package Number	Package Description
SSTV16857MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Name	Description
Q_1-Q_{14}	SSTL-2 Compatible Output
D_1-D_{14}	SSTL-2 Compatible Inputs
$\overline{\text{RESET}}$	Asynchronous LVCMOS Reset Input
CK	Positive Master Clock Input
$\overline{\text{CK}}$	Negative Master Clock Input
V_{REF}	Voltage Reference Pin for SSTL Level Inputs
V_{DDQ}	Power Supply Voltage for Output Signals
V_{DD}	Power Supply Voltage for Inputs

Truth Table

$\overline{\text{RESET}}$	D_n	CK	$\overline{\text{CK}}$	Q_n
L	X or Floating	X or Floating	X or Floating	L
H	L	↑	↓	L
H	H	↑	↓	H
H	X	L	H	Q_n
H	X	H	L	Q_n

L = Logic LOW
H = Logic HIGH
X = Don't Care, but not floating unless noted
↑ = LOW-to-HIGH Clock Transition
↓ = HIGH-to-LOW Clock Transition

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Functional Description

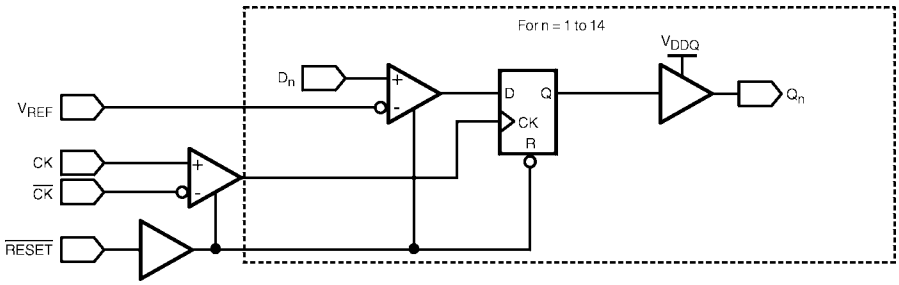
The SSTV16857 is a 14-bit register with SSTL-2 compatible inputs and outputs. Input data is captured by the register on the positive edge crossing of the differential clock pair.

When the LV-CMOS $\overline{\text{RESET}}$ signal is asserted LOW, all outputs and internal registers are asynchronously placed into the LOW logic state. In addition, the clock and data differential comparators are disabled for power savings. Output glitches are prevented by disabling the internal registers more quickly than the input comparators. When $\overline{\text{RESET}}$ is removed, the system designer must insure the clock and data inputs to the device are stable during the rising transition of the $\overline{\text{RESET}}$ signal.

The SSTL-2 data inputs transition based on the value of V_{REF}. V_{REF} is a stable system reference used for setting the trip point of the input buffers of the SSTV16857 and other SSTL-2 compatible devices.

The $\overline{\text{RESET}}$ signal is a standard CMOS compatible input and is not referenced to the V_{REF} signal.

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{DDQ})	−0.5V to +3.6V
Supply Voltage (V_{DD})	−0.5V to +3.6V
Reference Voltage (V_{REF})	−0.5V to +3.6V
Input Voltage (V_I)	−0.5V to V_{DD} + 0.5V
Output Voltage (V_O)	
Outputs Active (Note 2)	−0.5V to V_{DDQ} + 0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
V_I > V_{DD}	+50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
V_O > V_{DD}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{DD} or Ground Current per Supply Pin (I_{DD} or Ground)	±100 mA
Storage Temperature Range (T_{stg})	−65°C to +150°C

Recommended Operating Conditions (Note 3)

Power Supply (V_{DDQ})	2.3V to 2.7V
Power Supply (V_{DD})	
Operating Range	V_{DDQ} to 2.7V
Reference Supply (V_{REF} = V_{DDQ}/2)	1.15 to 1.35
Termination Voltage (V_{TT})	V_{REF} ± 40 mV
Input Voltage	0V to V_{DD}
Output Voltage (V_O)	
Output in Active States	0V to V_{DDQ}
Output Current I_{OH}/I_{OL}	
V_{DD} = 2.3V to 2.7V	±20 mA
Free Air Operating Temperature (T_A)	0°C to +70°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: IO Absolute Maximum Rating must be observed.

Note 3: The $\overline{\text{RESET}}$ input of the device must be held at V_{DD} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is asserted LOW.

DC Electrical Characteristics ($2.3V \le V_{DD} \le 2.7V$)

Symbol	Parameter	Conditions	V_{DD} (V)	Min	Max	Units
V_{IKL}	Input LOW Clamp Voltage	I_I = −18 mA	2.3		−1.2	V
V_{IKH}	Input HIGH Clamp Voltage	I_I = +18 mA	2.3		3.5	V
V_{IH-AC}	AC HIGH Level Input Voltage	Data Inputs		V_{REF}+310mV		V
V_{IL-AC}	AC LOW Level Input Voltage	Data Inputs			V_{REF}−310mV	V
V_{IH-DC}	DC HIGH Level Input Voltage	Data Inputs		V_{REF}+150mV		V
V_{IL-DC}	DC LOW Level Input Voltage	Data Inputs			V_{REF}−150mV	V
V_{IH}	HIGH Level Input Voltage	$\overline{\text{RESET}}$		1.7		V
V_{IL}	LOW Level Input Voltage	$\overline{\text{RESET}}$			0.7	V
V_{ICR}	Common Mode Input Voltage Range	CLK, $\overline{\text{CLK}}$		0.97	1.53	V
$V_{I(PP)}$	Peak to Peak Input Voltage	CLK, $\overline{\text{CLK}}$		360		mV
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA I_{OH} = −16 mA	2.3 to 2.7 2.3	V_{DD} − 0.2 1.95		V
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA I_{OL} = 16 mA	2.3 to 2.7 2.3		0.2 0.35	V
I_I	Input Leakage Current	V_I = V_{DD} or GND	2.7		±5.0	µA
I_{DD}	Static Standby	$\overline{\text{RESET}}$ = GND, I_O = 0	2.7		10	µA
	Static Operating	$\overline{\text{RESET}}$ = V_{DD}, I_O = 0 V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$			25	mA
I_{DDD}	Dynamic Operating Current Clock Only	$\overline{\text{RESET}}$ = V_{DD}, I_O = 0 V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$ CK, $\overline{\text{CK}}$ Duty Cycle 50%	2.7		90	µA/MHz
	Dynamic Operating Current per Data Input	$\overline{\text{RESET}}$ = V_{DD}, I_O = 0 V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$ CK, $\overline{\text{CK}}$ Duty Cycle 50% Data Input = ½ Clock Rate 50% Duty Cycle			15	µA/MHz

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{DD} (V)	Min	Max	Units
R_{OH}	Output HIGH On Resistance	I_{OH} = −20 mA	2.3 to 2.7	7	20	Ω
R_{OL}	Output LOW On Resistance	I_{OL} = 20 mA	2.3 to 2.7	7	20	Ω
$R_{O\Delta}$	$\lvert R_{OH} - R_{OL} \rvert$	I_O = 20 mA, T_A = 25°C	2.5		4	Ω

AC Electrical Characteristics (Note 4)

Symbol	Parameter	T_A = 0°C to +70°C, C_L = 30 pF, R_L = 50Ω; V_{DD} = 2.5V ± 0.2V; V_{DDQ} = 2.5V ± 0.2V		Units
		Min	Max	
f_{MAX}	Maximum Clock Frequency	200		MHz
t_W	Pulse Duration, CK, $\overline{CK}$ HIGH or LOW (Figure 2)	2.5		ns
t_{ACT} (Note 5)	Differential Inputs Activation Time, data inputs must be LOW after $\overline{RESET}$ HIGH (Figure 3)	22		ns
t_{INACT} (Note 5)	Differential Inputs De-activation Time, data and clock inputs must be held at valid levels (not floating) after $\overline{RESET}$ LOW	22		ns
t_S	Setup Time, Fast Slew Rate (Note 6)(Note 7) (Figure 5)	0.75		ns
	Setup Time, Slow Slew Rate (Note 7)(Note 8) (Figure 5)	0.9		
t_H	Hold Time, Fast Slew Rate (Note 6)(Note 8) (Figure 5)	0.75		ns
	Hold Time, Slow Slew Rate (Note 7)(Note 8) (Figure 5)	0.9		
t_{REM}	Reset Removal Time (Figure 7)	10		ns
t_{PHL}, t_{PLH}	Propagation Delay CLK, CLK to Q_n (Figure 4)	1.1	2.8	ns
t_{PHL}	Propagation Delay $\overline{RESET}$ to Q_n (Figure 6)		5.0	ns
$t_{SK(Pn-Pn)}$	Output to Output Skew		200	ps

Note 4: Refer to Figure 1 through Figure 7.

Note 5: This parameter is not production tested.

Note 6: For data signal input slew rate ≥ 1 V/ns.

Note 7: For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.

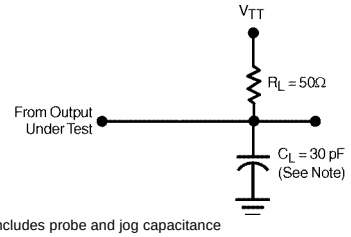
Note 8: For CK, $\overline{CK}$ signals input slew rates are ≥ 1 V/ns.

Capacitance (Note 9)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Data Pin Input Capacitance	2.0		3.0	pF	V_{DD} = 2.5V, $V_I = V_{REF} \pm 350$ mV
	CK, $\overline{CK}$ - Input Capacitance	2.5		3.5	pF	V_{DD} = 2.5V, V_{ICR} = 1.25V, $V_{I(PP)}$ = 360 mV
	$\overline{RESET}$	2.5		3.5	pF	V_{DD} = 2.5V, $V_I = V_{DD}$ to GND

Note 9: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms (See Notes A through F below)



Note: C_L includes probe and jog capacitance

FIGURE 1. AC Test Circuit

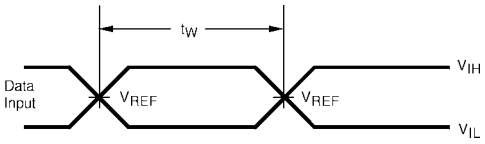
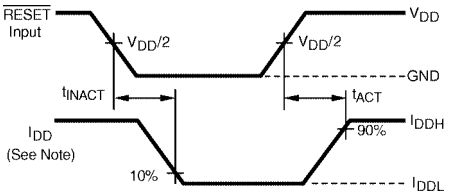


FIGURE 2. Voltage Waveforms - Pulse Duration



Note: I_{DD} tested with clock and data inputs held at V_{DD} or GND, and $I_O = 0$ mA.

FIGURE 3. Voltage and Current Waveforms Inputs Active and Inactive Times

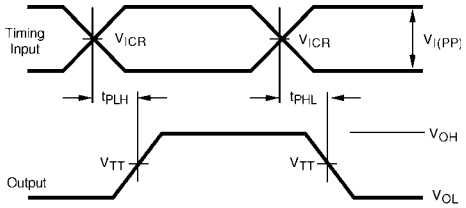


FIGURE 4. Voltage Waveforms - Propagation Delay Times

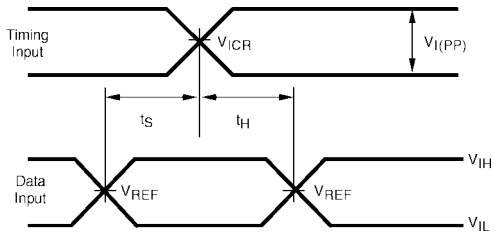


FIGURE 5. Voltage Waveforms - Setup and Hold Times

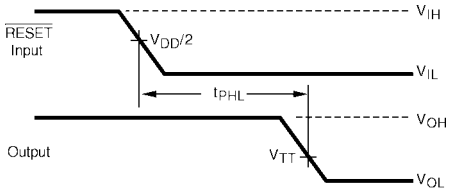


FIGURE 6. Voltage Waveforms - RESET Propagation Delay Times

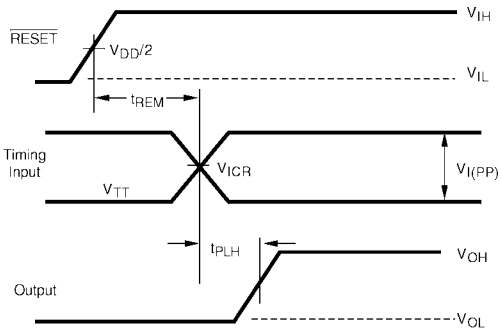


FIGURE 7. Voltage Waveforms - RESET Removal Delay Times

Note A: All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz, $Z_0 = 50\Omega$, input slew rate = 1V/ns ± 20% (unless otherwise specified).

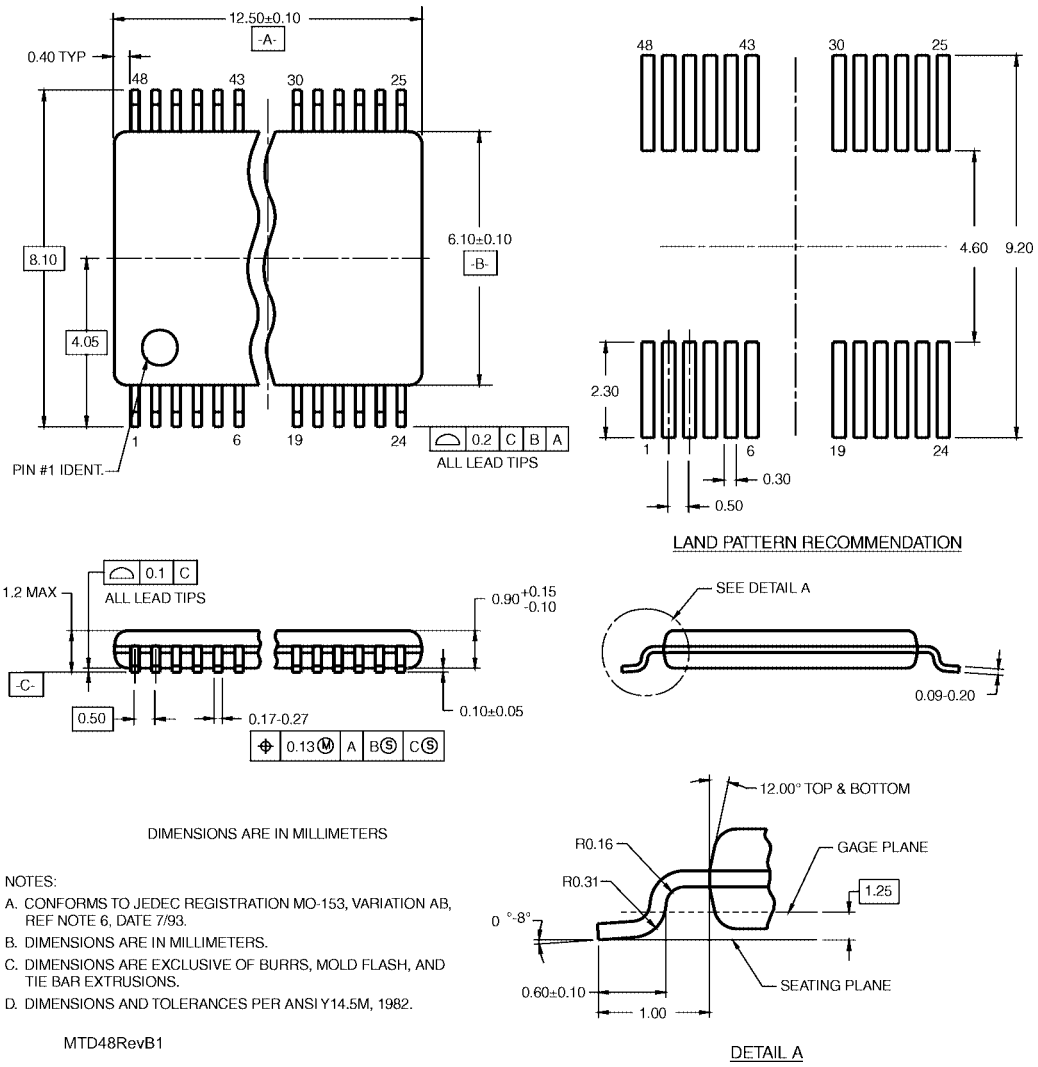
Note B: The outputs are measured one at a time with one transition per measurement.

Note C: $V_{TT} = V_{REF} = V_{DD}/2$.

Note D: $V_{IH} = V_{REF} + 310$ mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

Note E: $V_{IL} = V_{REF} - 310$ mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

Note F: Removal time (t_{REM}) is tested with one data input held active HIGH. The propagation time from CK to the corresponding output must meet valid timing specifications for the measurement to be accurate.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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