USB Downstream Port Terminator with VBUS ESD Protection

Features

- A low-capacitance USB downstream port terminator, EMI filter, and transient over-voltage protector in a single surface-mounted package
- ESD protection to ±20kV contact discharge, per MIL-STD-883D, Method 3015
- ESD protection to ±15kV contact discharge, per IEC 61000-4-2 International Standard
- Provides ESD protection for the VBUS line
- Compact SOT23-6 package saves board space and lowers manufacturing costs compared to discrete solutions
- Capacitors matched to a precision exceeding the USB specification
- Lead-free versions available

Applications

- ESD protection and termination of USB downstream ports
- Desktop PCs
- Notebooks
- Set-top boxes
- USB hubs

Product Description

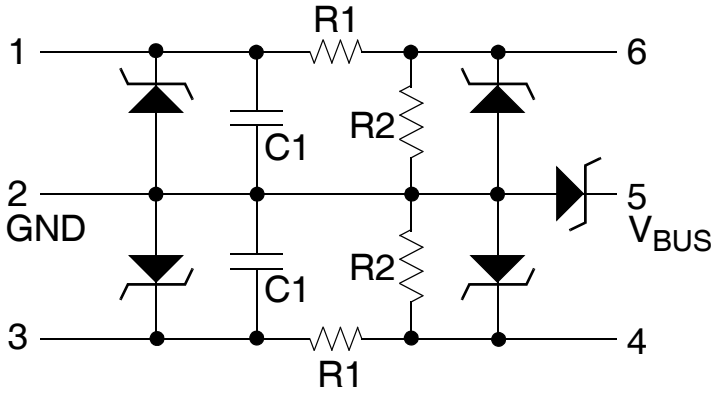
The PACUSBVB-D1/D2/D3 is a single-channel USB downstream-port termination network. It integrates EMI/RFI filter components R1 and C1 as recommended by the USB specification, as well as the required 15kΩ pull-down resistors (R2) to GND. In addition, PACUSBVB-D1/D2/D3 provides a very high level of protection for sensitive electronic components that may be subjected to electrostatic discharge (ESD). The device pins will safely dissipate ESD strikes of ±15kV, exceeding the maximum requirements of the IEC 61000-4-2 international standard. Using the MIL-STD-883D (Method 3015) specification for Human Body Model (HBM) ESD, all pins are protected from contact discharges to ±20kV.

The PACUSBVB-D1/D2/D3 also features a fifth zener diode (cathode at pin 5) which provides ESD protection for the USB VBUS line.

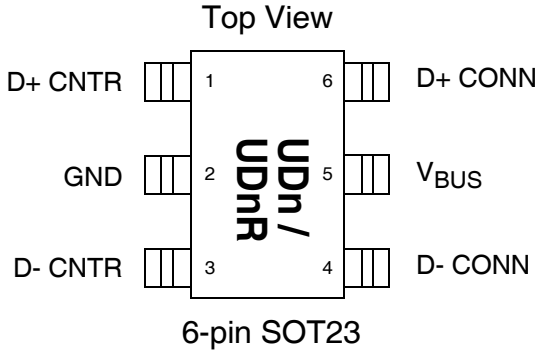
There are three options for the value of the series resistor R1: 15Ω, 33Ω, and 22Ω. This series resistance, plus the USB driver output resistance, must be close to the USB cable's characteristic impedance of 45Ω (each side) to minimize transmission line reflections.

The PACUSBVB-D1/D2/D3 is housed in a 6-pin SOT23 package and is available with optional lead-free finishing.

Electrical Schematic



PACKAGE / PINOUT DIAGRAMS



Note 1: The "n" shown in part markings above represents either the digit "1," "2," or "3."
Note 2: These drawings are not to scale.

PIN DESCRIPTIONS

PINS	NAME	DESCRIPTION
1	D+ CNTR	D+ Data to the USB controller circuitry
2	GND	Ground Pin
3	D- CNTR	D- Data to the USB controller circuitry
4	D- CONN	D- Data to the USB connector
5	V_{BUS}	V_{BUS} input pin
6	D+ CONN	D+ Data to the USB connector

Ordering Information

PART NUMBERING INFORMATION

Pins	R1 Value	Package	Standard Finish		Lead-free Finish	
			Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
6	15 Ω	SOT23-6	PACUSBVB-D2Y6	UD2	PACUSBVB-D2Y6R	UD2R
	22 Ω		PACUSBVB-D3Y6	UD3	PACUSBVB-D3Y6R	UD3R
	33 Ω		PACUSBVB-D1Y6	UD1	PACUSBVB-D1Y6R	UD1R

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
Storage Temperature Range	-65 to +150	°C
Power Dissipation per Resistor	100	mW
Package Power Dissipation	200	mW
Voltage on any pin (DC)	6	V

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
Operating Temperature	-40 to +85	°C
V_{BUS} Input Voltage	5	V

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
R1	Resistance of R1 Resistor (PACUSBVB-D2Y6/Y6R)	T_A = 25°C	12	15	18	Ω
R1	Resistance of R1 Resistor (PACUSBVB-D3Y6/Y6R)	T_A = 25°C	17.6	22	26.4	Ω
R1	Resistance of R1 Resistor (PACUSBVB-D1Y6/Y6R)	T_A = 25°C	26.4	33	39.6	Ω
R2	Resistance of R2 Resistor	T_A = 25°C		15		kΩ
TCR	Temperature Coefficient of Resistance	Note 1		±1300		ppm/°C
C1	Capacitance of C1 Capacitor	0 VDC; 30 mVAC; 1MHz; 25°C	37.6	47	56.4	pF
		2.5 VDC; 30 mVAC; 1MHz; 25°C	25.6	32	38.4	pF
TOL_{CM}	Matching Tolerance of C1 Capacitors	1MHz; 25°C			±2	%
I_{LEAK}	Diode Leakage Current to GND	Measured at 3.3 VDC, 25°C		1	100	nA
V_{RB}	Diode Reverse Bias Voltage	I_{LOAD} = 10μA; T_A = 25°C	5.5			V
V_{SIG}	Signal Voltage: Positive Clamp Negative Clamp	 I_{LOAD} = 10mA; T_A = 25°C I_{LOAD} = 10mA; T_A = 25°C	 5.6 -0.4	 6.8 -0.8	 9.0 -1.5	 V V
V_{ESD}	In-system ESD Withstand Voltage MIL-STD-883D, Method 3015 (HBM) IEC 61000-4-2 Contact Discharge	 Pins 1, 3; Notes 1, 2 and 3 Pins 4, 5; Notes 1 and 2 Pins 4, 5; Notes 1 and 2	 ±4 ±20 ±15			 kV kV kV
V_{CL}	Clamping voltage under ESD discharge	MIL-STD-883D, Method 3015 +8kV; Notes 1 and 4		12		V
		MIL-STD-883D, Method 3015 -8kV; Notes 1 and 4		-7		V

Note 1: Guaranteed by design and characterization.
Note 2: ESD voltage applied to pins with respect to GND, one at a time; unused pins are left open.
Note 3: Pins 1 and 3 are not connected to the USB port connector, and therefore are not exposed to external ESD hazards. Thus, they do not require the high ESD protection levels provided for pins 4, 5, and 6.
Note 4: ESD Clamping Voltage is measured at the opposite end of R1 from the pin to which the ESD discharge is applied (e.g., if ESD is applied to pin 6, then the clamping voltage is measured at pin 1).

Performance Information

Capacitance vs. Voltage

The C1 capacitance value as a function of DC voltage across it is presented in Figure 1. The curve is normalized to a capacitance of 1.0 capacitance units at 2.5 VDC.

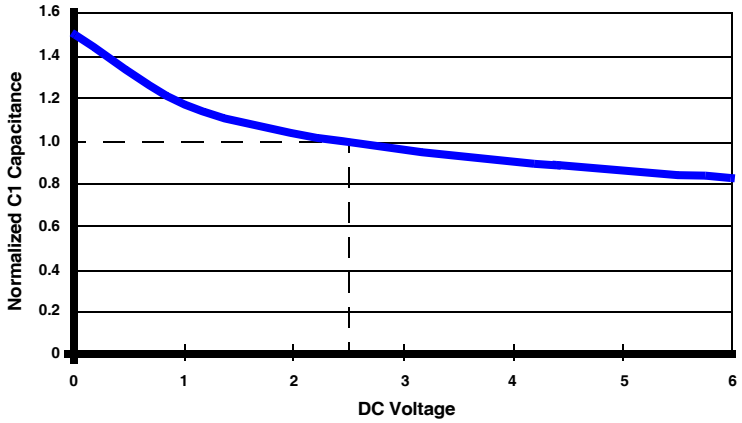


Figure 1. Diode Capacitance vs. DC Voltage (Normalized)

Insertion Loss vs. Frequency Characteristics

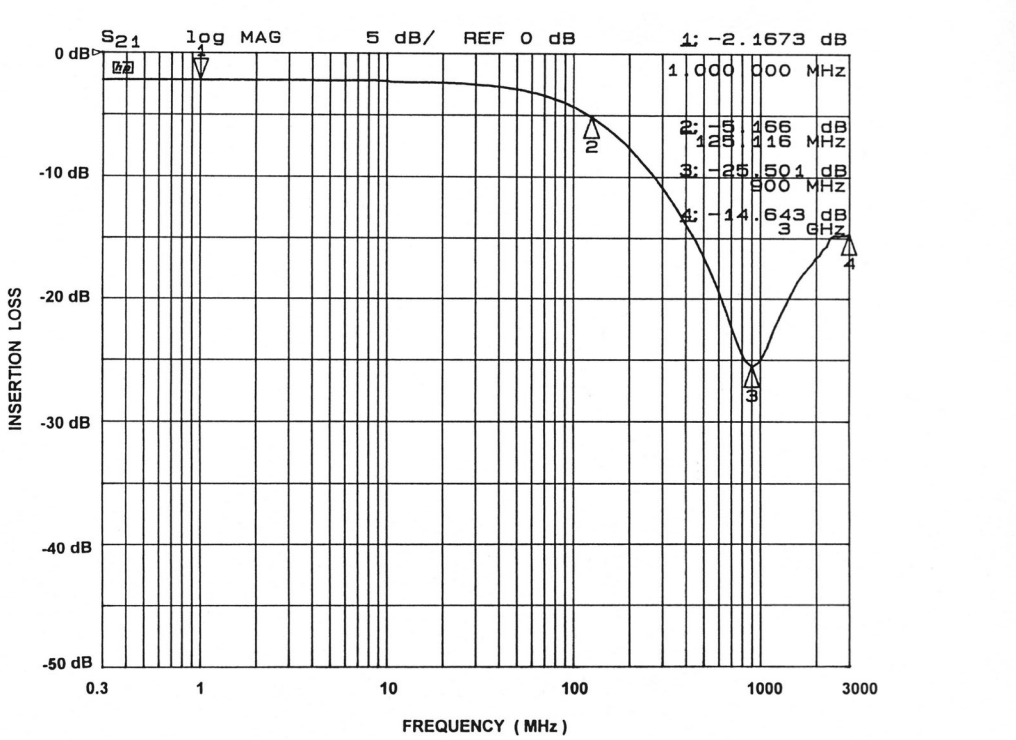


Figure 2. Insertion Loss vs. Frequency Performance Curve, PACUSBVB-D1 (SOT23-6)

Performance Information (cont'd)

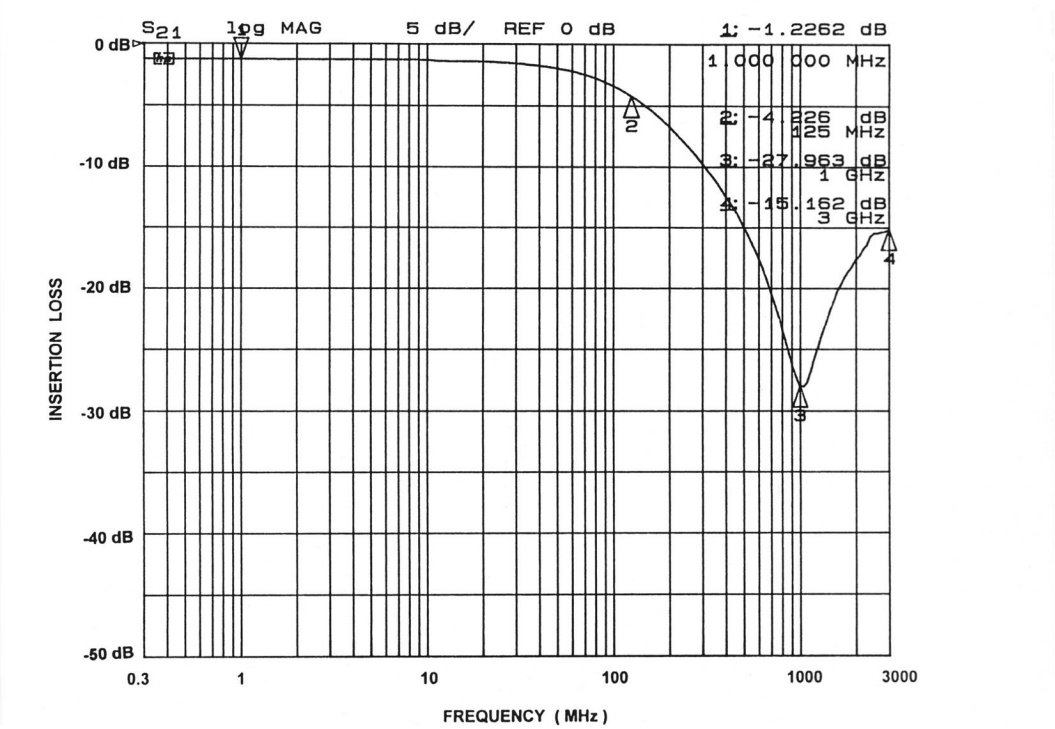


Figure 3. Insertion Loss vs. Frequency Performance Curve, PACUSBVB-D2 (SOT23-6)

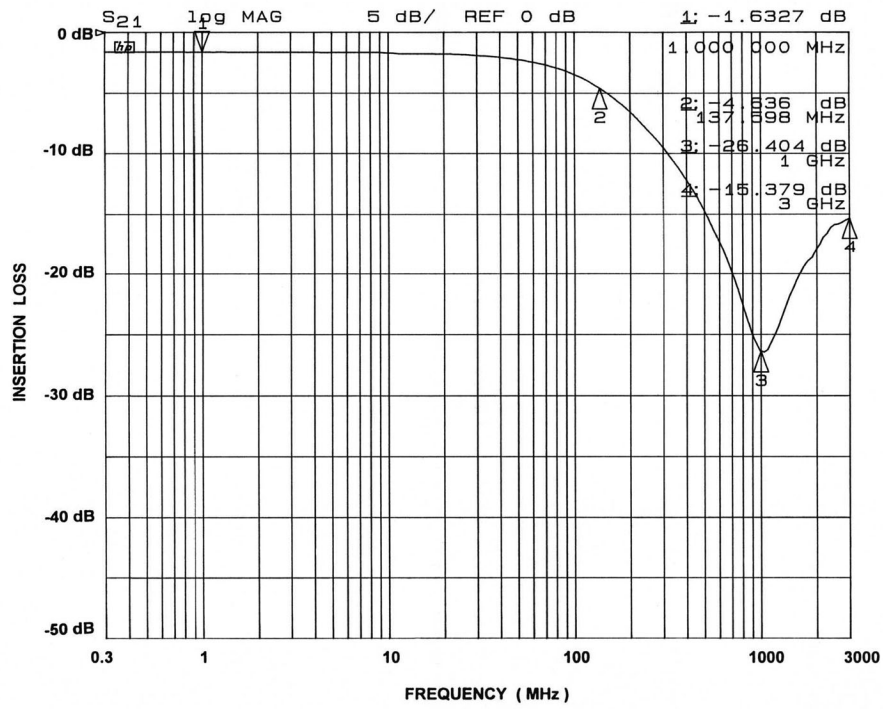


Figure 4. Insertion Loss vs. Frequency Performance Curve, PACUSBVB-D3 (SOT23-6)

Application Information

The PACUSBVB-D1/D2/D3 provides a complete interface for a single downstream USB port typically found in computers and USB hubs. It integrates the series resistors (R1) and the 15kΩ pull-down resistors (R2) for both USB data lines (D+ and D-) as well as the capacitors to ground for EMI suppression. Zener diodes provide ESD protection up to 15kV contact discharge per the IEC 61000-4-2 standard and protect the USB controller on both data lines. The 6-lead PACUSBVB-D1/D2/D3 device provides an additional zener diode to protect the VBUS USB power line.

The PACUSBVB-D1/D2/D3 should be placed on the PCB between the USB controller and the USB connector, as shown on the Connection Diagram Figure 5.

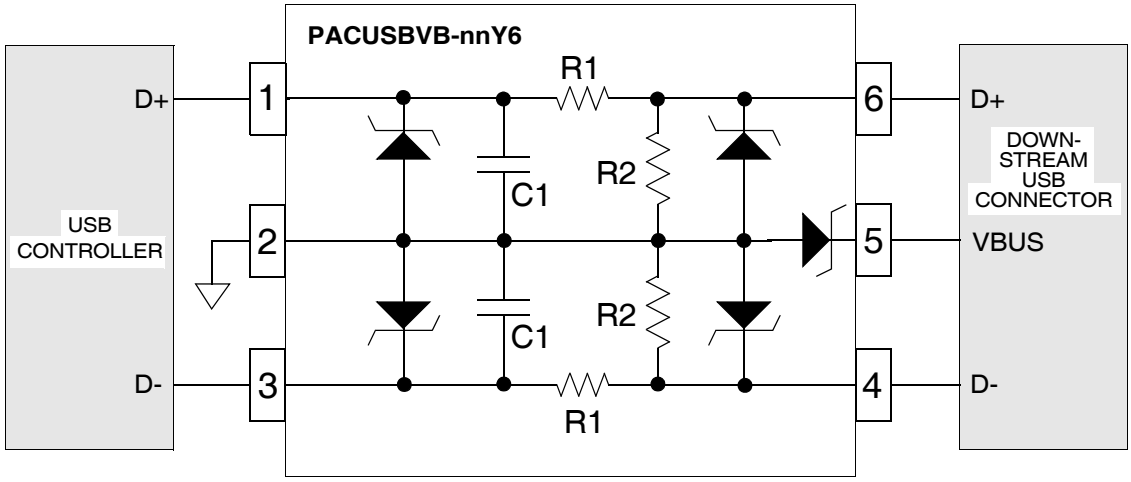


Figure 5. Connection Diagram for PACUSBVB-D1/D2/D3

To guarantee the best ESD and filtering performance, it is recommended that the PACUSBVB-D1/D2/D3 be located close to the USB connector. Also, the trace lengths between the PACUSBVB-D1/D2/D3 and the USB controller should be kept as short as possible.

Mechanical Details

SOT23-6 Mechanical Specifications:

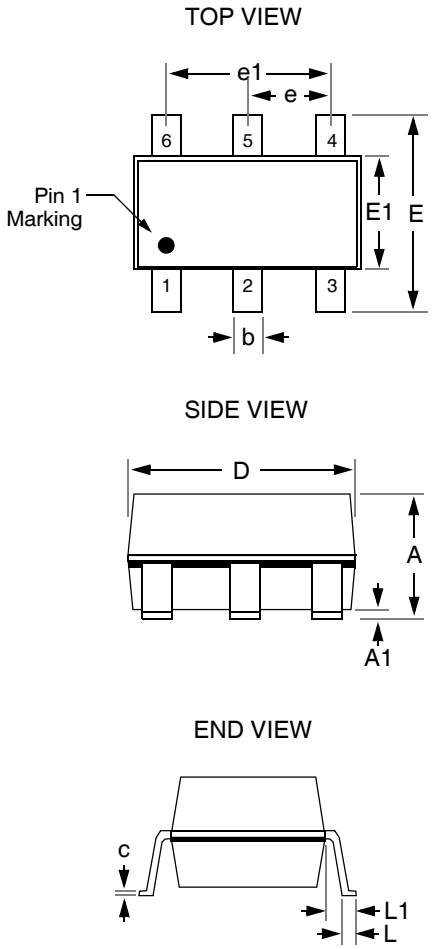
Dimensions for the PACUSBVB-D1/D2/D3 supplied in a 6-pin SOT23 package are presented below.

For complete information on the SOT23-6, see the California Micro Devices SOT23 Package Information document.

PACKAGE DIMENSIONS				
Package	SOT23-6 (JEDEC name is MO-178)			
Pins	6			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	--	1.45	--	0.057
A1	0.00	0.15	0.000	0.006
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.75	3.05	0.108	0.120
E	2.60	3.00	0.102	0.118
E1	1.45	1.75	0.057	0.069
e	0.95 BSC		0.0374 BSC	
e1	1.90 BSC		0.0748 BSC	
L	0.30	0.60	0.012	0.024
L1	0.60 REF		0.024 REF	
# per tape and reel	3000 pieces*			
Controlling dimension: millimeters				

* This is an approximate amount which may vary.

Mechanical Package Diagrams



Package Dimensions for SOT23-6.