

SOJ, TSOP  
Commercial Temp  
Industrial Temp

## 32K x 8 256Kb Asynchronous SRAM

7, 8, 10, 12, 15 ns  
3.3 V  $V_{DD}$   
Corner  $V_{DD}$  and  $V_{SS}$

### Features

- Fast access time: 7, 8, 10, 12, 15 ns
- 75/65/50/50/50 mA at max cycle rate
- Single 3.3 V  $\pm$  0.3 V power supply
- All inputs and outputs are TTL-compatible
- Fully static operation
- Industrial Temperature Option:  $-40^{\circ}$  to  $85^{\circ}\text{C}$
- Package line up
  - SJ: 300 mil, 28-pin SOJ package
  - TS: 8 mm x 13.4 mm, 28-pin TSOP Type I package

### Description

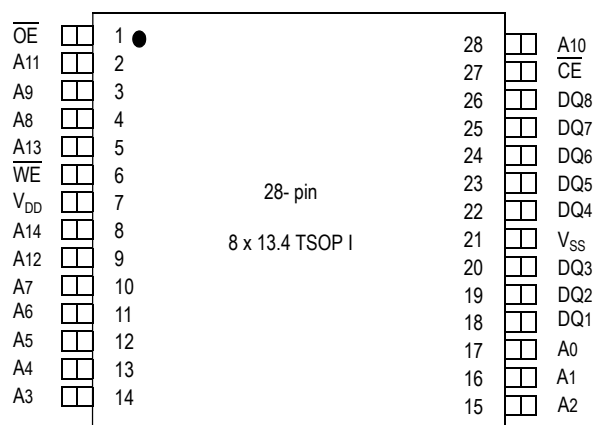
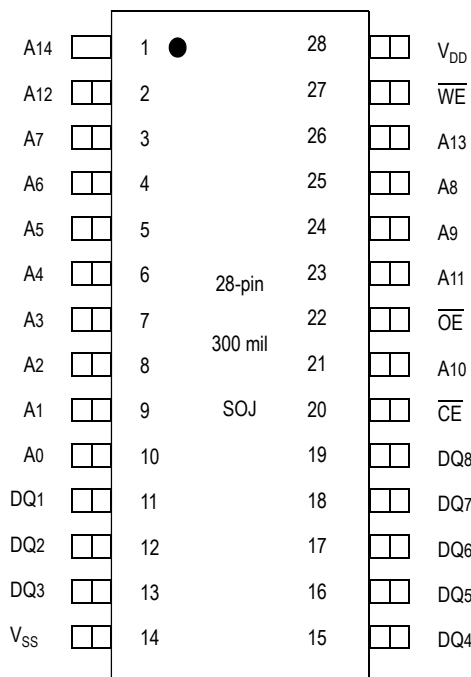
The GS70328 is a high speed CMOS static RAM organized as 32,768 words by 8 bits. Static design eliminates the need for external clocks or timing strobes. The GS70328 operates on a single 3.3 V power supply, and all inputs and outputs are TTL-compatible. The GS70328 is available in 300 mil, 28-pin SOJ and 8 x 13.4 mm<sup>2</sup>, 28-pin TSOP Type-I packages.

### Pin Descriptions

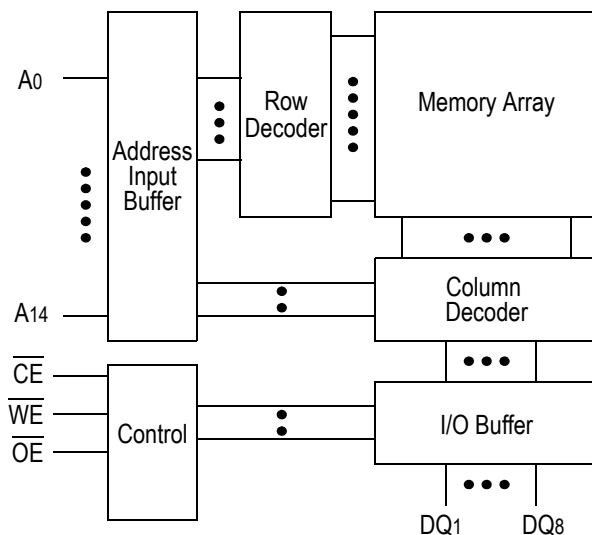
| Symbol           | Description         |
|------------------|---------------------|
| $A_0$ – $A_{14}$ | Address input       |
| $DQ_1$ – $DQ_8$  | Data input/output   |
| $\overline{CE}$  | Chip enable input   |
| $\overline{WE}$  | Write enable input  |
| $\overline{OE}$  | Output enable input |
| $V_{DD}$         | +3.3 V power supply |
| $V_{SS}$         | Ground              |
| NC               | No connect          |

### Pin Configuration

Top view



### Block Diagram



### Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | DQ1 to DQ8   | $V_{\text{DD}}$ Current |
|------------------------|------------------------|------------------------|--------------|-------------------------|
| H                      | X                      | X                      | Not Selected | ISB1, ISB2              |
| L                      | L                      | H                      | Read         | IDD                     |
| L                      | X                      | L                      | Write        |                         |
| L                      | H                      | H                      | High Z       |                         |

X: "H" or "L"

### Absolute Maximum Ratings

| Parameter                   | Symbol           | Rating                                                | Unit               |
|-----------------------------|------------------|-------------------------------------------------------|--------------------|
| Supply Voltage              | $V_{\text{DD}}$  | -0.5 to +4.6                                          | V                  |
| Input Voltage               | $V_{\text{IN}}$  | -0.5 to $V_{\text{DD}} + 0.5$<br>( $\leq 4.6$ V max.) | V                  |
| Output Voltage              | $V_{\text{OUT}}$ | -0.5 to $V_{\text{DD}} + 0.5$<br>( $\leq 4.6$ V max.) | V                  |
| Allowable power dissipation | PD               | 0.7                                                   | W                  |
| Storage temperature         | $T_{\text{STG}}$ | -55 to 150                                            | $^{\circ}\text{C}$ |

#### Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

## Recommended Operating Conditions

| Parameter                                | Symbol   | Minimum | Typical | Maximum        | Unit |
|------------------------------------------|----------|---------|---------|----------------|------|
| Supply Voltage for -7/8/10/12            | $V_{DD}$ | 3.0     | 3.3     | 3.6            | V    |
| Input High Voltage                       | $V_{IH}$ | 2.0     | —       | $V_{DD} + 0.3$ | V    |
| Input Low Voltage                        | $V_{IL}$ | -0.3    | —       | 0.8            | V    |
| Ambient Temperature,<br>Commercial Range | $T_{Ac}$ | 0       | —       | 70             | °C   |
| Ambient Temperature,<br>Industrial Range | $T_{AI}$ | -40     | —       | 85             | °C   |

### Notes:

- Input overshoot voltage should be less than  $V_{DD} + 2$  V and not exceed 20 ns.
- Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

## Capacitance

| Parameter          | Symbol    | Test Condition  | Maximum | Unit |
|--------------------|-----------|-----------------|---------|------|
| Input Capacitance  | $C_{IN}$  | $V_{IN} = 0$ V  | 5       | pF   |
| Output Capacitance | $C_{OUT}$ | $V_{OUT} = 0$ V | 7       | pF   |

### Notes:

- Tested at  $T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz
- These parameters are sampled and are not 100% tested.

## DC I/O Pin Characteristics

| Parameter              | Symbol   | Test Conditions                            | Min   | Max   |
|------------------------|----------|--------------------------------------------|-------|-------|
| Input Leakage Current  | $I_{IL}$ | $V_{IN} = 0$ to $V_{DD}$                   | -1uA  | 1uA   |
| Output Leakage Current | $I_{LO}$ | Output High Z<br>$V_{OUT} = 0$ to $V_{DD}$ | -1uA  | 1uA   |
| Output High Voltage    | $V_{OH}$ | $I_{OH} = -4$ mA                           | 2.4 V | —     |
| Output Low Voltage     | $V_{OL}$ | $I_{LO} = +4$ mA                           | —     | 0.4 V |

## Power Supply Currents

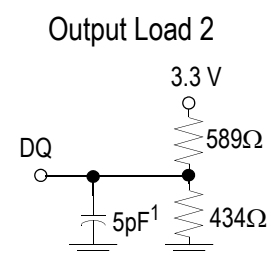
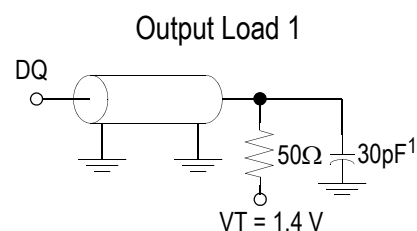
| Parameter                | Symbol | Test Conditions                                                                                                  | 0 to 70°C |       |       |       |       | -40 to 85°C |       |       |       |       |
|--------------------------|--------|------------------------------------------------------------------------------------------------------------------|-----------|-------|-------|-------|-------|-------------|-------|-------|-------|-------|
|                          |        |                                                                                                                  | 7 ns      | 8 ns  | 10 ns | 12 ns | 15 ns | 7 ns        | 8 ns  | 10 ns | 12 ns | 15 ns |
| Operating Supply Current | IDD    | $\overline{CE} \leq V_{IL}$<br>All other inputs $\geq V_{IH}$ or $\leq V_{IL}$<br>Min. cycle time<br>IOUT = 0 mA | 75 mA     | 65 mA | 50 mA | 50 mA | 50 mA | 80 mA       | 70 mA | 55 mA | 55 mA | 55 mA |
| Standby Current          | ISB1   | $\overline{CE} \geq V_{IH}$<br>All other inputs $\geq V_{IH}$ or $\leq V_{IL}$<br>Min. cycle time                | 35 mA     | 30 mA | 25 mA | 25 mA | 25 mA | 40 mA       | 35 mA | 30 mA | 30 mA | 30 mA |
| Standby Current          | ISB2   | $\overline{CE} \geq V_{DD} - 0.2 V$<br>All other inputs $\geq V_{DD} - 0.2 V$ or $\leq 0.2 V$                    | 1 mA      |       |       |       |       | 2 mA        |       |       |       |       |

## AC Test Conditions

| Parameter              | Conditions            |
|------------------------|-----------------------|
| Input high level       | $V_{IH} = 2.4 V$      |
| Input low level        | $V_{IL} = 0.4 V$      |
| Input rise time        | $t_r = 1 V/ns$        |
| Input fall time        | $t_f = 1 V/ns$        |
| Input reference level  | 1.4 V                 |
| Output reference level | 1.4 V                 |
| Output load            | <b>Fig. 1 &amp; 2</b> |

### Notes:

1. Include scope and jig capacitance
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted
3. Output load 2 for tLZ, tHZ, tOLZ and tOHZ



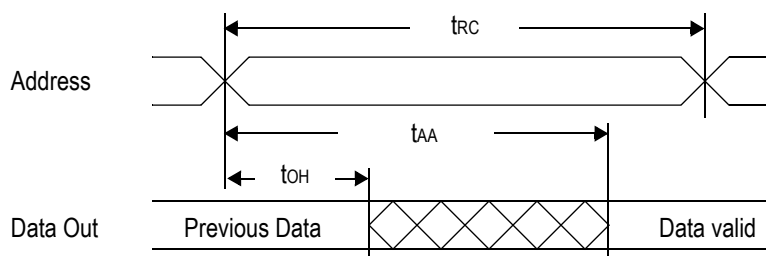
## AC Characteristics

### Read Cycle

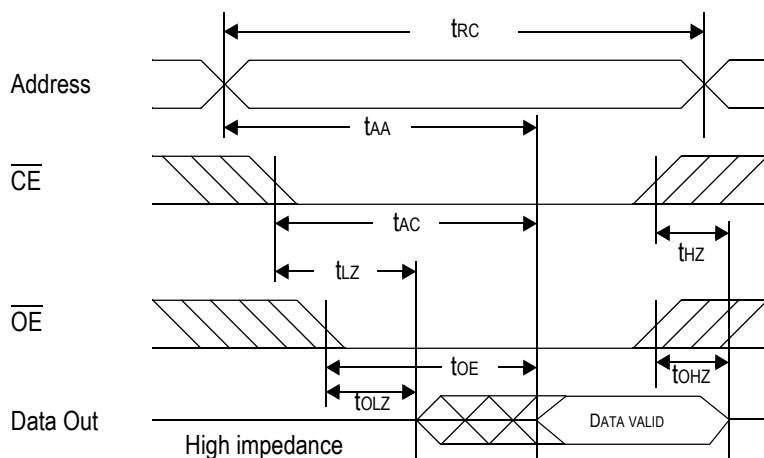
| Parameter                                              | Symbol      | -7  |     | -8  |     | -10 |     | -12 |     | -15 |     | Unit |
|--------------------------------------------------------|-------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
|                                                        |             | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |      |
| Read cycle time                                        | $t_{RC}$    | 7   | —   | 8   | —   | 10  | —   | 12  | —   | 15  | —   | ns   |
| Address access time                                    | $t_{AA}$    | —   | 7   | —   | 8   | —   | 10  | —   | 12  | —   | 15  | ns   |
| Chip enable access time ( $\overline{CE}$ )            | $t_{AC}$    | —   | 7   | —   | 8   | —   | 10  | —   | 12  | —   | 15  | ns   |
| Output enable to output valid ( $\overline{OE}$ )      | $t_{OE}$    | —   | 3.5 | —   | 4   | —   | 5   | —   | 6   | —   | 7   | ns   |
| Output hold from address change                        | $t_{OH}$    | 2   | —   | 2   | —   | 2   | —   | 3   | —   | 3   | —   | ns   |
| Chip enable to output in low Z ( $\overline{CE}$ )     | $t_{LZ}^*$  | 2   | —   | 2   | —   | 2   | —   | 3   | —   | 3   | —   | ns   |
| Output enable to output in low Z ( $\overline{OE}$ )   | $t_{OLZ}^*$ | 0   | —   | 0   | —   | 0   | —   | 0   | —   | 0   | —   | ns   |
| Chip disable to output in High Z ( $\overline{CE}$ )   | $t_{HZ}^*$  | —   | 3.5 | —   | 4   | —   | 5   | —   | 6   | —   | 7   | ns   |
| Output disable to output in High Z ( $\overline{OE}$ ) | $t_{OHZ}^*$ | —   | 3   | —   | 3.5 | —   | 4   | —   | 5   | —   | 6   | ns   |

\* These parameters are sampled and are not 100% tested

**Read Cycle 1:  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$**



### Read Cycle 2: $\overline{WE} = V_{IH}$

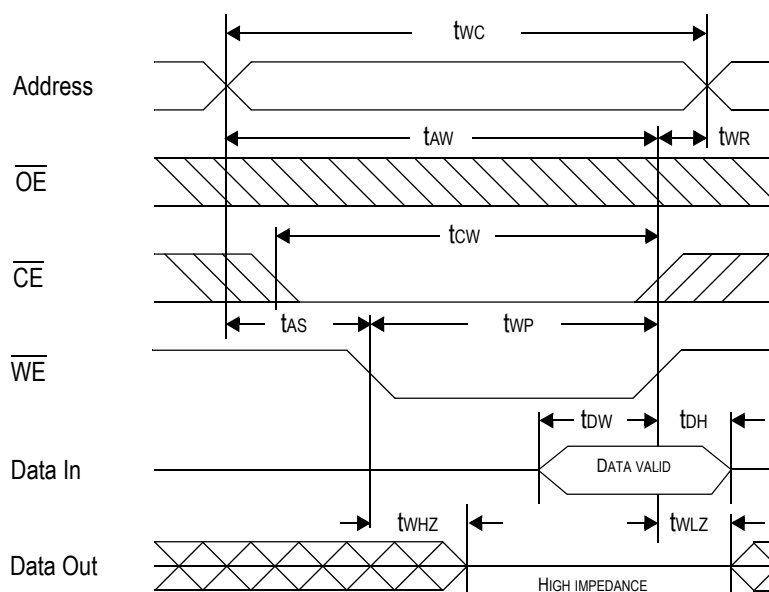


### Write Cycle

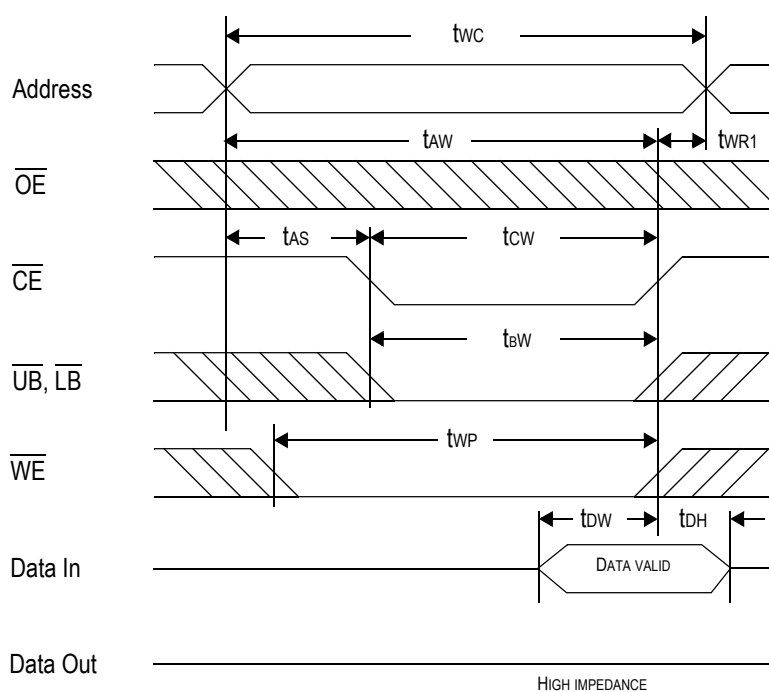
| Parameter                               | Symbol | -7  |     | -8  |     | -10 |     | -12 |     | -15 |     | Unit |
|-----------------------------------------|--------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|
|                                         |        | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |      |
| Write cycle time                        | tWC    | 7   | —   | 8   | —   | 10  | —   | 12  | —   | 15  | —   | ns   |
| Address valid to end of write           | tAW    | 5   | —   | 5.5 | —   | 7   | —   | 10  | —   | 13  | —   | ns   |
| Chip enable to end of write             | tCW    | 5   | —   | 5.5 | —   | 7   | —   | 10  | —   | 13  | —   | ns   |
| Data set up time                        | tDW    | 3.5 | —   | 4   | —   | 5   | —   | 7   | —   | 10  | —   | ns   |
| Data hold time                          | tDH    | 0   | —   | 0   | —   | 0   | —   | 0   | —   | 0   | —   | ns   |
| Write pulse width                       | tWP    | 5   | —   | 5.5 | —   | 7   | —   | 10  | —   | 13  | —   | ns   |
| Address set up time                     | tAS    | 0   | —   | 0   | —   | 0   | —   | 0   | —   | 0   | —   | ns   |
| Write recovery time ( $\overline{WE}$ ) | tWR    | 0   | —   | 0   | —   | 0   | —   | 0   | —   | 0   | —   | ns   |
| Write recovery time ( $\overline{CE}$ ) | tWR1   | 0   | —   | 0   | —   | 0   | —   | 0   | —   | 0   | —   | ns   |
| Output Low Z from end of write          | tWLZ*  | 2   | —   | 2   | —   | 2   | —   | 3   | —   | 3   | —   | ns   |
| Write to output in High Z               | tWHZ*  | —   | 3   | —   | 3.5 | —   | 4   | —   | 5   | —   | 5   | ns   |

\* These parameters are sampled and are not 100% tested

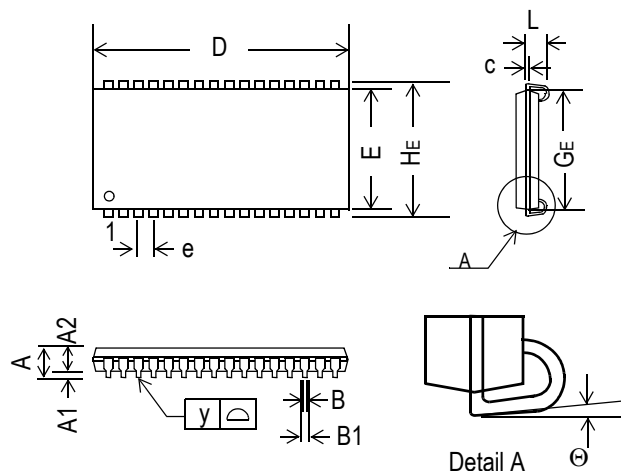
### Write Cycle 1: $\overline{WE}$ control



### Write Cycle 2: $\overline{CE}$ control



## 28-Pin SOJ, 300 mil

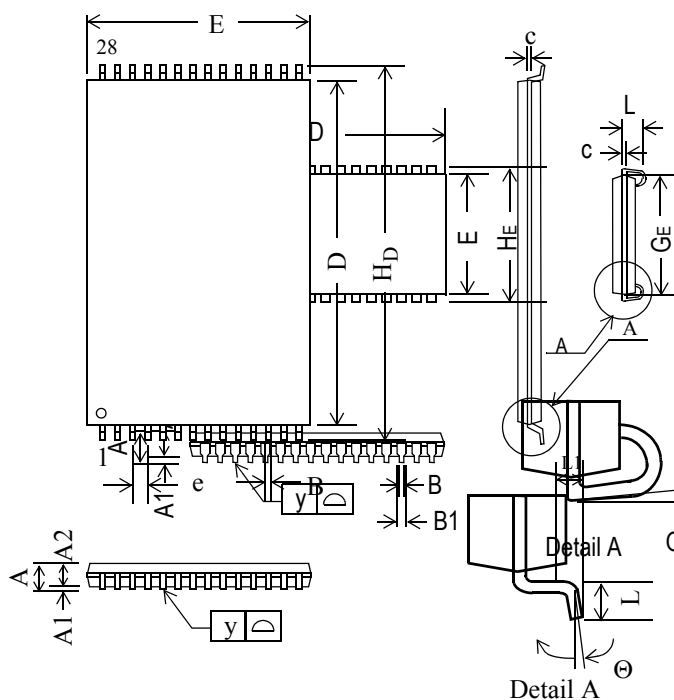


| Symbol | Dimension in inch |       |       | Dimension in mm |       |       |
|--------|-------------------|-------|-------|-----------------|-------|-------|
|        | min               | nom   | max   | min             | nom   | max   |
| A      | —                 | —     | 0.148 | —               | —     | 3.76  |
| A1     | 0.025             | —     | —     | 0.64            | —     | —     |
| A2     | 0.095             | 0.100 | 0.105 | 2.41            | 2.54  | 2.67  |
| B      | 0.015             | —     | 0.020 | 0.38            | —     | 0.51  |
| B1     | 0.026             | 0.028 | 0.032 | 0.66            | 0.71  | 0.81  |
| c      | 0.008             | 0.010 | 0.012 | 0.20            | 0.25  | 0.30  |
| D      | 0.705             | 0.71  | 0.715 | 17.91           | 18.03 | 18.16 |
| E      | 0.295             | 0.300 | 0.305 | 7.49            | 7.62  | 7.75  |
| e      | —                 | 0.05  | —     | —               | 1.27  | —     |
| HE     | 0.330             | 0.335 | 0.340 | 8.38            | 8.51  | 8.64  |
| GE     | 0.255             | 0.265 | 0.275 | 6.48            | 6.73  | 6.985 |
| L      | 0.082             | —     | —     | 2.08            | —     | —     |
| y      | —                 | —     | 0.004 | —               | —     | 0.10  |
| Θ      | 0°                | —     | 10°   | 0°              | —     | 10°   |

**Notes:**

1. Dimension D & E do not include interlead flash
2. Dimension B1 does not include dambar protrusion/intrusion
3. Controlling dimension: inches

## 28-Pin TSOP-I, 8 mm x 13.4 mm



| Symbol         | Dimension in inch |       |       | Dimension in mm |      |      |
|----------------|-------------------|-------|-------|-----------------|------|------|
|                | min               | nom   | max   | min             | nom  | max  |
| A              | —                 | —     | 0.047 | —               | —    | 1.20 |
| A1             | 0.002             | —     | 0.006 | 0.05            | —    | 0.15 |
| A2             | 0.035             | 0.040 | 0.041 | 0.90            | 1.00 | 1.05 |
| B              | 0.007             | 0.008 | 0.011 | 0.17            | 0.20 | 0.27 |
| D              | —                 | 0.465 | —     | —               | 11.8 | —    |
| H <sub>D</sub> | —                 | .528  | —     | —               | 13.4 | —    |
| c              | 0.004             | 0.006 | 0.008 | 0.10            | 0.15 | 0.21 |
| E              | —                 | 0.315 | —     | —               | 8.00 | —    |
| e              | —                 | 0.022 | —     | —               | 0.55 | —    |
| L              | 0.020             | 0.024 | 0.028 | 0.50            | 0.60 | 0.70 |
| L1             | 0.024             | 0.032 | 0.040 | 0.60            | 0.80 | 1.00 |
| y              | —                 | —     | 0.003 | —               | —    | 0.08 |
| Θ              | 0°                | —     | 5°    | 0°              | —    | 5°   |

**Notes:**

1. Dimension D & E do not include interlead flash
2. Dimension B1 does not include dambar protrusion/intrusion
3. Controlling dimension: inches
4. Profile tolerance zones for D and E do not include mold protrusion. Allowable mold protrusion on E is 0.15 mm per side and on D is 0.25 mm per side.

**Ordering Information**

| Part Number * | Package                         | Access Time | Temp. Range | Status |
|---------------|---------------------------------|-------------|-------------|--------|
| GS70328SJ-7   | 300-mil SOJ                     | 7 ns        | Commercial  |        |
| GS70328SJ-8   | 300-mil SOJ                     | 8 ns        | Commercial  |        |
| GS70328SJ-10  | 300-mil SOJ                     | 10 ns       | Commercial  |        |
| GS70328SJ-12  | 300-mil SOJ                     | 12 ns       | Commercial  |        |
| GS70328SJ-15  | 300-mil SOJ                     | 15 ns       | Commercial  |        |
| GS70328SJ-7I  | 300-mil SOJ                     | 7 ns        | Industrial  |        |
| GS70328SJ-8I  | 300-mil SOJ                     | 8 ns        | Industrial  |        |
| GS70328SJ-10I | 300-mil SOJ                     | 10 ns       | Industrial  |        |
| GS70328SJ-12I | 300-mil SOJ                     | 12 ns       | Industrial  |        |
| GS70328SJ-15I | 300-mil SOJ                     | 15 ns       | Industrial  |        |
| GS70328TS-7   | TSOP-I 8 x 13.4 mm <sup>2</sup> | 7 ns        | Commercial  |        |
| GS70328TS-8   | TSOP-I 8 x 13.4 mm <sup>2</sup> | 8 ns        | Commercial  |        |
| GS70328TS-10  | TSOP-I 8 x 13.4 mm <sup>2</sup> | 10 ns       | Commercial  |        |
| GS70328TS-12  | TSOP-I 8 x 13.4 mm <sup>2</sup> | 12 ns       | Commercial  |        |
| GS70328TS-15  | TSOP-I 8 x 13.4 mm <sup>2</sup> | 15 ns       | Commercial  |        |
| GS70328TS-7I  | TSOP-I 8 x 13.4 mm <sup>2</sup> | 7 ns        | Industrial  |        |
| GS70328TS-8I  | TSOP-I 8 x 13.4 mm <sup>2</sup> | 8 ns        | Industrial  |        |
| GS70328TS-10I | TSOP-I 8 x 13.4 mm <sup>2</sup> | 10 ns       | Industrial  |        |
| GS70328TS-12I | TSOP-I 8 x 13.4 mm <sup>2</sup> | 12 ns       | Industrial  |        |
| GS70328TS-15I | TSOP-I 8 x 13.4 mm <sup>2</sup> | 15 ns       | Industrial  |        |

\* Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS70328TP-8T

**R**
**Revision History**

| <b>Rev. Code: Old;<br/>New</b>             | <b>Types of Changes<br/>Format or Content</b> | <b>Page #/Revisions/Reason</b>                                                                  |
|--------------------------------------------|-----------------------------------------------|-------------------------------------------------------------------------------------------------|
| 1.03 8/1999;<br>1.04 11/1999               | Content                                       | • Added 12ns speed bin information to 70328 datasheet.                                          |
| GS70328Rev1.04 12/1999KRev<br>1.05 2/2000L | Format/Content                                | • GSI Logo                                                                                      |
| Rev 1.05 2/2000L; Rev1.06 6/2000           | Content                                       | • Nominal value for $H_D$ on the TSOP-I 28-pin package changed to 13.4                          |
| Rev1.06; Rev1.07                           | Format/Content                                | • Updated format to conform to Tech Pubs standards<br>• Corrected errors in both case diagrams  |
| 70328_r1_07; 70328_r1_08                   | Content                                       | • Added 12 ns reference to Parameter column in Recommended Operating Conditions table on page 3 |
| 70328_r1_08; 70328_r1_09                   | Content                                       | • Added 15 ns references to entire document                                                     |
| 70328_r1_09; 70328_r1_10                   | Content                                       | • Removed 6 ns speed bin from entire document                                                   |
| 70328_r1_10; 70328_r1_11                   | Format                                        | • Updated format                                                                                |