# DS1642
# Nonvolatile Timekeeping RAM

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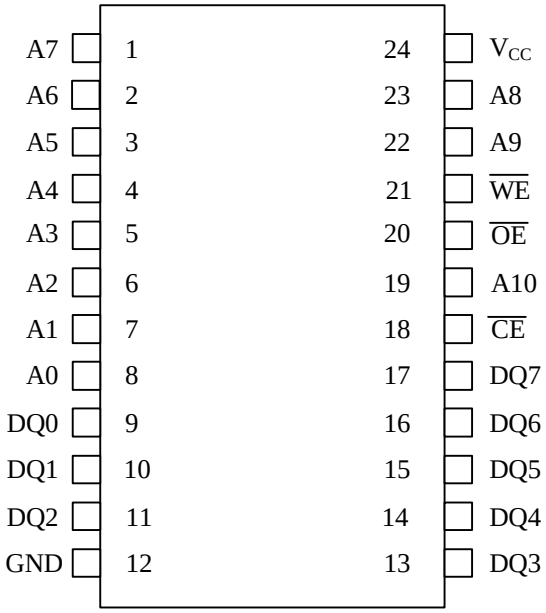
## FEATURES

- Integrated NV SRAM, real time clock, crystal, power fail control circuit and lithium energy source
- Standard JEDEC bytewide 2K x 8 static RAM pinout
- Clock registers are accessed identically to the static RAM. These registers are resident in the eight top RAM locations
- Totally nonvolatile with over 10 years of operation in the absence of power
- Access times of 70 ns and 100 ns
- Quartz accuracy ±1 minute a month @ 25°C, factory calibrated
- BCD coded year, month, date, day, hours, minutes, and seconds with leap year compensation valid up to 2100
- Power-fail write protection allows for ±10% $V_{CC}$ power supply tolerance
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time

## PIN ASSIGNMENT




## PIN DESCRIPTION

| | |
|---|---|
| A0-A10 | - Address Input |
| $\overline{CE}$ | - Chip Enable |
| $\overline{OE}$ | - Output Enable |
| $\overline{WE}$ | - Write Enable |
| $V_{CC}$ | - +5 Volts |
| GND | - Ground |
| DQ0-DQ7 | - Data Input/Output |

## ORDERING INFORMATION

| | |
|---|---|
| DS1642-70 | 70 ns access |
| DS1642-100 | 100 ns access |

## DESCRIPTION

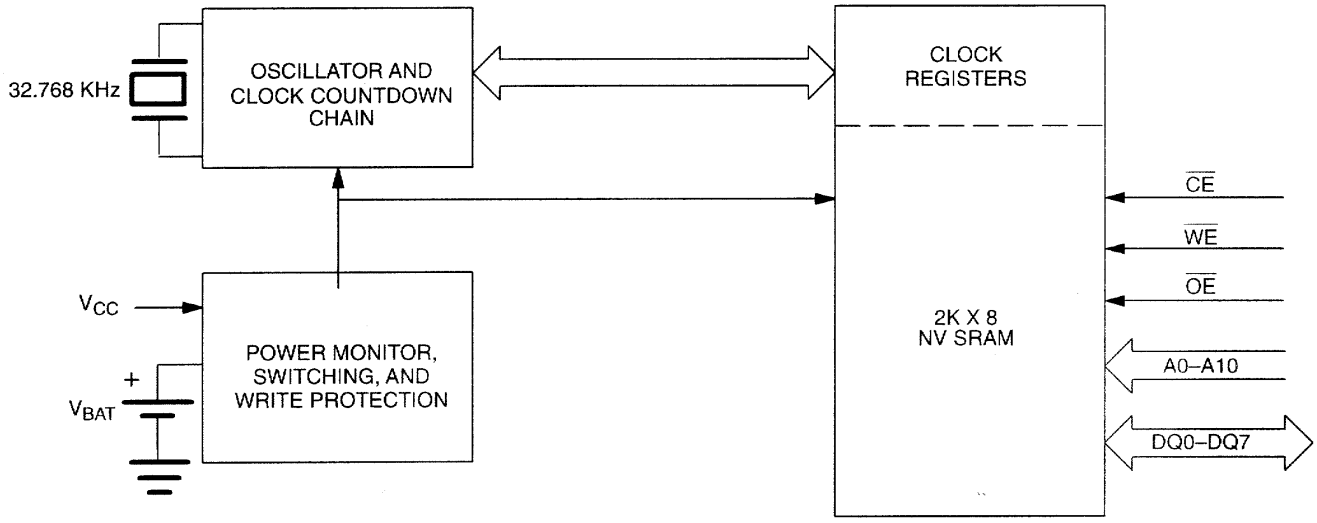
The DS1642 is a 2K x 8 nonvolatile static RAM and a full-function real time clock which are both accessible in a bytewide format. The nonvolatile time keeping RAM is pin- and function-equivalent to any JEDEC standard 2K x 8 SRAM. The device can also be easily substituted in ROM, EPROM and EEPROM sockets, providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also

prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1642 also contains its own power-fail circuitry which deselects the device when the $V_{CC}$ supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low $V_{CC}$ as errant access and update cycles are avoided.

## CLOCK OPERATIONS-READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1642 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the 7th most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was current at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1642 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to 0.

## DS1642 BLOCK DIAGRAM Figure 1




## DS1642 TRUTH TABLE Table 1

| $V_{CC}$ | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | MODE | DQ | POWER |
|---|---|---|---|---|---|---|
| 5 VOLTS ± 10% | $V_{IH}$ | X | X | DESELECT | HIGH Z | STANDBY |
| | $V_{IL}$ | X | $V_{IL}$ | WRITE | DATA IN | ACTIVE |
| | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | READ | DATA OUT | ACTIVE |
| | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | READ | HIGH Z | ACTIVE |
| <4.5 VOLTS >$V_{BAT}$ | X | X | X | DESELECT | HIGH Z | CMOS STANDBY |
| <$V_{BAT}$ | X | X | X | DESELECT | HIGH Z | DATA RETENTION MODE |

## SETTING THE CLOCK

The 8th bit of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1642 registers. The user can then load them with the correct day, date and time data in 24-hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

## STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

## FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, and $\overline{OE}$ low) and address for seconds register remain valid and stable.

## CLOCK ACCURACY

The DS1642 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The clock is calibrated at the factory by Dallas Semiconductor using special calibration nonvolatile tuning elements. The DS1642 does not require additional calibration and temperature deviations will have a negligible effect in most applications. For this reason, methods of field clock calibration are not available and not necessary.

## DS1642 REGISTER MAP – BANK1 Table 2

| ADDRESS | DATA | | | | | | | | FUNCTION | |
|---|---|---|---|---|---|---|---|---|---|---|
| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| 7FF | - | - | - | - | - | - | - | - | YEAR | 00-99 |
| 7FE | X | X | X | - | - | - | - | - | MONTH | 01-12 |
| 7FD | X | X | - | - | - | - | - | - | DATE | 01-31 |
| 7FC | X | FT | X | X | X | - | - | - | DAY | 00-23 |
| 7FB | X | X | - | - | - | - | - | - | HOUR | 00-59 |
| 7FA | X | - | - | - | - | - | - | - | MINUTES | 00-59 |
| 7F9 | $\overline{OSC}$ | - | - | - | - | - | - | - | SECONDS | 00-59 |
| 7F8 | W | R | X | X | X | X | X | X | CONTROL | A |

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

## NOTE:

All indicated "X" bits are not dedicated to any particular function and can be used as normal RAM bits.

## RETRIEVING DATA FROM RAM OR CLOCK

The DS1642 is in the read mode whenever $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple−through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within $t_{AA}$ after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access ($t_{CEA}$) or at output enable access time ($t_{OEA}$). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before $t_{AA}$, the data lines are driven to an intermediate state until $t_{AA}$. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time ($t_{OH}$) but will then go indeterminate until the next address access.

## WRITING DATA TO RAM OR CLOCK

The DS1642 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of $t_{WR}$ prior to the initiation of another read or write cycle. Data in must be valid $t_{DS}$ prior to the end of write and remain valid for $t_{DH}$ afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs $t_{WEZ}$ after $\overline{WE}$ goes active.

## DATA RETENTION MODE

When $V_{CC}$ is within nominal limits ($V_{CC}$ > 4.5 volts) the DS1642 can be accessed as described above by read or write cycles. However, when $V_{CC}$ is below the power-fail point $V_{PF}$ (point at which write protection occurs) the internal clock registers and RAM is blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. When $V_{CC}$ falls below the level of the internal battery supply, power input is switched from the $V_{CC}$ pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until $V_{CC}$ is returned to nominal level.

## BATTERY LONGEVITY

The DS1642 has a lithium power source that is designed to provide energy for clock activity, and clock and RAM data retention when the $V_{CC}$ supply is not present. The capability of this internal power supply is sufficient to power the DS1642 continuously for the life of the equipment in which it is installed. For specification purposes, the life expectancy is 10 years at 25°C with the internal clock oscillator running in the absence of $V_{CC}$ power. Each DS1642 is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When $V_{CC}$ is first applied at a level greater than $V_{PF}$, the lithium energy source is enabled for battery backup operation. Actual life expectancy of the DS1642 will be much longer than 10 years since no lithium battery energy is consumed when $V_{CC}$ is present.

## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on Any Pin Relative to Ground | –0.3V to +7.0V |
| Operating Temperature | 0°C to 70°C |
| Storage Temperature | –20°C to +70°C |
| Soldering Temperature | 260°C for 10 seconds (See Note 6) |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Logic 1 Voltage All Inputs | $V_{IH}$ | 2.2 | | $V_{CC}$+0.3 | V | 1 |
| Logic 0 Voltage All Inputs | $V_{IL}$ | -0.3 | | 0.8 | V | 1 |

## DC ELECTRICAL CHARACTERISTICS

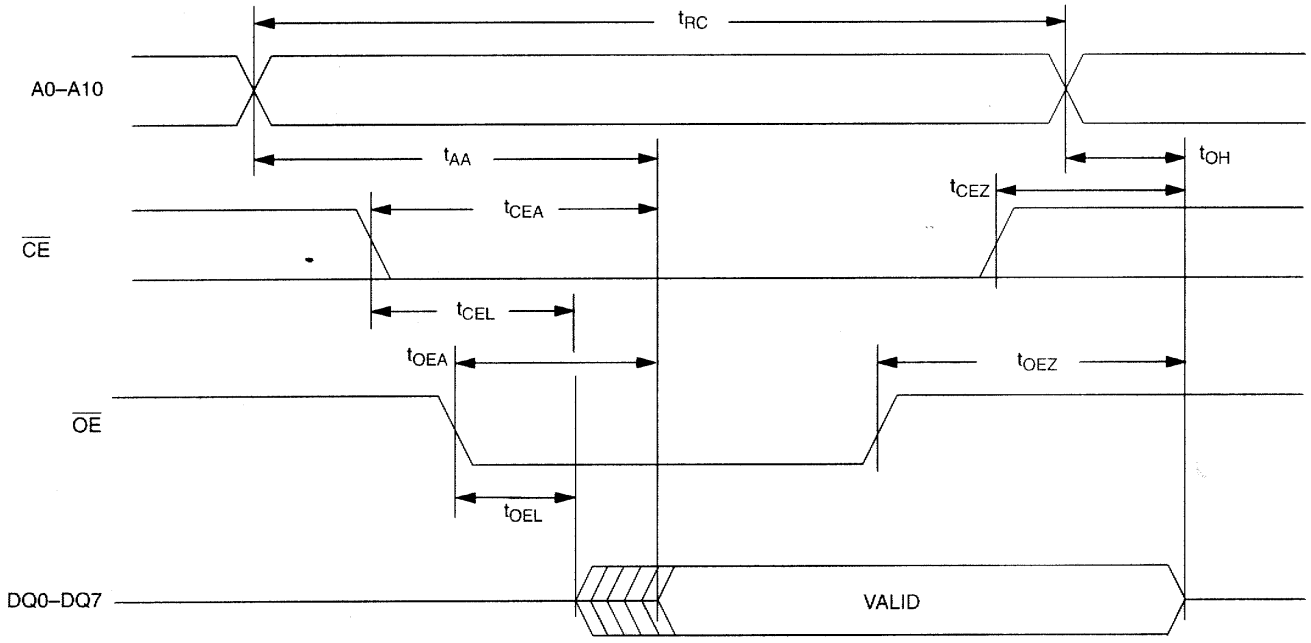
($0°C \leq t_A \leq 70°C$; $V_{CC}$ (MAX) $\leq V_{CC} \leq V_{CC}$ (MIN)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Active Supply Current | $I_{CC}$ | | 15 | 50 | mA | 2, 3 |
| TTL Standby Current ($\overline{CE} = V_{IH}$) | $I_{CC1}$ | | 1 | 3 | mA | 2, 3 |
| CMOS Standby Current ($\overline{CE} \leq V_{CC}$-0.2V) | $I_{CC2}$ | | 1 | 3 | mA | 2, 3 |
| Input Leakage Current (any input) | $I_{IL}$ | -1 | | +1 | µA | |
| I/O Leakage Current (any output) | $I_{OL}$ | -1 | | +1 | µA | |
| Output Logic 1 Voltage ($I_{OUT}$ = -1.0 mA) | $V_{OH}$ | 2.4 | | | | 1 |
| Output Logic 0 Voltage ($I_{OUT}$ = +2.1 mA) | $V_{OL}$ | | | 0.4 | | 1 |
| Write Protection Voltage | $V_{PF}$ | 4.25 | 4.37 | 4.50 | V | 1 |

## READ CYCLE, AC CHARACTERISTICS (0°C to 70°C; VCC = 5.0V ± 10%)

| PARAMETER | SYMBOL | 70 ns access | | 100 ns access | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Read Cycle Time | $t_{RC}$ | 70 | | 100 | | ns | |
| Address Access Time | $t_{AA}$ | | 70 | | 100 | ns | |
| $\overline{CE}$ to DQ Low-Z | $t_{CEL}$ | 5 | | 5 | | ns | |
| $\overline{CE}$ Access Time | $t_{CEA}$ | | 70 | | 100 | ns | |
| $\overline{CE}$ Data Off Time | $t_{CEZ}$ | | 25 | | 35 | ns | |
| $\overline{OE}$ to DQ Low-Z | $t_{OEL}$ | 5 | | 5 | | ns | |
| $\overline{OE}$ Access Time | $t_{OEA}$ | | 35 | | 55 | ns | |
| $\overline{OE}$ Data Off Time | $t_{OEZ}$ | | 25 | | 35 | ns | |
| Output Hold from Address | $t_{OH}$ | 5 | | 5 | | ns | |

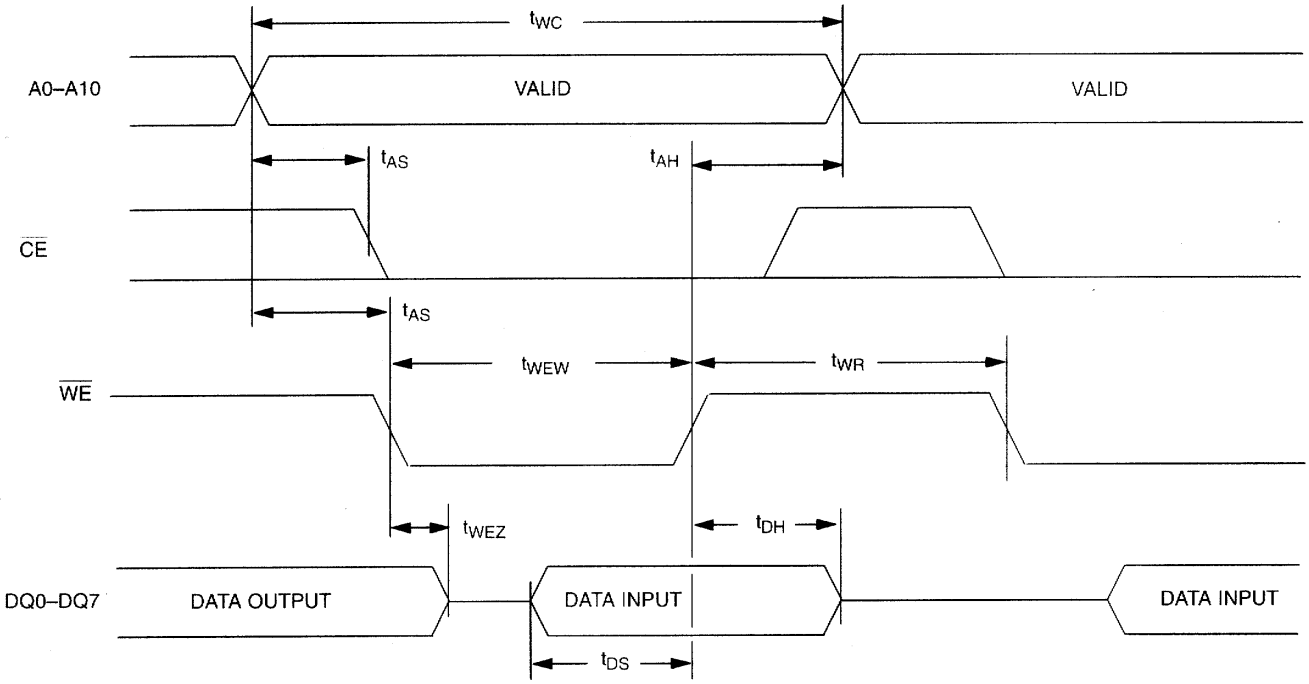
## READ CYCLE TIMING DIAGRAM



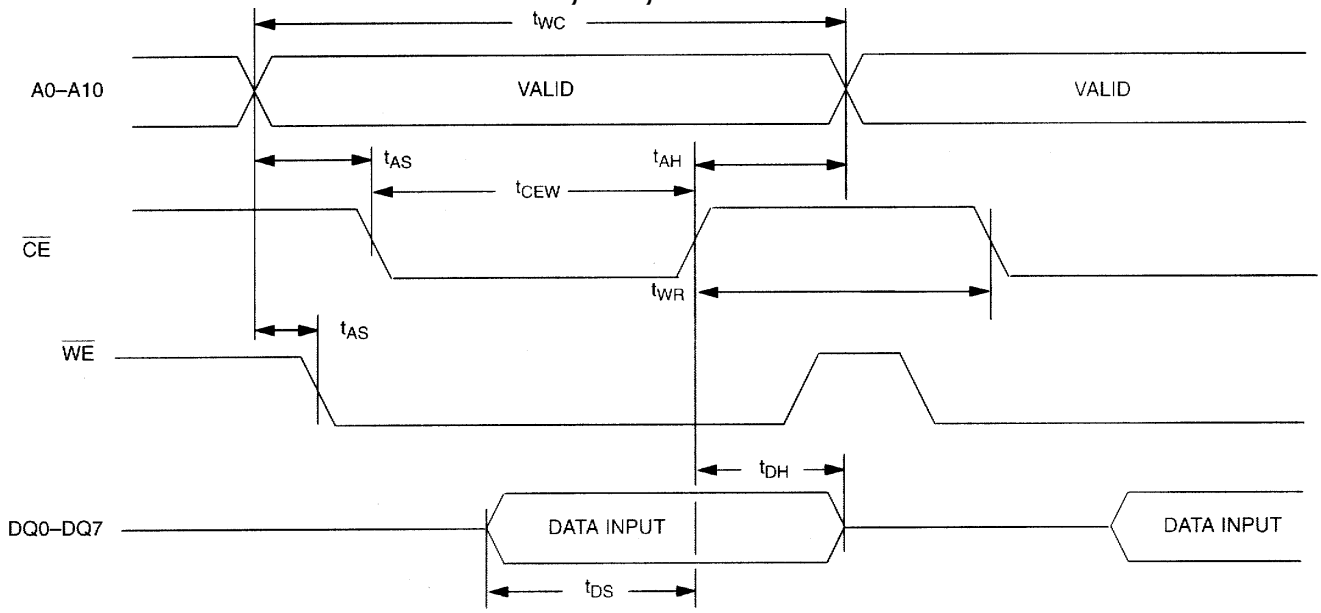
## WRITE CYCLE, AC CHARACTERISTICS (0°C to 70°C; VCC = 5.0V ± 10%)

| PARAMETER | SYMBOL | 70 ns access | | 100 ns access | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Write Cycle Time | $t_{WC}$ | 70 | | 100 | | ns | |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | ns | |
| $\overline{WE}$ Pulse Width | $t_{WEW}$ | 50 | | 70 | | ns | |
| $\overline{CE}$ Pulse Width | $t_{CEW}$ | 60 | | 75 | | ns | |
| Data Setup Time | $t_{DS}$ | 30 | | 40 | | ns | |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | ns | |
| Address Hold Time | $t_{AH}$ | 5 | | 5 | | ns | |
| $\overline{WE}$ Data Off Time | $t_{WEZ}$ | | 25 | | 35 | ns | |
| Write Recovery Time | $t_{WR}$ | 5 | | 5 | | ns | |

## WRITE CYCLE TIMING DIAGRAM, WRITE-ENABLE CONTROLLED



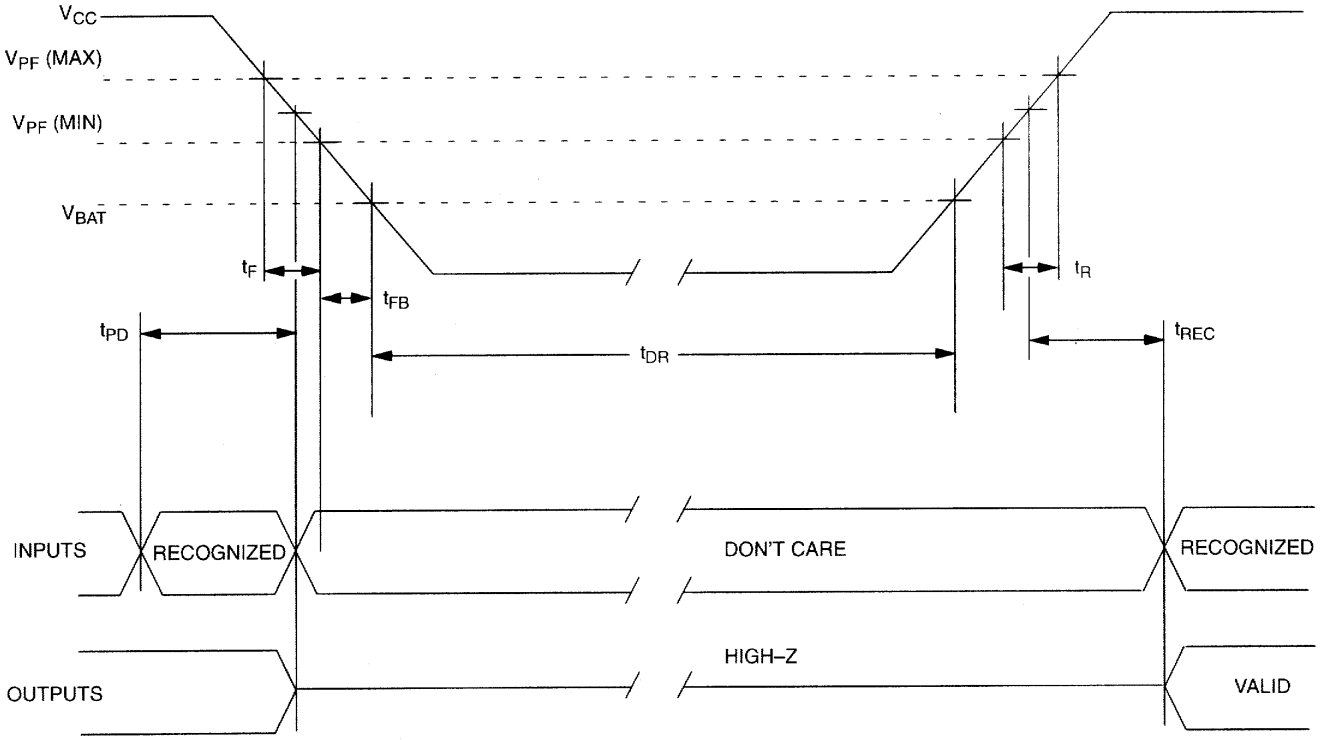

## WRITE CYCLE TIMING DIAGRAM, $\overline{CE}$, CONTROLLED



## POWER-UP/DOWN AC CHARACTERISTICS (0°C to 70°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ or $\overline{WE}$ at $V_{IH}$ Before Power-down | $t_{PD}$ | 0 | | | µs | |
| $V_{CC}$ Fall Time: $V_{PF}$ (MAX) to $V_{PF}$ (Min) | $t_F$ | 300 | | | µs | |
| $V_{CC}$ Fall Time: $V_{PF}$ (MIN) to $V_{BAT}$ | $t_{FB}$ | 10 | | | µs | |
| $V_{CC}$ Rise Time: $V_{PF}$ (MIN) to $V_{PF}$ (MAX) | $t_R$ | 0 | | | µs | |
| Power-up Recover Time | $t_{REC}$ | | | 35 | ms | |
| Expected Data Retention Time (Oscillator On) | $t_{DR}$ | 10 | | | years | 4, 5 |

## POWER-UP/DOWN WAVEFORM TIMING




## CAPACITANCE ($t_A$ = 25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Capacitance on all pins (except DQ) | $C_{IN}$ | | | 7 | pF | |
| Capacitance on DQ pins | $C_O$ | | | 10 | pF | |

## AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0.0 to 3.0 Volts
Timing Measurement Reference Levels:
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

## NOTES:

1. Voltages are referenced to ground.

2. Typical values are at 25°C and nominal supplies.

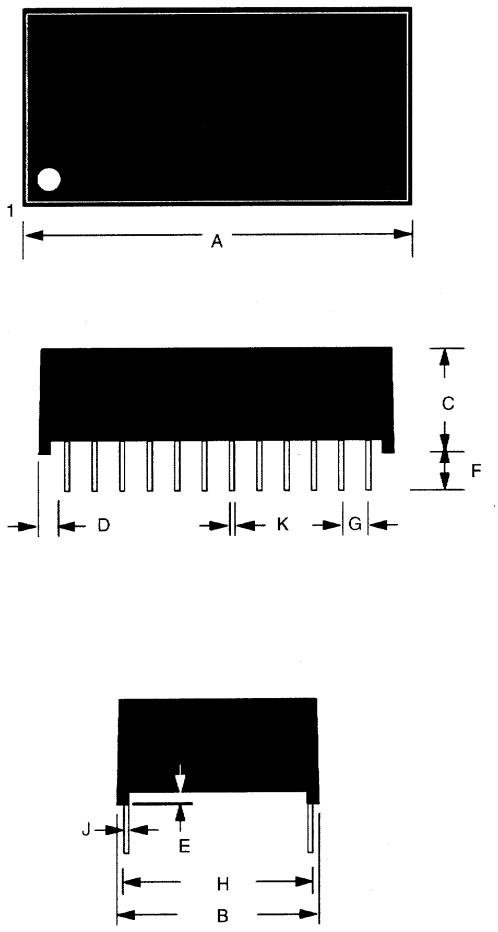
3. Outputs are open.

4. Data retention time is at 25°C.

5. Each DS1642 has a built−in switch that disconnects the lithium source until $V_{CC}$ is first applied by the user. The expected $t_{DR}$ is defined as a cumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user.

6. Real Time Clock Modules can be successfully processed through conventional wave−soldering techniques as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post-solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used to prevent damage to the crystal.

# DS1642 24-PIN PACKAGE




| PKG | 24-PIN | |
|---|---|---|
| DIM. | MIN | MAX |
| A IN. | 1.270 | 0.290 |
| MM | 37.34 | 37.85 |
| B IN. | 0.675 | 0.700 |
| MM | 17.15 | 17.78 |
| C IN. | 0.315 | 0.335 |
| MM | 8.00 | 78.51 |
| D IN. | 0.075 | 0.105 |
| MM | 1.91 | 2.67 |
| E IN. | 0.015 | 0.030 |
| MM | 0.38 | 0.76 |
| F IN. | 0.140 | 0.180 |
| MM | 3.56 | 4.57 |
| G IN. | 0.090 | 0.110 |
| MM | 2.29 | 2.79 |
| H IN. | 0.590 | 0.630 |
| MM | 14.99 | 16.00 |
| J IN. | 0.010 | 0.018 |
| MM | 0.25 | 0.45 |
| K IN. | 0.015 | 0.025 |
| MM | 0.43 | 0.58 |