New Features of the X25057 and X25097

by Application Staff

Introduction

This application note discusses the new features of the X25057 and X25097 EEPROM. The X25057 and X25097 is a CMOS 4K/8K-bit serial EEPROM, internally organized as 512/1024 x 8. The X25057 and X25097 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select (CS) input, allowing any number of devices to share the same bus.

High Speed and Low Power

Revolutionary changes are affecting system designs. This change is occurring because of a confluence of factors ranging from power consumption to physical size to I/O requirements. The Xicor X25057 and X25097 were designed to meet the needs of high speed, small size, and low power, and still be transparent to existing designs.

The X25057 and X25097 will operate at 3MHz at 1.8 volts and 5MHz at 2.7volts, and draw less than 1 uA when in the standby mode. These devices have been designed to meet the low power needs of portable battery powered products. When idle they consume less than 5 microwatts, resulting in extended battery life.

Table 1: Total download time to access 8K bits

		Time to read 8K bits
2-wire	- 100KHz	83 ms
	- 400KHz	20 ms
SPI	- 1 MHz	8.3 ms
	- 2 MHz	4.1 ms
	- 5 MHz	1.6 ms

Block Lock™ and ID Lock™ Options

Xicor has enhanced the Block Lock Operation on the X25057 and X25097. These devices now provide the end-user the ability to Block Lock none of the array, any one quadrant, or the lower half of the array (H1). ID Lock allows the user to protect either the first or last page only. By setting three bits in the Status Register, the user can prevent a write operation from changing data in the Block Locked or ID Locked region. This is especially important when there are configuration parameters, critical data or manufacturing information on the same device as other data that is being changed more often or is of less significance.

In order to change the Block Lock and ID Lock bits, the following steps are required:

1. Perform a Write Enable Operation to set the “Write Enable Latch”.

7	6	5	4	3	2	1	0
0	0	0	0	0	IDL2	IDL1	IDL0

Note: Bits [7:3] specified to be “0’s,

Figure 2. Status Register/ID Lock Protection Byte