OP- 07
Precision Operational Amplifier

Description

The OP-07 operational amplifier is designed for precision low-level signal conditioning where ultra low V_{OS} and TCV_{OS} are required along with very low bias currents. Internal compensation eliminates the need for external components. Novel circuit design and tight process controls are used to obtain very low values of V_{OS} which is further reduced by computer controlled digital nulling techniques at test. Low frequency noise is minimized. Internal biasing techniques reduce external bias and offset currents to values on the order of ±1 nA over the military temperature range. The OP-07 is a direct replacement for the 108A. The OP-07 can also replace chopper stabilized amplifiers in many applications.

Features

- Low noise – 0.35 μV_{p-p} (0.1 Hz to 10 Hz)
- Ultra low V_{OS} – 10 μV
- Ultra low V_{OS} drift – 0.2 $\mu V/^{\circ}C$
- Long term stability — 0.2 $\mu V/Mo$
- Low Input bias current — ±1 nA
- High CMRR – 120 dB min
- Wide input voltage range — ±14V
- Wide supply voltage range — ±3V to ±22V
- Fits 108A and 741 sockets

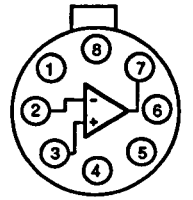
Ordering Information

Part Number	Package	Operating Temperature Range
OP-07CN	N	0°C to +70°C
OP-07DN	N	0°C to +70°C
OP-07EN	N	0°C to +70°C
OP-07CM	M	0°C to +70°C
OP-07DM	M	0°C to +70°C
OP-07EM	M	0°C to +70°C
OP-07T	T	-55°C to +125°C
OP-07T/883B	T	-55°C to +125°C
OP-07AT	T	-55°C to +125°C
OP-07AT/883B	T	-55°C to +125°C
OP-07D	D	-55°C to +125°C
OP-07D/883B	D	-55°C to +125°C
OP-07AD	D	-55°C to +125°C
OP-07AD/883B	D	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
T = 8-lead metal can (TO-99)
M = 8-lead plastic SOIC

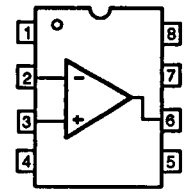
Connection Information

8-Lead TO-99 Metal Can
(Top View)



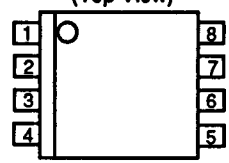
65-03205

8-Lead Dual In-Line Package
(Top View)



65-03206A

8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$ (Case)
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage[1] ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation[2] ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
  Range ..... -65°C to +150°C
Operating Temperature Range
  OP-07A ..... -55°C to +125°C
  OP-07E/C/D ..... -25°C to +85°C
Lead Soldering Temperature
  SO-8 (10 sec) ..... +260°C
  TO-99, DIP (60 sec) ..... +300°C

Notes:

1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Observe package thermal characteristics.

Thermal Characteristics

	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Plastic SO	8-Lead Plastic DIP
Max. Junction Temp.	+175°C	+175°C	+125°C	+125°C
Max. P_D T_A <50°C	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	45°C/W	50°C/W	–	–
Therm. Res. θ_{JA}	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			10	25		30	75	µV
Long Term V_{OS} Stability[3,4]			0.2	1.0		0.2	1.0	µV/Mo
Input Offset Current			0.3	2.0		0.4	2.8	nA
Input Bias Current			±0.7	±2.0		±1.0	±3.0	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density[2]	F_O = 10 Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10	13		10	13	
	F_O = 1000 Hz		9.6	11		9.6	11	
Input Noise Current[2]	0.1 Hz to 10 Hz		14	30		14	35	pA_{p-p}
Input Noise Current Density[2]	F_O = 10 Hz		0.32	0.80		0.32	0.80	$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14	0.23		0.14	0.23	
	F_O = 1000 Hz		0.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[3]		30	80		20	60		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	110	126		110	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	100	110		100	110		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	300	500		200	500		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500$ kΩ, V_{OUT} = ±0.5V, V_S = ±3V	150	500		150	500		V/mV
Output Voltage Swing	$R_L \geq 10$ kΩ,	±12.5	±13		±12.5	±13		V
	$R_L \geq 2$ kΩ,	±12	±12.8		±12	±12.8		
	$R_L \geq 1$ kΩ,	±10.5	±12		±10.5	±12		
Slew Rate	$R_L \geq 2$ kΩ,	0.1	0.3		0.1	0.3		V/µS
Unity Gain Bandwidth	A_{VOL} = +1.0		0.8			0.8		MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60		Ω
Power Consumption	V_S = ±15V		75	120		75	120	mW
	V_S = ±3V		4.0	6.0		4.0	6.0	
Offset Adjustment Range	R_{TRIM} = 20 kΩ		±4.0			±4.0		mV

Notes:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. OP-07A is tested fully warmed up.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.
4. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.54 µV.

Electrical Characteristics

(V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			30	75		60	150		60	150	µV
Long Term Input Offset Voltage Stability[3,4]			0.3	1.5		0.4	2.0		0.5	3.0	µV/Mo
Input Offset Current			0.5	3.8		0.8	6.0		0.8	6.0	nA
Input Bias Current			±1.2	±4.0		±1.8	±7.0		±2.0	±12	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.35	0.6		0.38	0.65		0.38	0.65	μV_{p-p}
Input Noise Voltage Density[2]	F_O = 10 Hz		10.3	18		10.5	20		10.5	20	$\frac{nV}{\sqrt{Hz}}$
	F_O = 100 Hz		10	13		10.2	13.5		10.2	13.5	
	F_O = 1000 Hz		9.6	11		9.8	11.5		9.8	11.5	
Input Noise Current[2]	0.1 Hz to 10 Hz		14	30		15	35		15	35	pA_{p-p}
Input Noise Current Density[2]	F_O = 10 Hz		0.32	0.8		0.35	0.9		0.35	0.9	$\frac{pA}{\sqrt{Hz}}$
	F_O = 100 Hz		0.14	0.23		0.15	0.27		0.15	0.27	
	F_O = 1000 Hz		0.12	0.17		0.13	0.18		0.13	0.18	
Input Resistance (Differential Mode)[3]		15	50		8.0	335		7.0	31		MΩ
Input Resistance (Common Mode)			160			120			120		GΩ
Input Voltage Range		±13	±14		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	106	123		100	120		94	110		dB
Power Supply Rejection Ratio	V_S = ± 3V to ±18V	94	107		90	104		90	104		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10V	200	500		1200	400		120	400		V/mV
Large Signal Voltage Gain[3]	$R_L \geq 500$ kΩ, V_{OUT}										
	= ± 0.5V, V_S = ± 3V	150	500		100	400			400		V/mV
Output Voltage Swing	RL ≥ 10 kΩ	±12.5	±13		±12	±13		±12	±13		V
	$R_L \geq 2$ kΩ	±12	±12.8		±11.5	±12.8		±11.5	±12.8		
	$R_L \geq 1$ kΩ	±10.5	±12		±12						
Slew Rate	$R_l \geq 2$ kΩ	0.1	0.3		0.1	0.3		0.1	0.3		V/µS
Unity Gain Bandwidth	A_{VCL} = +1.0	0.8			0.8			0.8			MHz
Open Loop Output Resistance	V_{OUT} = 0, I_{OUT} = 0		60			60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		75	120		80	150		80	150	mW
	V_S = ± 3V, R_L = ∞		4.0	6.0		4.0	8.0		4.0	8.0	
Offset Adjustment Range	R_{TRIM} = 20 kΩ		±4.0			±4.0			±4.0		mV

Linear

Electrical Characteristics (V_S = ±15V, -55°C ≤ T_A ≤+125°C unless otherwise noted)

Parameters	Test Conditions	OP-07A			OP-07B			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			25	60		60	200	µV
Average Input Offset Voltage Drift without External Trim[1]			0.2	0.6		0.3	1.3	µV/°C
With External Trim[3]	R_{TRIM} = 20 kΩ		0.2	0.6		0.3	1.3	
Input Offset Current			0.8	4.0		1.2	5.6	nA
Average Input Offset Current Drift[2]			5.0	25		8.0	50	pA/°C
Input Bias Current			±1.0	±4.0		±2.0	±6.0	nA
Average Input Bias Current Drift[2]			8.0	25		13	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM}= ±13V	106	123		106	123		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	94	106		94	106		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	200	400		150	400		V/mV
Output Voltage	R_L ≥ 2 kΩ,	±12	±12.6		±12	±12.6		V

Electrical Characteristics (V_S = ±15V, 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	OP-07E			OP-07C			OP-07D			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			45	130		85	250		85	250	µV
Average Input Offset Voltage Drift without External Trim			0.3	1.3		0.5	1.8		0.7	2.5	µV/°C
With External Trim[3]	R_{TRIM} = 20 kΩ		0.3	1.3		0.4	1.6		0.7	2.5	
Input Offset Current			0.9	5.3		1.6	8.0		1.6	8.0	nA
Average Input Offset Current Drift[2]			8.0	35		12	50		12	50	pA/°C
Input Bias Current			±1.5	±5.5		±2.2	±9.0		±3.0	±14	nA
Average Input Bias Current Drift[2]			13	35		18	50		18	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM}= ±13V	103	123		97	120		94	106		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	90	104		86	100		86	100		dB
Large Signal Voltage Gain	R_L ≥ 2 kΩ, V_{OUT} = ±10V	180	450		100	400		100	400		V/mV
Output Voltage Swing	R_L ≥ 2 kΩ	±12	±12.6		±11	±12.6		±11	±12.6		V

Notes:
1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
2. This parameter is tested on a sample basis only.
3. Guaranteed but not tested.

Digital Nulling Technique

The digital nulling technique involves the Zener diode nulling network of Figure 1. The zener diodes have relatively high breakdown voltages and never operate in the Zener mode. The purpose of the Zeners is to short out resistors R1, 2R1, 4R1, or 8R1 by forcing a high reverse current through the diode to metalize the junction. The input offset voltage can be adjusted by varying the collector resistor ratio. If the difference in the two collector resistors (R_C) is a small increment ΔR_C. V_{OS} can be written as:

$$V_{OS} = V_T \ln \frac{R_C + \Delta R_C}{R_C} = V_T \ln 1 + \frac{\Delta R_C}{R_C}$$

for $\Delta R_C/R_C << 1.0$ $\ln(1+\Delta R_C/R_C) \sim \Delta R_C/R_C$, thus:

$$V_{OS} \approx V_T \frac{\Delta R_C}{R_C}$$

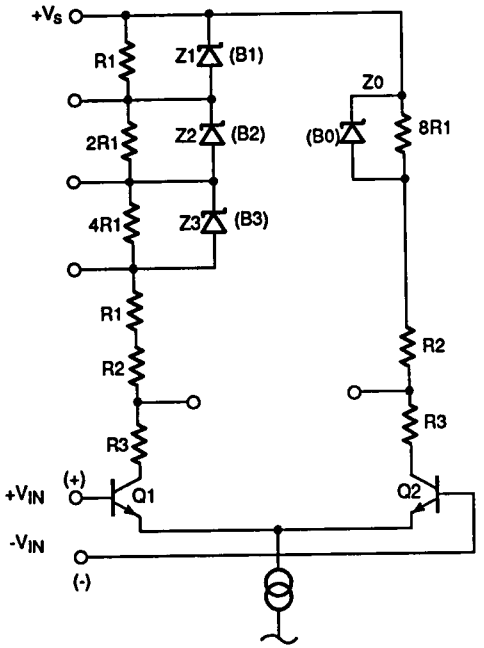
For Figure 1, R2 + R3 >> 8R1, thus

$$V_{OS} \approx V_T \frac{R_1}{8R1 + R2 + R3} (7 - B_3B_2B_1) \qquad (B0 = 1)$$

Or:

$$V_{OS} \approx V_T \frac{R1}{R2 + R3} (1 + B_3B_2B_1) \qquad (B0 = 0)$$

Where $B_3B_2B_1$ is a binary number which corresponds to the state of zener diodes Z1, Z2 and Z3 per Figure 1.



$$\Delta V_{OS}\,(25°C) \approx \frac{-2.6\ \text{mV}\ (7 - B_3B_2B_1)\ R1}{8R1 + R2 + R3} \qquad (B_0 = 1)$$

$B_n = 1$ for Z_n unshorted

$B_n = 0$ for Z_n shorted

$B_3B_2B_1$ = Binary number with values from 0 to 7

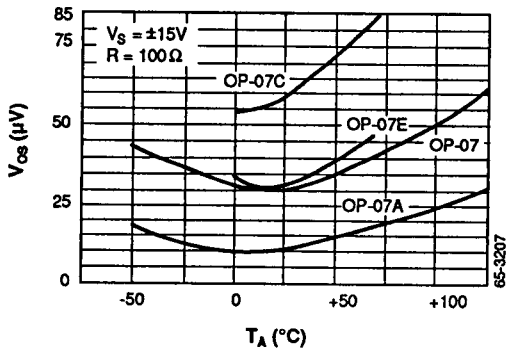
$$\Delta V_{OS}\,(25°C) \approx \frac{2.6\ \text{mV}\ (1 + B_3B_2B_1)\ R1}{R2 + R3} \qquad (B_0 = 0)$$

65-0365

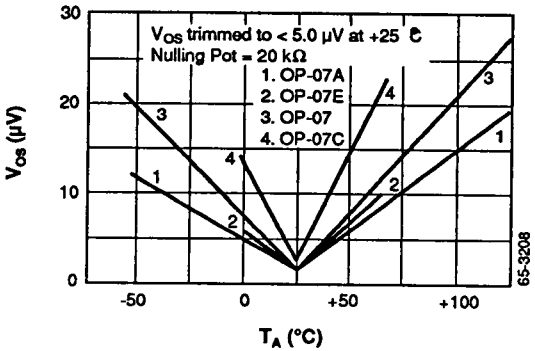
Figure 1. Digital Nulling Network

Typical Performance Characteristics

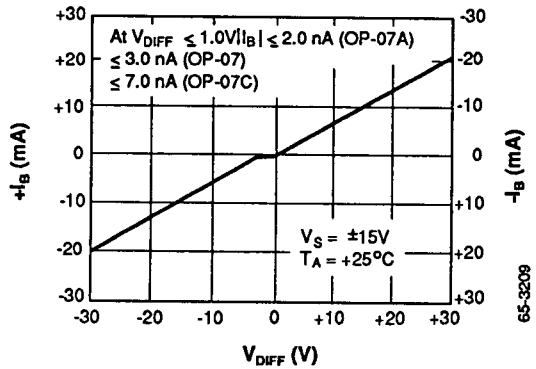
Untrimmed Offset Voltage vs. Temperature



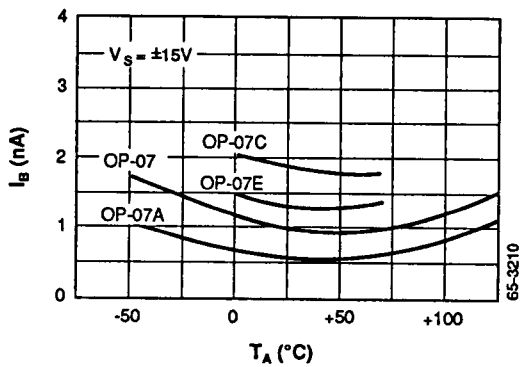
Trimmed Offset Voltage vs. Temperature



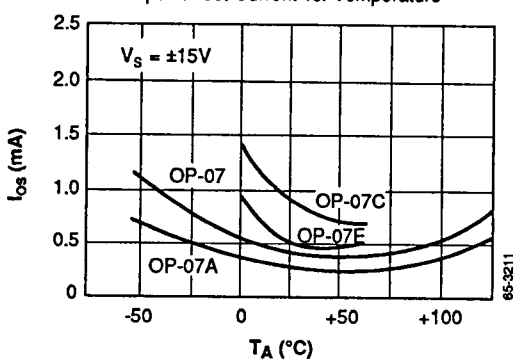
Input Bias Current vs. Differential Input Voltage



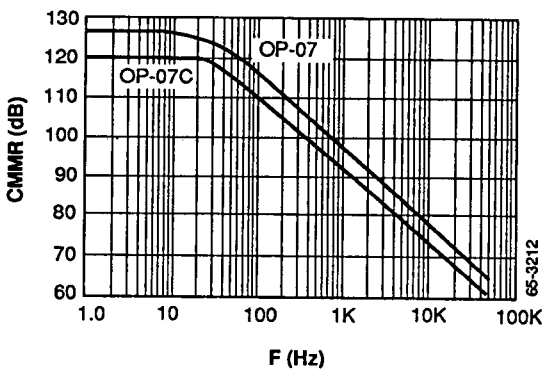
Input Bias Current vs. Temperature



Input Offset Current vs. Temperature

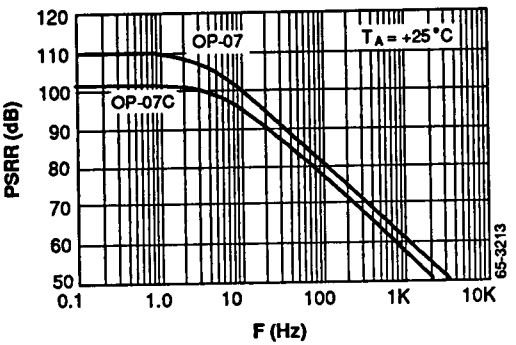


CMRR vs. Frequency

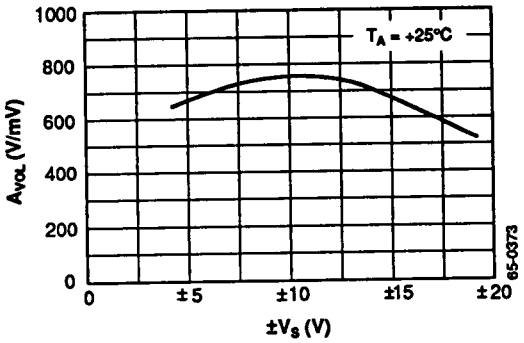


Typical Performance Characteristics

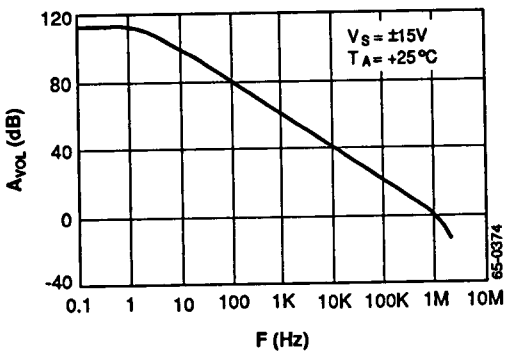
PSRR vs. Frequency



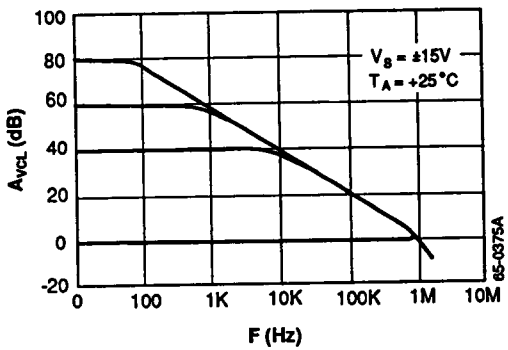
Open Loop Gain vs. Supply Voltage



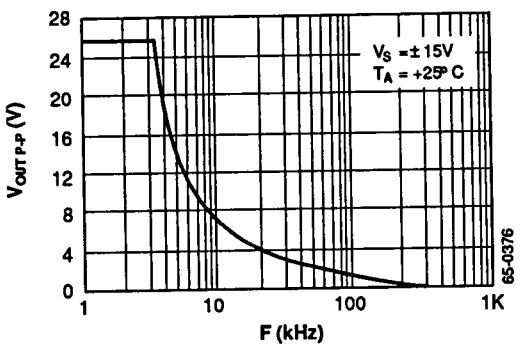
Open Loop Gain vs. Frequency



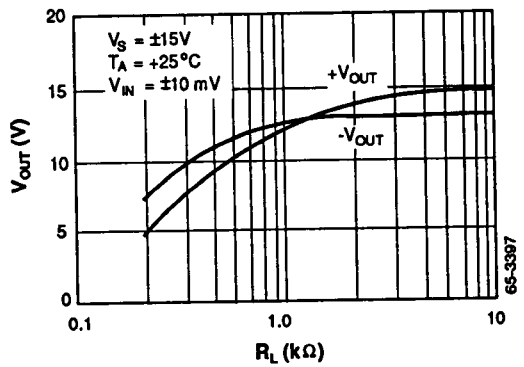
Closed Loop Response for Various Gain Configurations



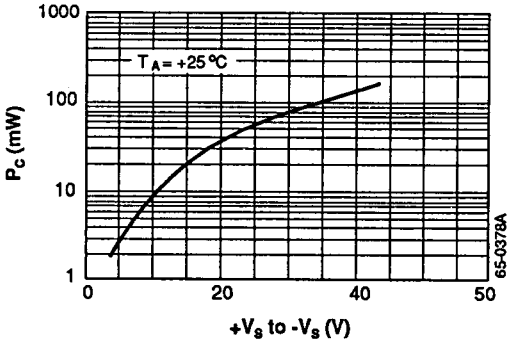
Maximum Undistorted Input vs. Frequency

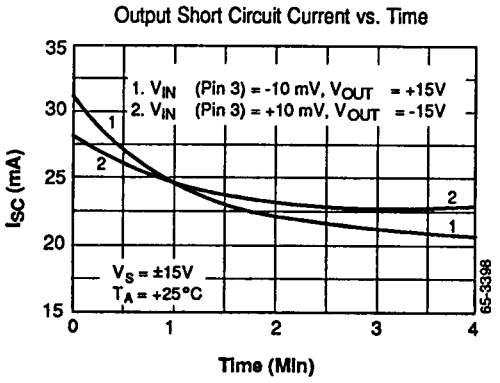


Output Voltage vs. Load Resistance to Ground

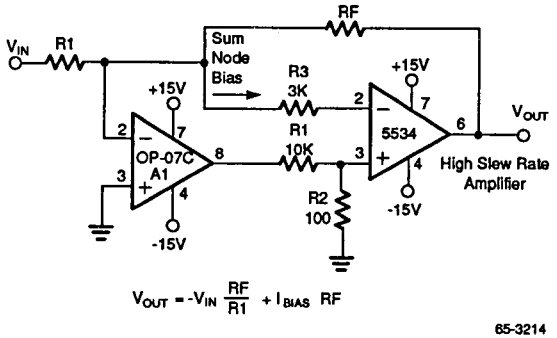


Typical Performance Characteristics

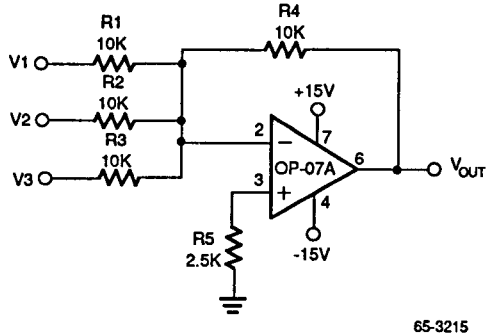




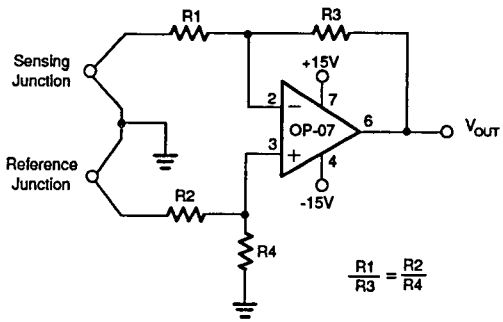
Typical Applications



High Speed, Low V_{OS} Composite Amplifier



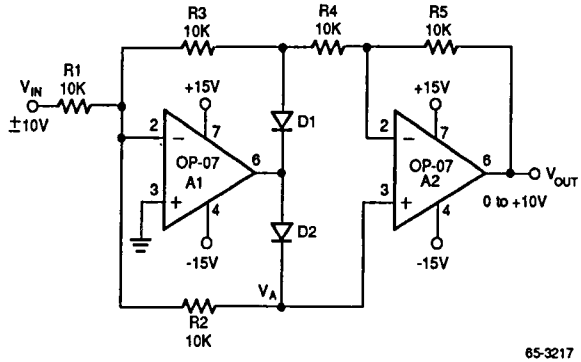
Adjustment-Free Precision Summing Amplifier



Note: Pin numbers shown are for 8-lead packages.

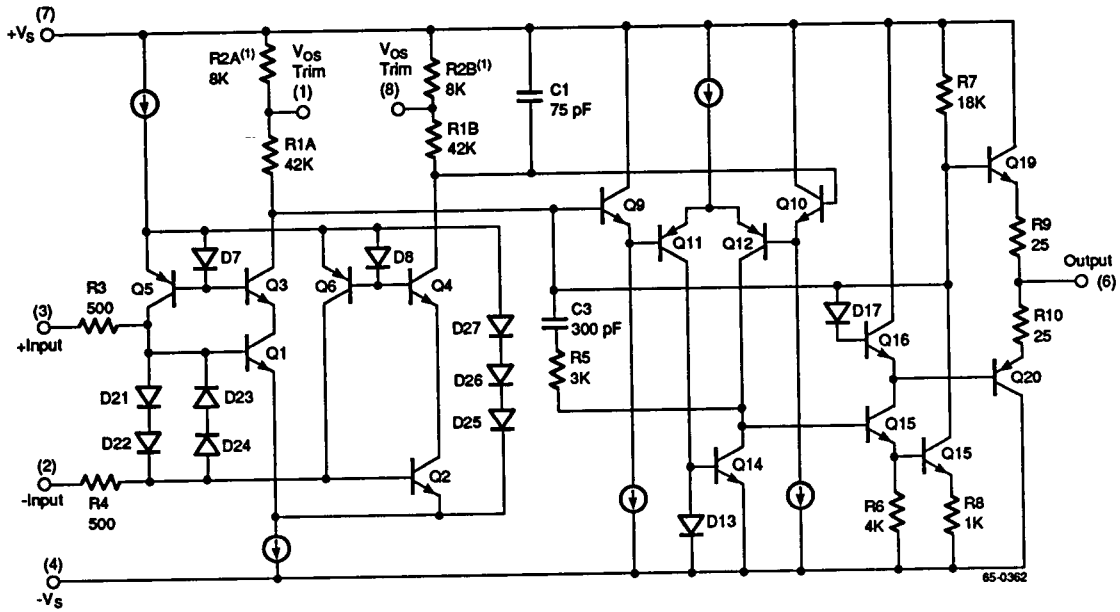
65-3216

High Stability Thermocouple Amplifier



Precision Absolute Value Circuit

Schematic Diagram



Notes:

1. R2A and R2B are electronically adjusted during factory test for minium Vos.
2. Pin numbers shown are for 8-lead packages.