

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4028B **MSI** 1-of-10 decoder

Product specification
File under Integrated Circuits, IC04

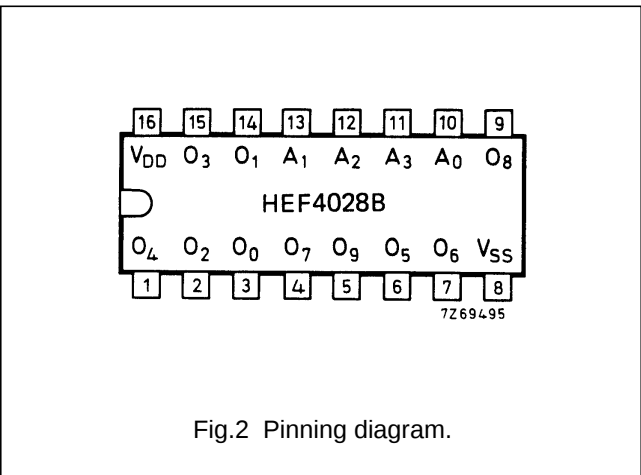
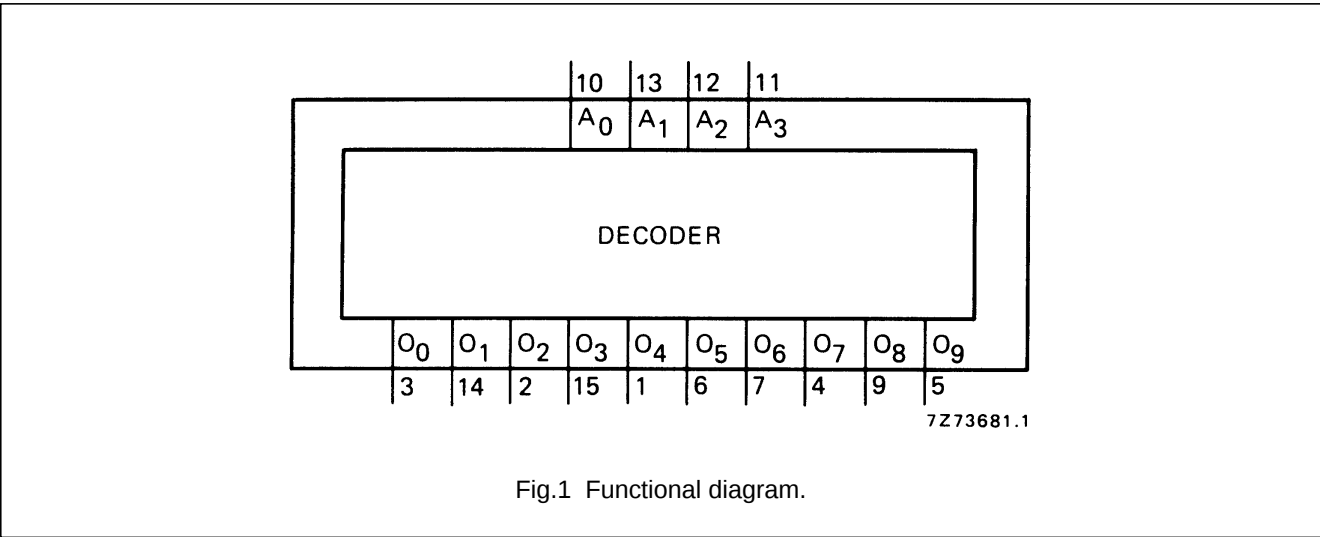
January 1995

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DESCRIPTION

The HEF4028B is a 4-bit BCD to 1-of-10 active HIGH decoder. A 1-2-4-8 BCD code applied to inputs A₀ to A₃ causes the selected output to be HIGH, the other nine will be LOW. If desired, the device may be used as a 1-of-8 decoder with enable; 3-bit octal inputs are applied to inputs A₀, A₁ and A₂ selecting an output O₀ to O₇. Input A₃ then becomes an active LOW enable, forcing the selected output LOW when A₃ is HIGH. The HEF4028B may also be used as an 8-output (O₀ to O₇) demultiplexer with A₀ to A₂ as address inputs and A₃ as an active LOW data input. The outputs are fully buffered for best performance.



- HEF4028BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4028BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4028BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

- A₀ to A₃ address inputs, 1-2-4-8 BCD
- O₀ to O₉ outputs (active HIGH)

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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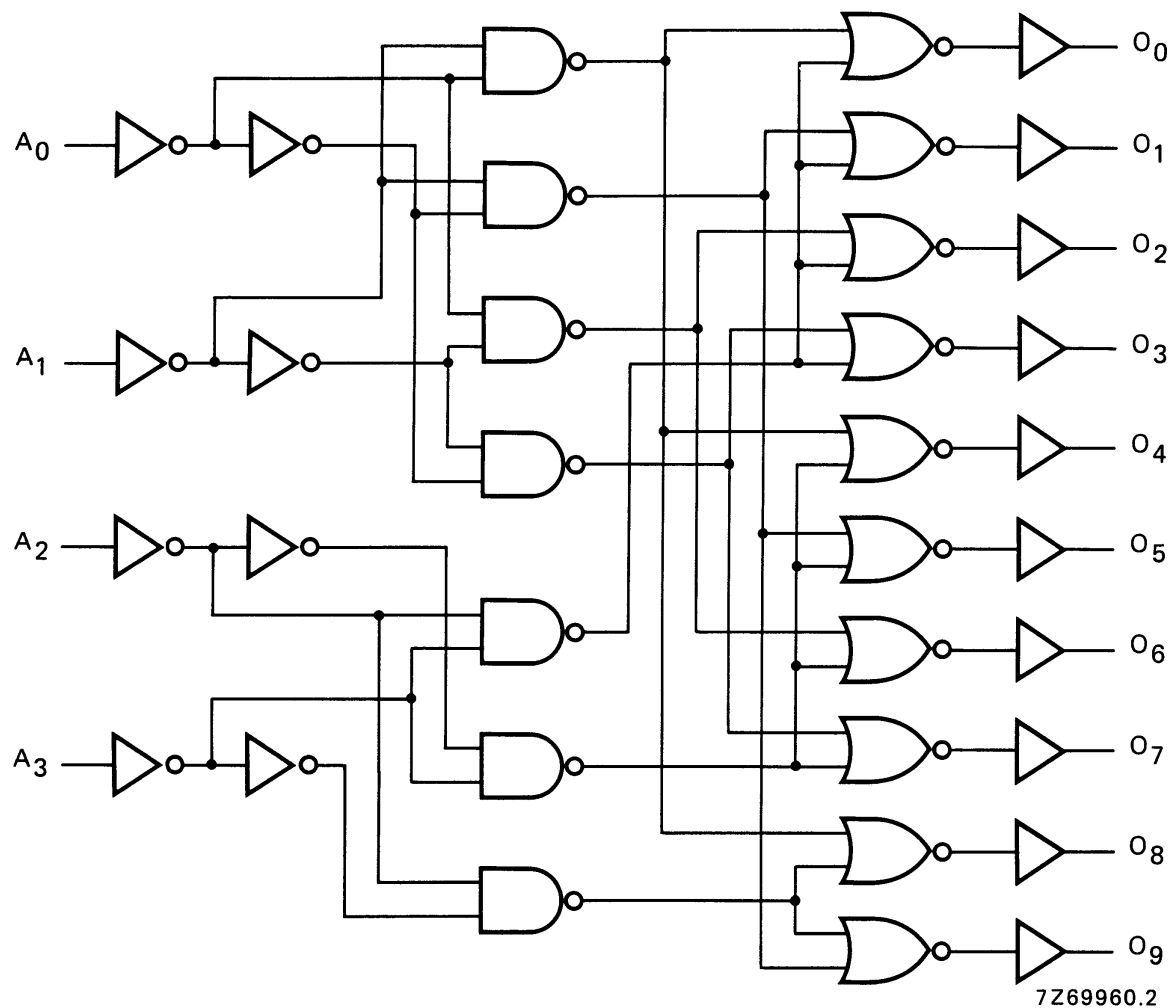
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Fig.3 Logic diagram.

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TRUTH TABLE

INPUTS				OUTPUTS									
A ₃	A ₂	A ₁	A ₀	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	O ₈	O ₉
L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	L	L	H	L	H	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	H	L	L	L	H	L	L	L	L	L	L
L	H	L	L	L	L	L	L	H	L	L	L	L	L
L	H	L	H	L	L	L	L	L	H	L	L	L	L
L	H	H	L	L	L	L	L	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L	L	L	H	L	L
H	L	L	L	L	L	L	L	L	L	L	L	H	L
H	L	L	H	L	L	L	L	L	L	L	L	L	H
H	L	H	L	L	L	L	L	L	L	L	L	L	L
H	L	H	H	L	L	L	L	L	L	L	L	L	L
H	H	L	L	L	L	L	L	L	L	L	L	L	L
H	H	L	H	L	L	L	L	L	L	L	L	L	L
H	H	H	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	L	L	L	L	L	L	L	L	L	L

(2)

Notes

1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
2. Extraordinary states.

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AC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $A_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	100	200	ns	73 ns + (0,55 ns/pF) C_L
	10		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5	t_{PLH}	90	180	ns	63 ns + (0,55 ns/pF) C_L
	10		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
Output transition times HIGH to LOW	5	t_{THL}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L
	5	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$350 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = total load cap. (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2\,200 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$7\,350 f_i + \sum (f_o C_L) \times V_{DD}^2$	