

DATA SHEET

74ALVC16244/74ALVCH16244 2.5V/3.3V 16-bit buffer/line driver (3-State)

Product specification
Supersedes data of 1997 Mar 21
IC24 Data Handbook

1998 Jun 29

16-bit buffer/line driver (3-State)

**74ALVC16244/
74ALVCH16244**

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Bus hold on data inputs (74ALVCH16244 only)
- Output drive capability 50Ω transmission lines @ 85°C
- Current drive ±24 mA at 3.0 V

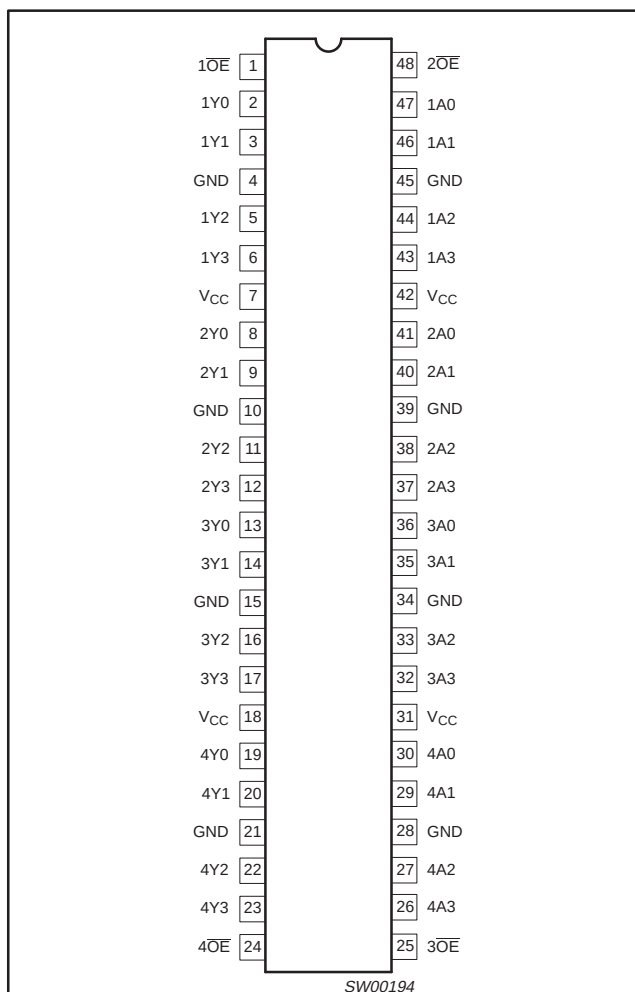
DESCRIPTION

The 74ALVC16244(74ALVCH16244) is a 16-bit non-inverting buffer/line driver with 3-State outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-State outputs are controlled by the output enable inputs 1OE and 2OE. A HIGH on nOE causes the outputs to assume a high impedance OFF-state.

The 74ALVCH16244 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

The 74ALVC16244 has 5V tolerant inputs.

PIN CONFIGURATION



QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_r = t_f ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t _{PHL} /t _{PLH}	Propagation delay An to Yn	V _{CC} = 2.5V, CL = 30pF V _{CC} = 3.3V, CL = 50pF		1.9 1.9	ns
C _I	Input capacitance			5.0	pF
C _{PD}	Power dissipation capacitance per buffer	V _I = GND to V _{CC} ¹	Outputs enabled	25	pF
			Outputs disabled	4	

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
P_D = C_{PD} × V_{CC}² × f_i + Σ (C_L × V_{CC}² × f_o) where: f_i = input frequency in MHz; C_L = output load capacitance in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V; Σ (C_L × V_{CC}² × f_o) = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	−40°C to +85°C	74ALVC16244 DL	AC16244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74ALVC16244 DGG	AC16244 DGG	SOT362-1
48-Pin Plastic SSOP Type III	−40°C to +85°C	74ALVCH16244 DL	ACH16244 DL	SOT370-1
48-Pin Plastic TSSOP Type II	−40°C to +85°C	74ALVCH16244 DGG	ACH16244 DGG	SOT362-1

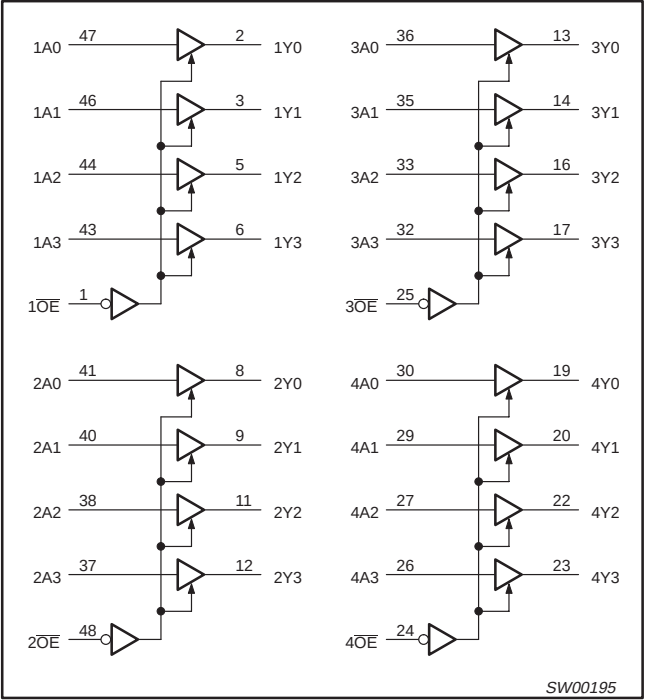
16-bit buffer/line driver (3-State)

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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	1OE	Output enable input (active LOW)
2, 3, 5, 6	1Y0 to 1Y3	Data outputs
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	VCC	Positive supply voltage
8, 9, 11, 12	2Y0 to 2Y3	Data outputs
13, 14, 16, 17	3Y0 to 3Y3	Data outputs
19, 20, 22, 23	4Y0 to 4Y3	Data outputs
24	4OE	Output enable input (active LOW)
25	3OE	Output enable input (active LOW)
30, 29, 27, 26	4A0 to 4A3	Data inputs
36, 35, 33, 32	3A0 to 3A3	Data inputs
41, 40, 38, 37	2A0 to 2A3	Data inputs
47, 46, 44, 43	1A0 to 1A3	Data inputs
48	2OE	Output enable input (active LOW)

LOGIC SYMBOL

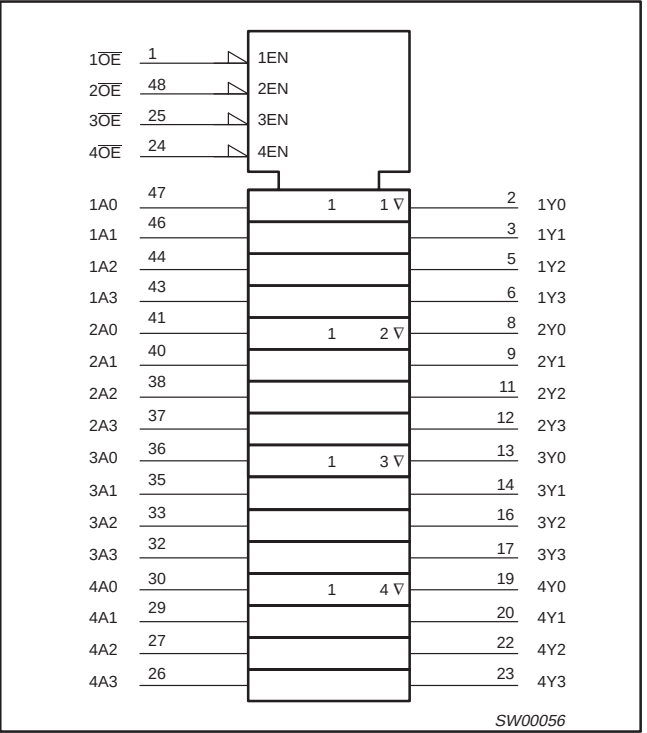


FUNCTION TABLE

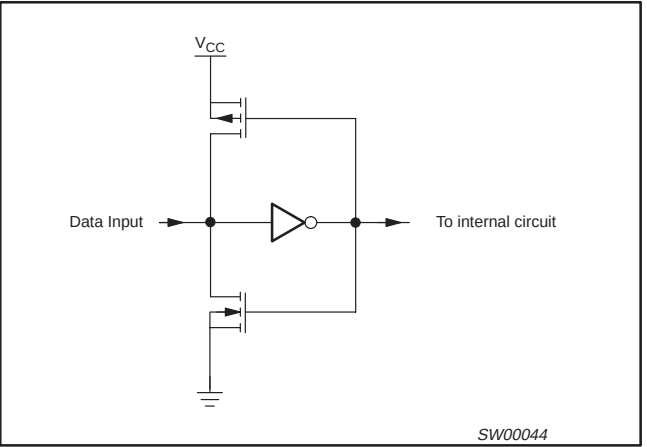
INPUTS		OUTPUT
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



16-bit buffer/line driver (3-State)

74ALVC16244/
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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC Input voltage range	For data input pins with bus hold	0	V_{CC}	V
		For data input pins without bus hold	0	5.5	
		For control pins	0	5.5	
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		-40	+85	°C
t_r, t_f	Input rise and fall times	$V_{CC} = 2.3$ to 3.0 V $V_{CC} = 3.0$ to 3.6 V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	For data inputs with bus hold ²	-0.5 to $V_{CC} + 0.5$	V
		For data inputs without bus hold ²	-0.5 to +5.5	
		For control pins ²	-0.5 to +5.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage	Note 2	-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current	$V_O = 0$ to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		-65 to +150	°C
P_{TOT}	Power dissipation per package	For temperature range: -40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	850	mW
	-plastic medium-shrink (SSOP) -plastic thin-medium-shrink (TSSOP)		600	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

16-bit buffer/line driver (3-State)

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DC CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 1.8V	0.7*V _{CC}	0.9		
		V _{CC} = 2.3 to 2.7V	1.7	1.2		
		V _{CC} = 2.7 to 3.6V	2.0	1.5		
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 1.8V		0.9	0.2*V _{CC}	
		V _{CC} = 2.3 to 2.7V		1.2	0.7	
		V _{CC} = 2.7 to 3.6V		1.5	0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 1.8 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = -100μA	V _{CC} -0.2	V _{CC}		V
		V _{CC} = 1.8V; V _I = V _{IH} or V _{IL} ; I _O = -6mA	V _{CC} -0.4	V _{CC} -0.10		
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -6mA	V _{CC} -0.3	V _{CC} -0.08		
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} -0.5	V _{CC} -0.17		
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} -0.6	V _{CC} -0.26		
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} -0.5	V _{CC} -0.14		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} -1.0	V _{CC} -0.28		
V _{OL}	LOW level output voltage	V _{CC} = 1.8 to 3.6V; V _I = V _{IH} or V _{IL} ; I _O = 100μA		GND	0.20	V
		V _{CC} = 1.8V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.09	0.30	
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 6mA		0.07	0.20	
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.15	0.40	
		V _{CC} = 2.3V; V _I = V _{IH} or V _{IL} ; I _O = 18mA		0.23	0.60	
		V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA		0.14	0.40	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA		0.27	0.55	
I _I	Input leakage current per data pin with bus hold	V _{CC} = 1.8 to 3.6V; V _I = V _{CC} or GND		0.1	5	μA
	Input leakage current per data pin without bus hold	V _{CC} = 1.8 to 3.6V; V _I = 5.5 V or GND		0.1	5	
	Input leakage current per control pin	V _{CC} = 1.8 to 3.6V; V _I = 5.5 V or GND		0.1	5	
I _{IHZ} /I _{ILZ}	Input current for common I/O pins	V _{CC} = 1.8 to 2.7V; V _I = V _{CC} or GND		0.1	10	μA
		V _{CC} = 3.6V; V _I = V _{CC} or GND		0.1	15	
I _{OZ}	3-State output OFF-state current	V _{CC} = 1.8 to 2.7V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	5	μA
		V _{CC} = 2.7 to 3.6V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND		0.1	10	
I _{CC}	Quiescent supply current	V _{CC} = 1.8 to 2.7V; V _I = V _{CC} or GND; I _O = 0		0.1	20	μA
		V _{CC} = 2.3 to 3.6V; V _I = V _{CC} or GND; I _O = 0		0.2	40	
ΔI _{CC}	Additional quiescent supply current given per data I/O pin with bus hold	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		150	750	μA
	Additional quiescent supply current given per data I/O pin without bus hold			5	500	
	Additional quiescent supply current given per control pin			5	500	

16-bit buffer/line driver (3-State)

74ALVC16244/
74ALVCH16244**DC ELECTRICAL CHARACTERISTICS (Continued)**

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
I _{BHL} ²	Bus hold LOW sustaining current	V _{CC} = 2.3V; V _I = 0.7V	45	—		μA
		V _{CC} = 3.0V; V _I = 0.8V	75	150		
I _{BHH} ²	Bus hold HIGH sustaining current	V _{CC} = 2.3V; V _I = 1.7V	–45			μA
		V _{CC} = 3.0V; V _I = 2.0V	–75	–175		
I _{BHLO} ²	Bus hold LOW overdrive current	V _{CC} = 2.7V	300			μA
		V _{CC} = 3.6V	450			
I _{BHHO} ²	Bus hold HIGH overdrive current	V _{CC} = 2.7V	–300			μA
		V _{CC} = 3.6V	–450			

NOTES:

1. All typical values are at $T_{amb} = 25^{\circ}C$.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR $V_{CC} = 2.3V$ TO $2.7V$ RANGE AND $V_{CC} < 2.3V$ GND = 0V; $t_r = t_f \leq 2.0ns$; $C_L = 30pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			$V_{CC} = 2.3$ to $2.7V$			$V_{CC} = 1.8V$			$V_{CC} = 1.2V$	
			MIN	TYP ^{1, 2}	MAX	MIN	TYP ¹	MAX	TYP ¹	
t_{PHL}/t_{PLH}	Propagation delay nAn to nYn	1, 3	1.0	1.9	3.7	1.5	2.8	5.1	5.8	ns
t_{PZH}/t_{PZL}	3-State output enable time nOE to nYn	2, 3	1.0	2.5	4.9	1.5	3.8	7.1	8.4	ns
t_{PHZ}/t_{PLZ}	3-State output disable time nOE to nYn	2, 3	1.0	2.1	4.1	1.5	3.1	3.5	5.9	ns

NOTES:

1. All typical values are measured at $T_{amb} = 25^{\circ}C$.
2. Typical value is measured at $V_{CC} = 2.5V$

AC CHARACTERISTICS FOR $V_{CC} = 3.0V$ TO $3.6V$ RANGE AND $V_{CC} = 2.7V$ GND = 0V; $t_r = t_f \leq 2.5ns$; $C_L = 50pF$

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V _{CC} = 3.3 ± 0.3V			V _{CC} = 2.7V			
			MIN	TYP ^{1, 2}	MAX	MIN	TYP ¹	MAX	
t _{PHL} /t _{PLH}	Propagation delay nAn to nYn	1, 3	1.0	1.9	3.0	1.0	2.1	3.6	ns
t _{PZH} /t _{PZL}	3-State output enable time nOE to nYn	2, 3	1.0	2.3	4.0	1.0	2.9	4.9	ns
t _{PHZ} /t _{PLZ}	3-State output disable time nOE to nYn	2, 3	1.0	2.7	4.1	1.0	3.0	4.5	ns

NOTES:

1. All typical values are measured at $T_{amb} = 25^{\circ}C$.
2. Typical value is measured at $V_{CC} = 3.3V$

16-bit buffer/line driver (3-State)

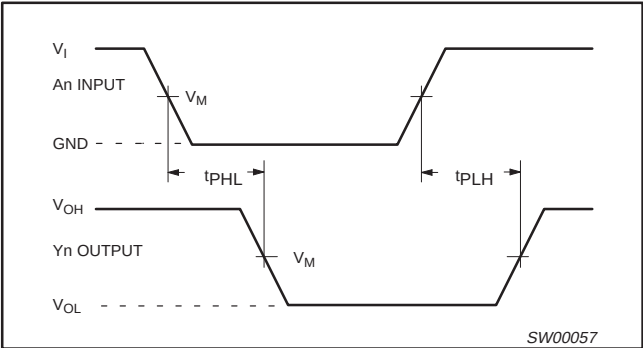
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AC WAVEFORMS FOR $V_{CC} = 2.3V$ TO $2.7V$ AND $V_{CC} < 2.3V$ RANGE

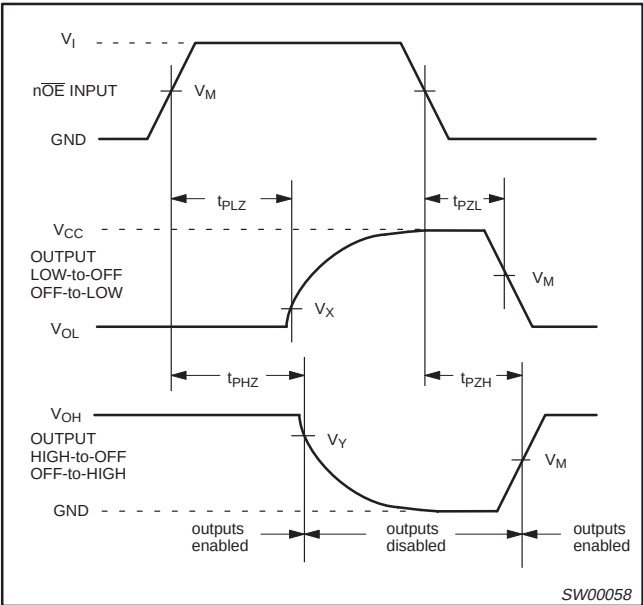
$V_M = 0.5 V_{CC}$
 $V_X = V_{OL} + 0.15V$
 $V_Y = V_{OH} - 0.15V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = V_{CC}$

AC WAVEFORMS FOR $V_{CC} = 3.0V$ TO $3.6V$ AND $V_{CC} = 2.7V$ RANGE

$V_M = 1.5 V$
 $V_X = V_{OL} + 0.3V$
 $V_Y = V_{OH} - 0.3V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_I = 2.7V$



Waveform 1. Input (An) to output (Yn) propagation delay times



Waveform 2. 3-State enable and disable times

TEST CIRCUIT

Test Circuit for switching times

DEFINITIONS

R_L = Load resistor
 C_L = Load capacitance includes jig and probe capacitance
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

TEST	S_1	V_{CC}	V_I
t_{PLH}/t_{PHL}	Open	$< 2.7V$	V_{CC}
t_{PLZ}/t_{PZL}	$2 * V_{CC}$	$2.7-3.6V$	$2.7V$
t_{PHZ}/t_{PZH}	GND		

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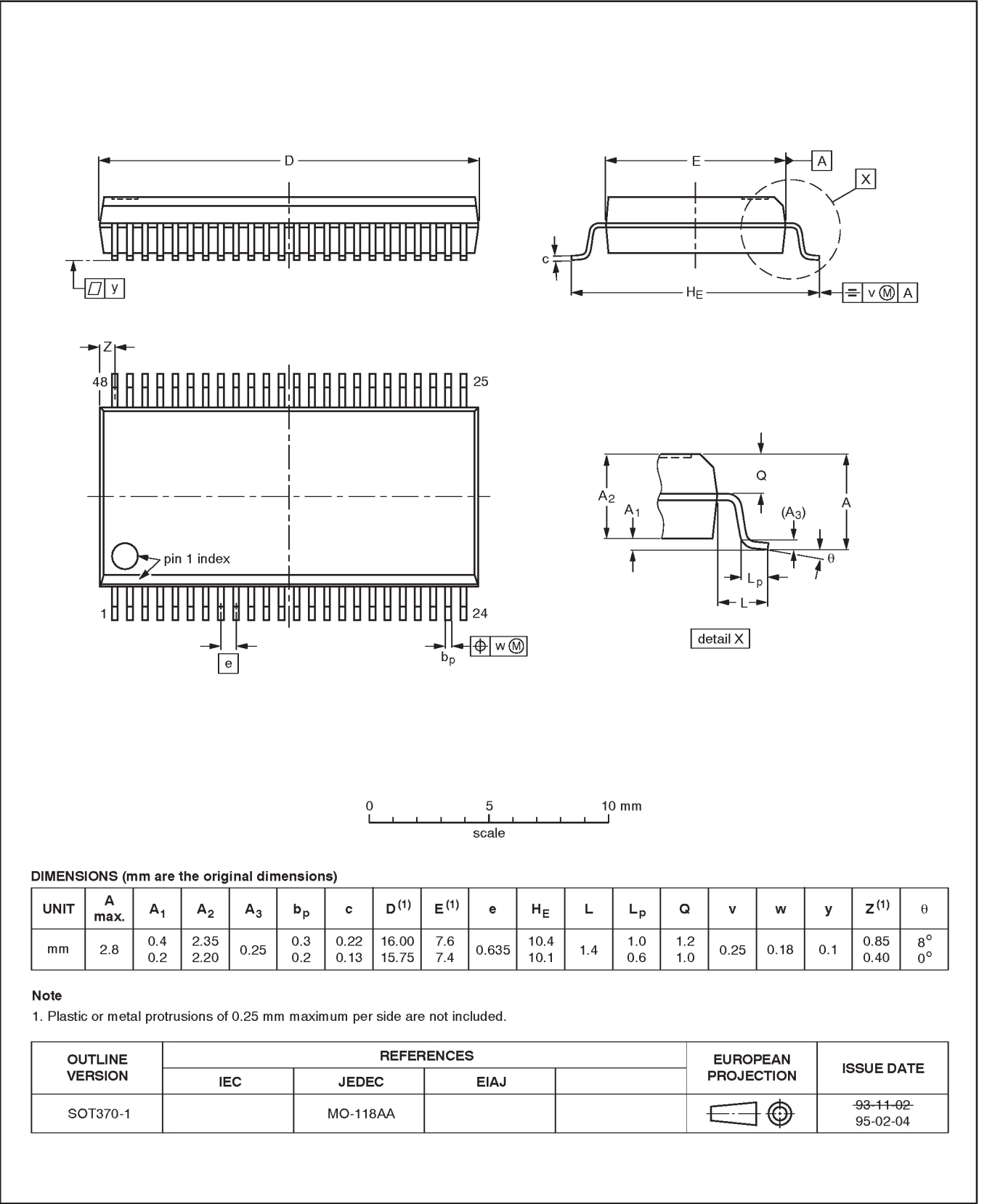
Waveform 3. Load circuitry for switching times

2.5V/3.3V 16-bit buffer/line driver (3-State)

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SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

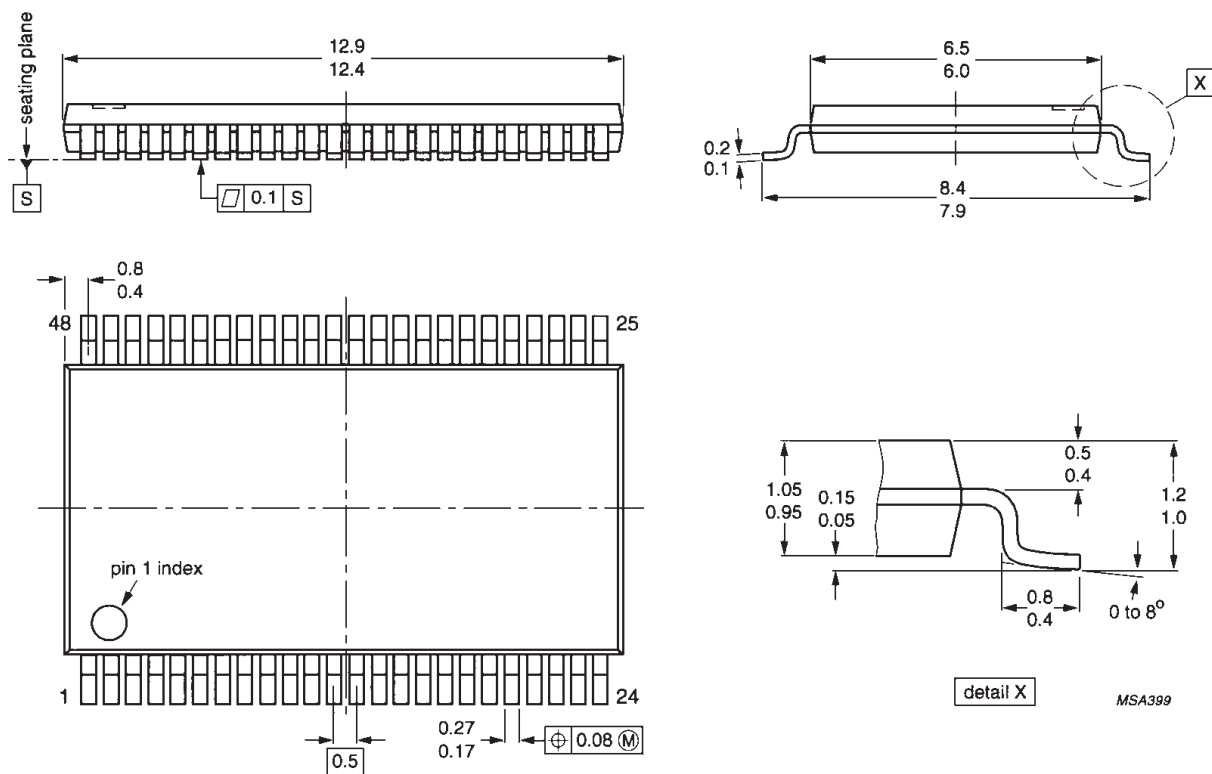


2.5V/3.3V 16-bit buffer/line driver (3-State)

74ALVC16244/
74ALVCH16244

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1



2.5V/3.3V 16-bit buffer/line driver (3-State)

74ALVC16244/
74ALVCH16244

DEFINITIONS		
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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