

DATA SHEET

~~74F175*~~, **74F175A** Quad D flip-flop

* Discontinued part. Please see the Discontinued Product List in Section 1, page 21.

Product specification

1996 Mar 12

IC15 Data Handbook

Quad D flip-flop

74F175A

FEATURES

- Four edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- True and complementary outputs
- Industrial temperature range available (–40°C to +85°C)
- PNP light loading inputs

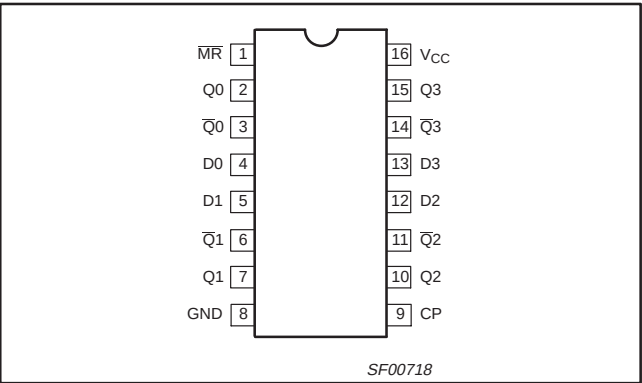
DESCRIPTION

The 74F175A is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independently of clock or data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complementary outputs are required, and the CP and $\overline{MR}$ are common to all storage elements.

PIN CONFIGURATION



TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F175A	160MHz	22mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG. DWG. #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	
16-pin plastic DIP	74F175AN	SOT38-4
16-pin plastic SO	74F175AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION		74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	74F175A	1.0/0.033	20 μ A/20 μ A
$\overline{MR}$	Master reset input (active–Low)	74F175A	1.0/0.033	20 μ A/20 μ A
CP	Clock input (active rising edge)	74F175A	1.0/0.033	20 μ A/20 μ A
Q0–Q3	True outputs		50/33	1.0mA/20mA
$\overline{Q0}$ – $\overline{Q3}$	Complementary outputs		50/33	1.0mA/20mA

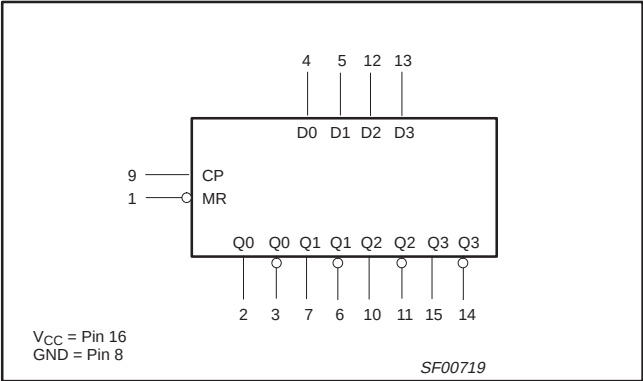
NOTE:

One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

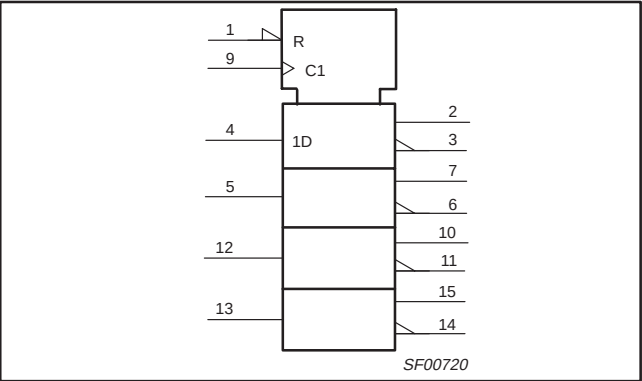
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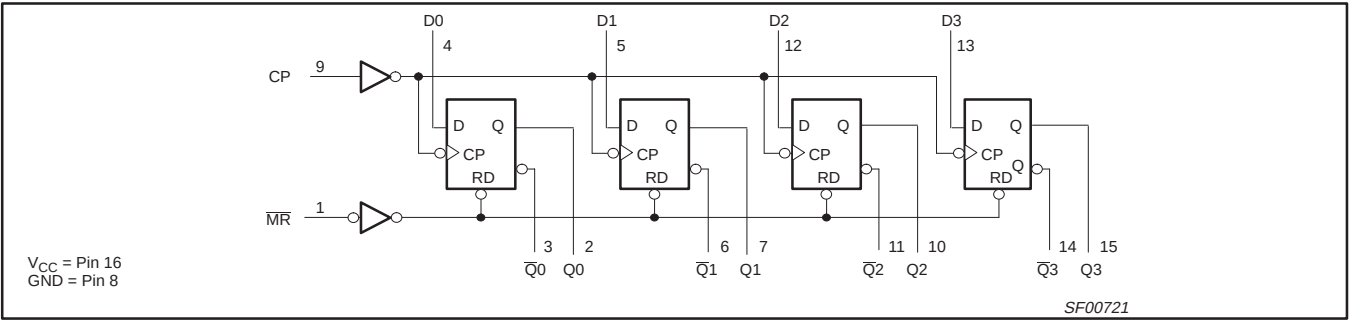
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS		OPERATING MODE
MR	CP	D _n	Q _n	$\bar{Q}_n$	
L	X	X	L	H	Reset (clear)
H	↑	h	H	L	Load "1"
H	↑	l	L	H	Load "0"

H = High voltage level
h = High state must be present one setup time before the Low-to-High clock transition
L = Low voltage level
l = Low state must be present one setup time before the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		−0.5 to +7.0	V
V _{IN}	Input voltage		−0.5 to +7.0	V
I _{IN}	Input current		−30 to +5	mA
V _{OUT}	Voltage applied to output in High output state		−0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state		40	mA
T _{amb}	Operating free air temperature range	Commercial range	0 to +70	°C
		Industrial range	−40 to +85	°C
T _{stg}	Storage temperature range		−65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free air temperature range	Commercial range	0	+70	°C
		Industrial range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			MIN	TYP ²	MAX	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 10\%V_{CC}$	2.5		V
			$\pm 5\%V_{CC}$	2.7	3.4	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.30	V
			$\pm 5\%V_{CC}$		0.30	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V
I_I	Input current at maximum input voltage	$V_{CC} = 0.0V, V_I = 7.0V$			100	μA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$	74F175A		-20	μA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	-60		-150	mA
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}$	74F175A	22	31	mA

Notes to DC electrical characteristics

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS FOR 74F175A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			$T_{amb} = 25^{\circ}C$ $V_{CC} = +5V$ $C_L = 50pF,$ $R_L = 500\Omega$			$T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF,$ $R_L = 500\Omega$		$T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF,$ $R_L = 500\Omega$			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f _{max}	Maximum clock frequency	Waveform 1	140	160		125		110		MHz	
t _{PLH} t _{PHL}	Propagation delay CP to Qn or Q̄n	Waveform 1	3.0 4.5	4.0 6.0	6.5 8.5	2.5 4.0	7.5 9.0	2.5 4.0	8.0 10.0	ns	
t _{PLH} t _{PHL}	Propagation delay MR to Qn	Waveform 3	4.5	6.5	9.0	4.5	10.0	4.5	11.0	ns	
t _{PHL} t _{PHL}	Propagation delay MR to Q̄n	Waveform 3	4.5	6.0	8.0	4.0	9.0	4.0	10.0	ns	

Quad D flip-flop

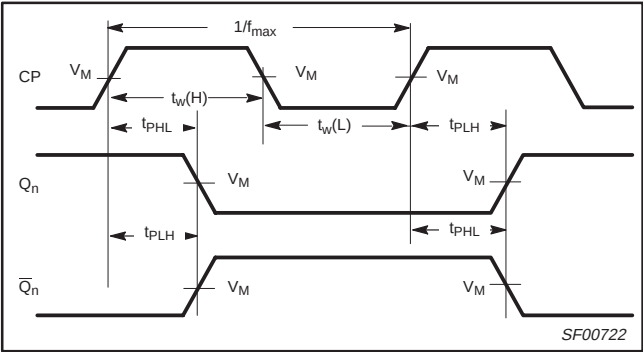
74F175A

AC SETUP REQUIREMENTS FOR 74F175A

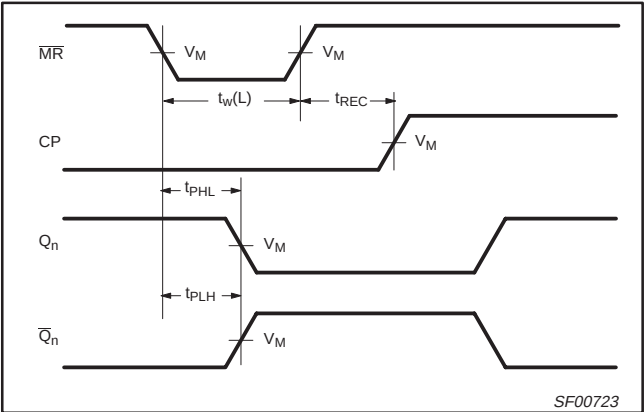
SYMBOL	PARAMETER	TEST CONDITION	LIMITS								UNIT
			T _{amb} = 25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		T _{amb} = −40°C to +85°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t _s (H) t _s (L)	Setup time, High or Low Dn to CP	Waveform 2	3.0 3.0			3.5 3.5		4.0 4.0		ns	
t _h (H) t _h (L)	Hold time, High or Low Dn to CP	Waveform 2	0.0 0.0			0.0 0.0		0.0 0.0		ns	
t _w (H) t _w (L)	CP Pulse width High or Low	Waveform 1	3.0 4.0			3.5 5.0		4.0 5.5		ns	
t _w (L)	$\overline{\text{MR}}$ Pulse width Low	Waveform 3	3.5			3.5		4.0		ns	
t _{REC}	Recovery time $\overline{\text{MR}}$ to CP	Waveform 3	4.0			4.5		5.0		ns	

AC WAVEFORMS

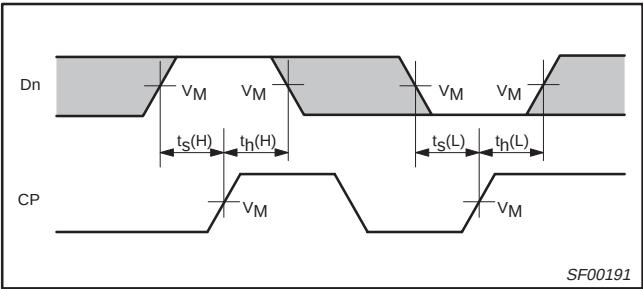
For all waveforms, V_M = 1.3V.



Waveform 1. Propagation delay for clock input to output, clock pulse width, and maximum clock frequency



Waveform 3. Master Reset pulse width, Master Reset to output delay and Master Reset to Clock recovery time

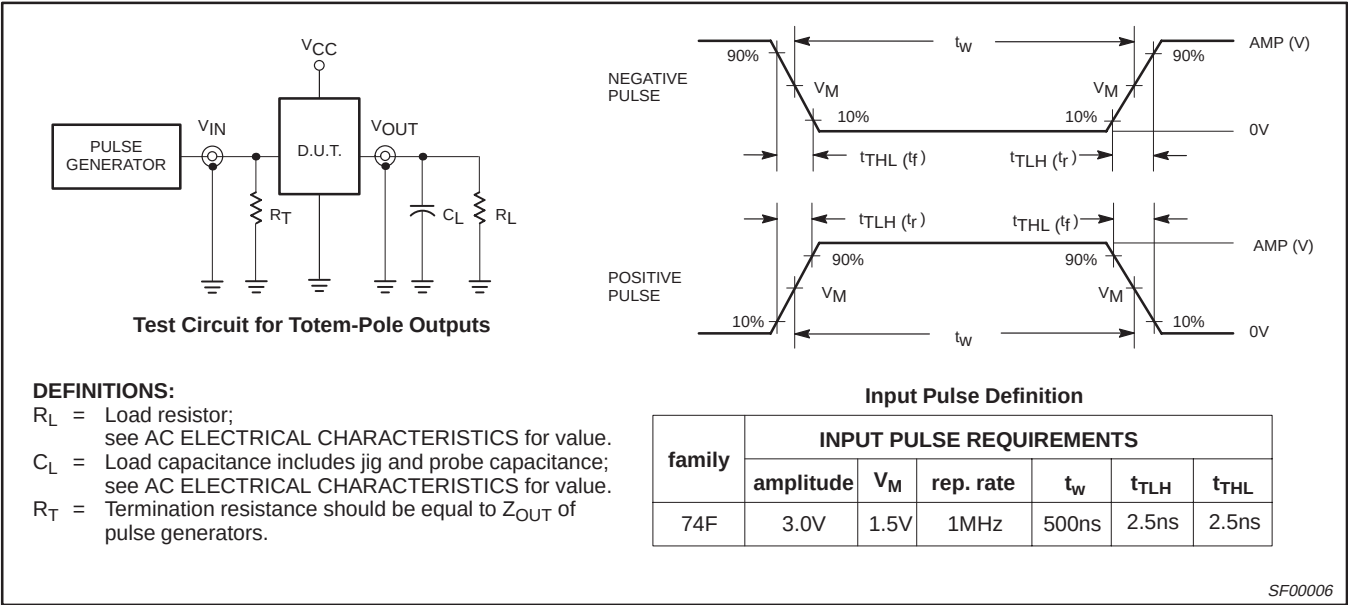


Waveform 2. Data setup time and hold times

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TEST CIRCUIT AND WAVEFORMS

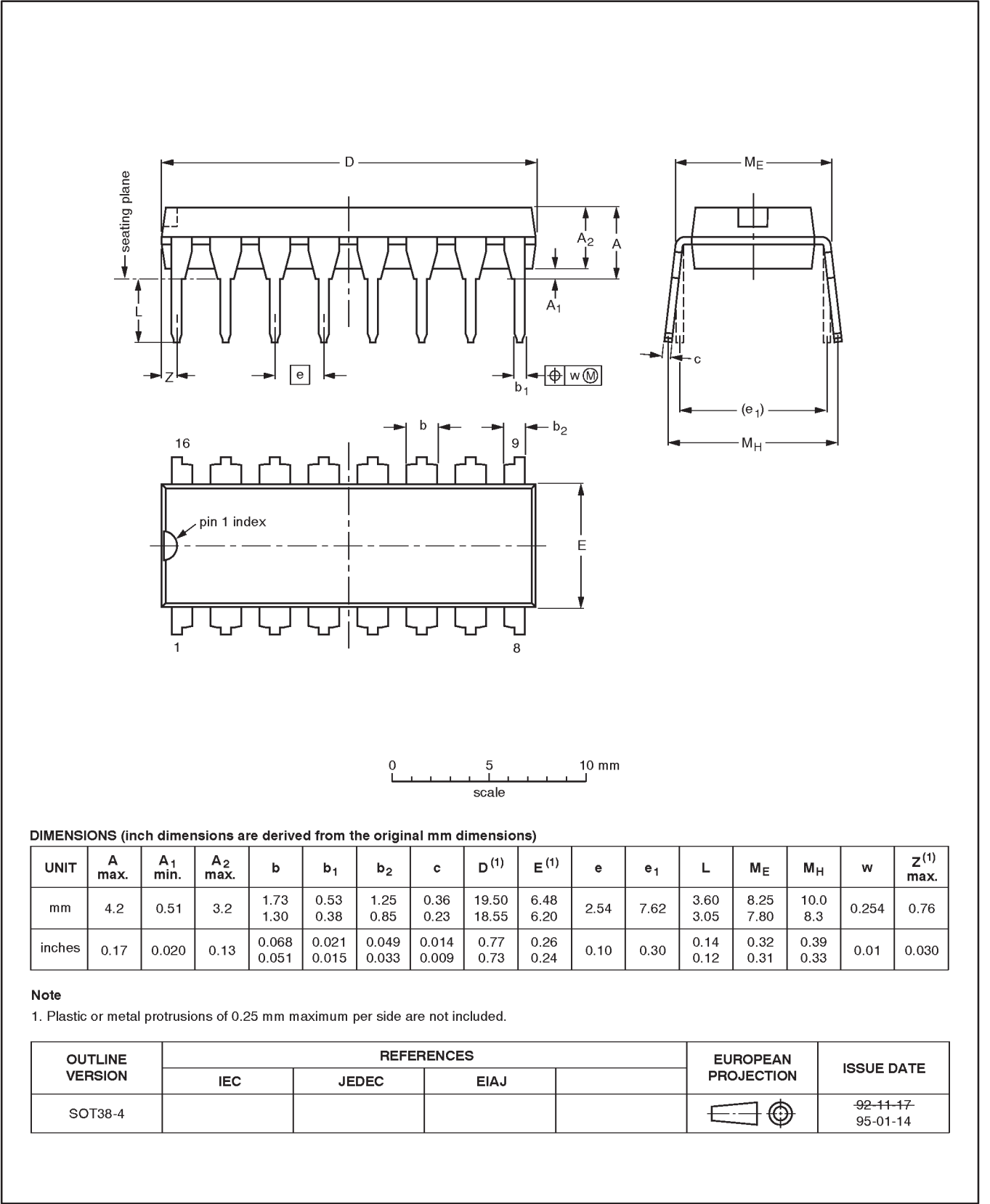


Quad D flip-flop

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

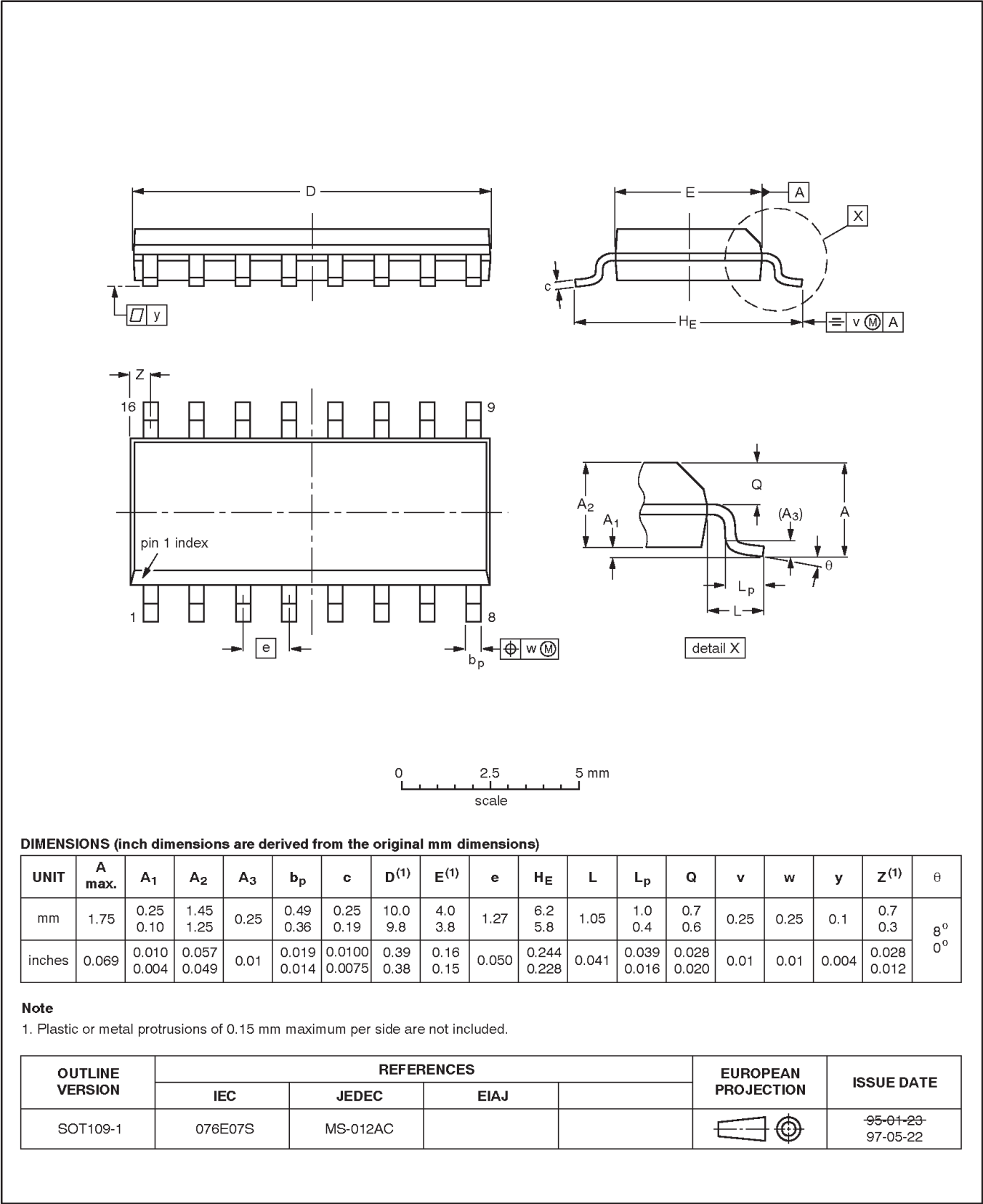


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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Quad D flip-flop

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NOTES

^{*} *Discontinued part. Please see the Discontinued Product List.*

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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