

DATA SHEET

74F194

4-bit bidirectional universal shift register

Product specification

1989 Apr 04

IC15 Data Handbook

4-bit bidirectional universal shift register

74F194

FEATURES

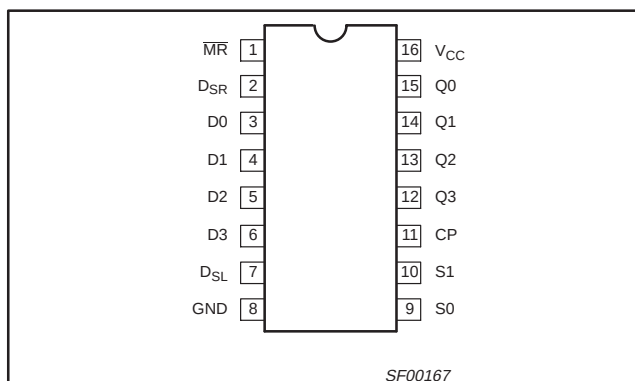
- Shift right and shift left capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

DESCRIPTION

The functional characteristics of the 74F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical) for 74F, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The 74F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S0 and S1. As shown in the Mode Select-Function Table, data can be entered and shifted from left to right (shift right, Q0→Q1, etc.), or right to left (shift left, Q3→Q2, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S0 and S1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation. Mode Select and data inputs on the 74F194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Select and selected data inputs must be stable one setup time prior to the Low-to-High transition of the clock pulse. Signals on the Mode Select, Parallel Data (D0–D3) and Serial Data (D_{SR}, D_{SL}) can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed. The four Parallel Data inputs (D0–D3) are D-type inputs. Data appearing on (D0–D3) inputs when S0 and S1 are High is transferred to the Q0–Q3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F194	150MHz	33mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
16-pin plastic DIP	N74F194N	SOT38-4
16-pin plastic SO	N74F194D	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

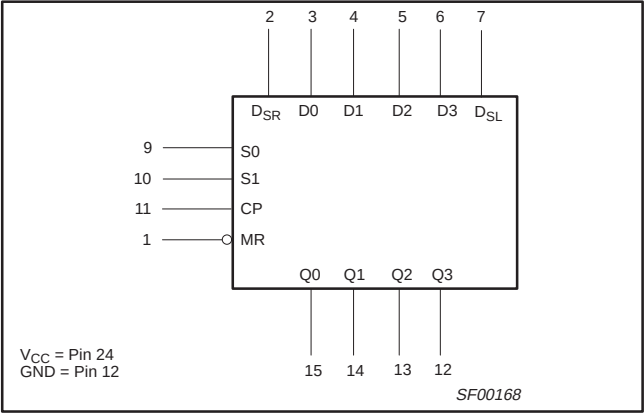
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D3	Parallel data inputs	1.0/1.0	20 μ A/0.6mA
D _{SR}	Serial data input (Shift Right)	1.0/1.0	20 μ A/0.6mA
D _{SL}	Serial data input (Shift Left)	1.0/1.0	20 μ A/0.6mA
S0, S1	Mode Select inputs	1.0/1.0	20 μ A/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20 μ A/0.6mA
$\overline{MR}$	Asynchronous master Reset input (Active Low)	1.0/1.0	20 μ A/0.6mA
Q0–Q3	Data outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

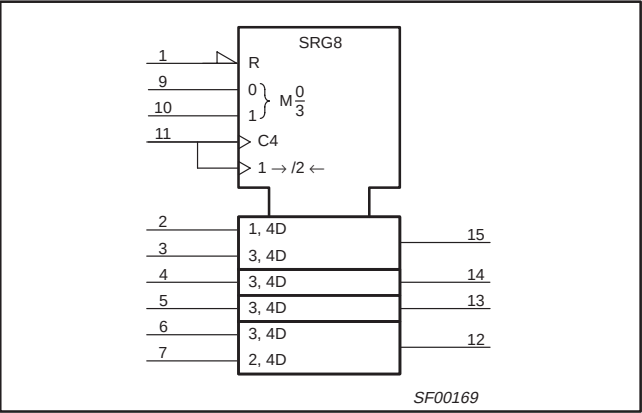
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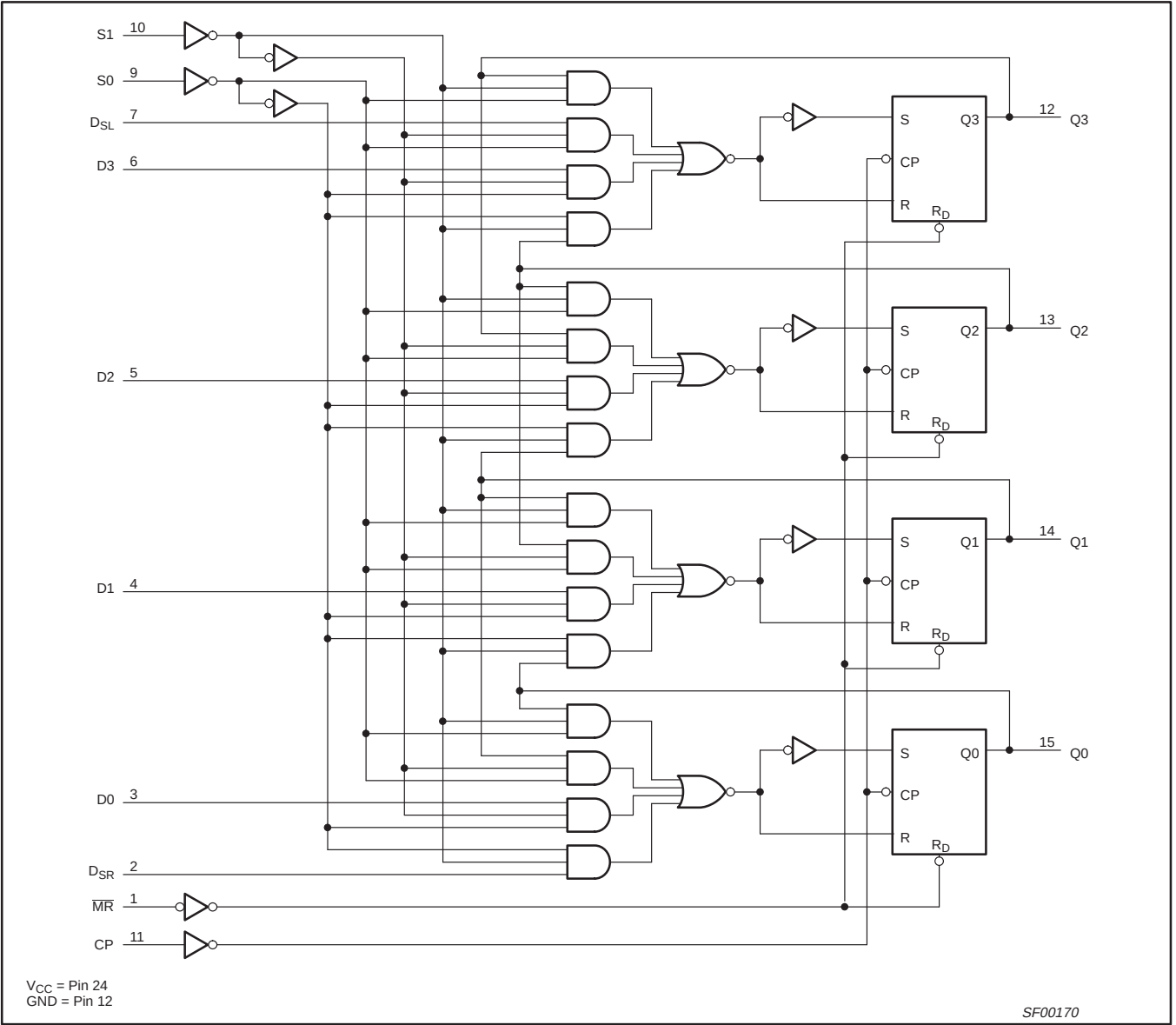
LOGIC SYMBOL



IEC/IEEE SYMBOL



LOGIC DIAGRAM



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FUNCTION TABLE

INPUTS							OUTPUTS				OPERATING MODES
CP	$\overline{MR}$	S1	S0	D _{SR}	D _{SL}	D _n	Q0	Q1	Q2	Q3	
X	L	X	X	X	X	X	L	L	L	L	Reset (clear)
X	H	l	l	X	X	X	q0	q1	q2	q3	Hold (do nothing)
↑	H	h	l	X	l	X	q1	q2	q3	L	Shift left
↑	H	h	l	X	h	X	q1	q2	q3	H	
↑	H	l	h	l	X	X	L	q0	q1	q2	Shift right
↑	H	l	h	h	X	X	H	q0	q1	q2	
↑	H	h	h	X	X	dn	d0	d1	d2	d3	Parallel load

H = High voltage level

h = High voltage level one setup time prior to Low-to-High clock transition

L = Low voltage level

l = Low voltage level one setup time prior to Low-to-High clock transition

X = Don't care

↑ = Low-to-High clock transition

dn(qn) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.)

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	−0.5 to +7.0	V
V _{IN}	Input voltage	−0.5 to +7.0	V
I _{IN}	Input current	−30 to +5	mA
V _{OUT}	Voltage applied to output in High output state	−0.5 to V _{CC}	V
I _{OUT}	Current applied to output in Low output state	40	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			−18	mA
I _{OH}	High-level output current			−1	mA
I _{OL}	Low-level output current			20	mA
T _{amb}	Operating free-air temperature range	0		+70	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT
			MIN	TYP ²	MAX	
V _{OH}	High-level output voltage ³	V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}	2.5		V
		V _{IH} = MIN, I _{OH} = MAX	±5%V _{CC}	2.7	3.4	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX	±10%V _{CC}		0.30	V
		V _{IH} = MIN, I _{OL} = MAX	±5%V _{CC}		0.30	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}		−0.73	−1.2	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			100	μA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V			−0.6	mA
I _{OS}	Short-circuit output current ⁴	V _{CC} = MAX	−60		−150	mA
I _{CC}	Supply current (total) ⁵	V _{CC} = MAX		33	46	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
- Output High state will change to Low state if an external voltage of less than 0.0V is applied.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- With all outputs open, D_i inputs grounded and a 4.5V applied to S0, S1, MR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = +5.0V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	Waveform 1	105	150		90		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Qn	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.5 3.5	8.0 8.0	ns
t _{PHL}	Propagation delay MR to Qn	Waveform 2	4.5	8.6	12.0	4.5	14.0	ns

AC SETUP REQUIREMENTS

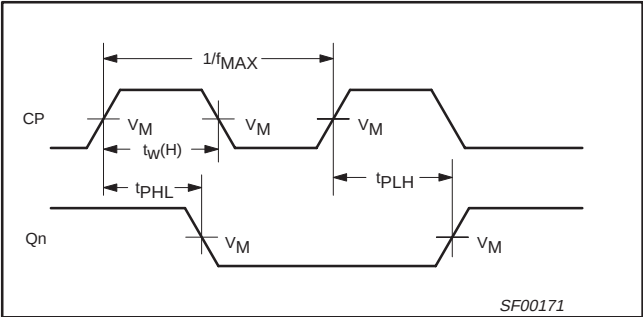
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = +5.0V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = +5.0V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _S (H) t _S (L)	Setup time, High or Low Dn, D _{SL} , D _{SR} to CP	Waveform 3	4.0 4.0			4.0 4.0		ns
t _H (H) t _H (L)	Hold time, High or Low Dn, D _{SL} , D _{SR} to CP	Waveform 3	0 0			1.0 1.0		ns
t _S (H) t _S (L)	Setup time, High or Low Sn to CP	Waveform 3	8.0 8.0			9.0 8.0		ns
t _H (H) t _H (L)	Hold time, High or Low Sn to CP	Waveform 3	0 0			0 0		ns
t _W (H)	CP Pulse width, High	Waveform 1	5.0			5.5		ns
t _W (L)	MR Pulse width, Low	Waveform 2	5.0			5.0		ns
t _{REC}	Recovery time, MR to CP	Waveform 2	7.0			8.0		ns

4-bit bidirectional universal shift register

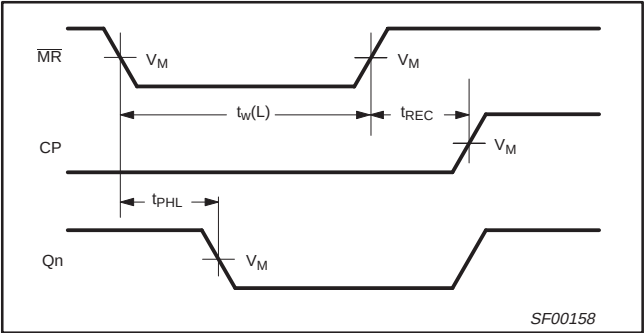
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AC WAVEFORMS

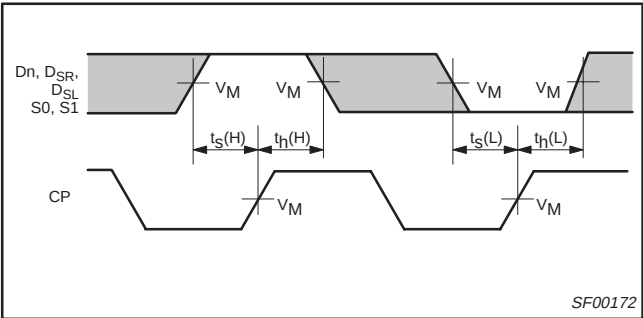
For all waveforms, $V_M = 1.5V$.
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



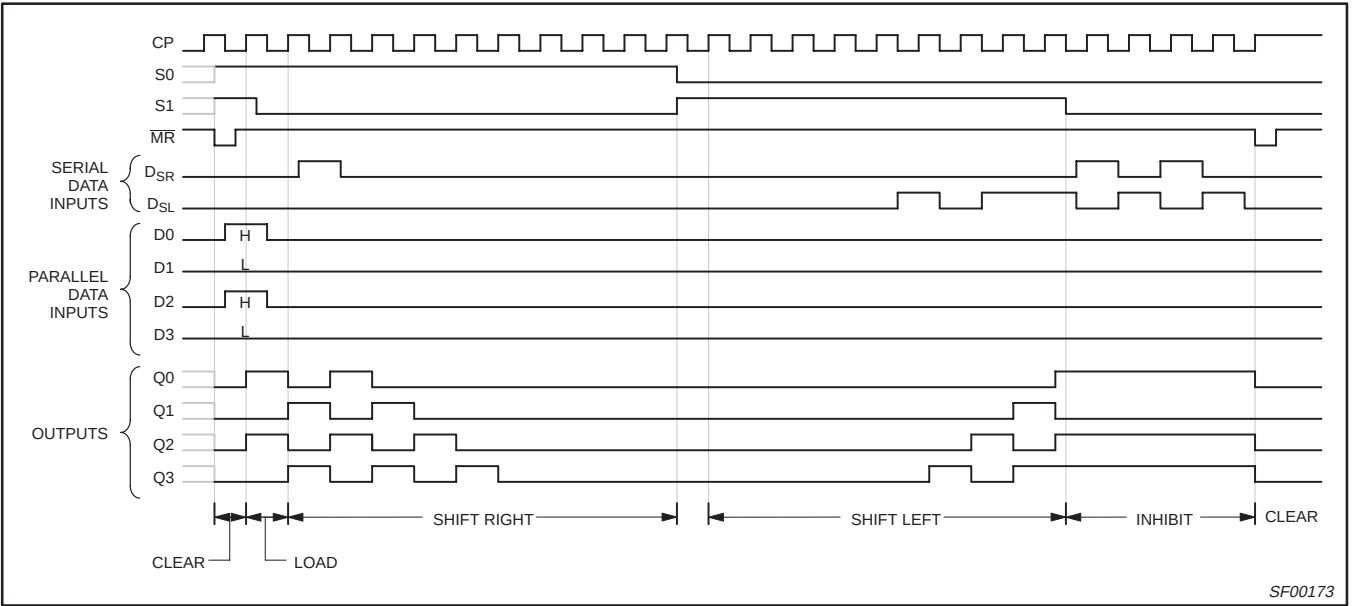
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time



Waveform 3. Setup and Hold Times

TIMING DIAGRAM

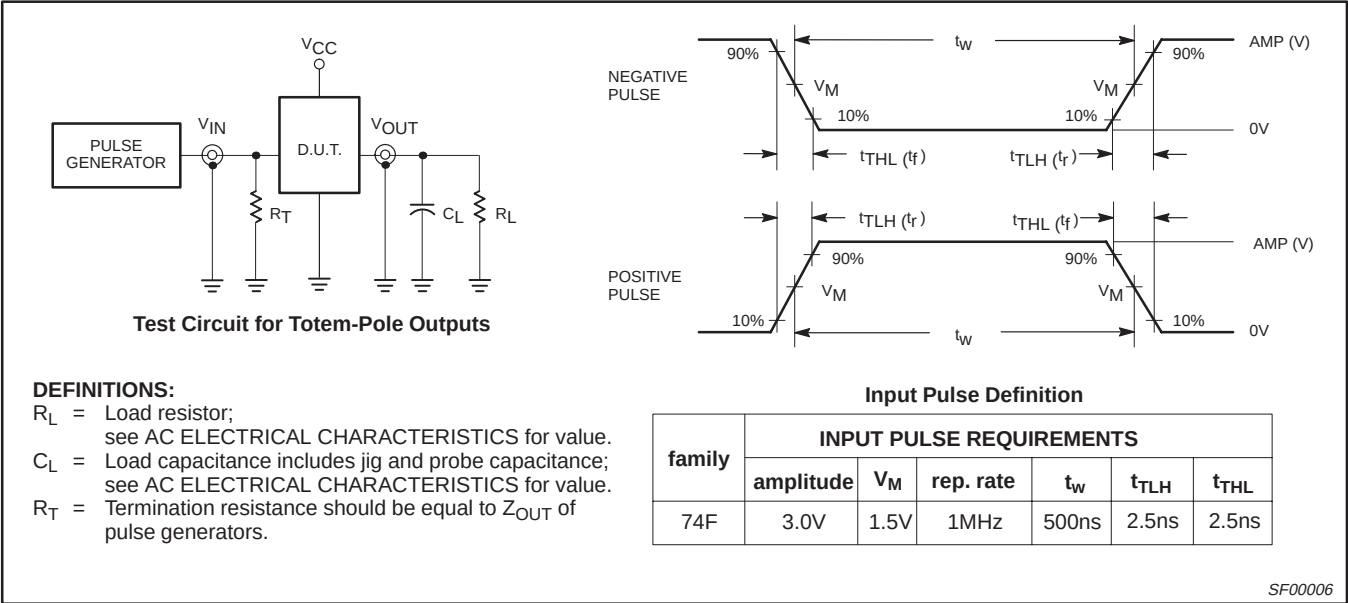
Typical Clear, Load, Shift-Right, Shift-Left and Inhibit Sequence



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TEST CIRCUIT AND WAVEFORMS

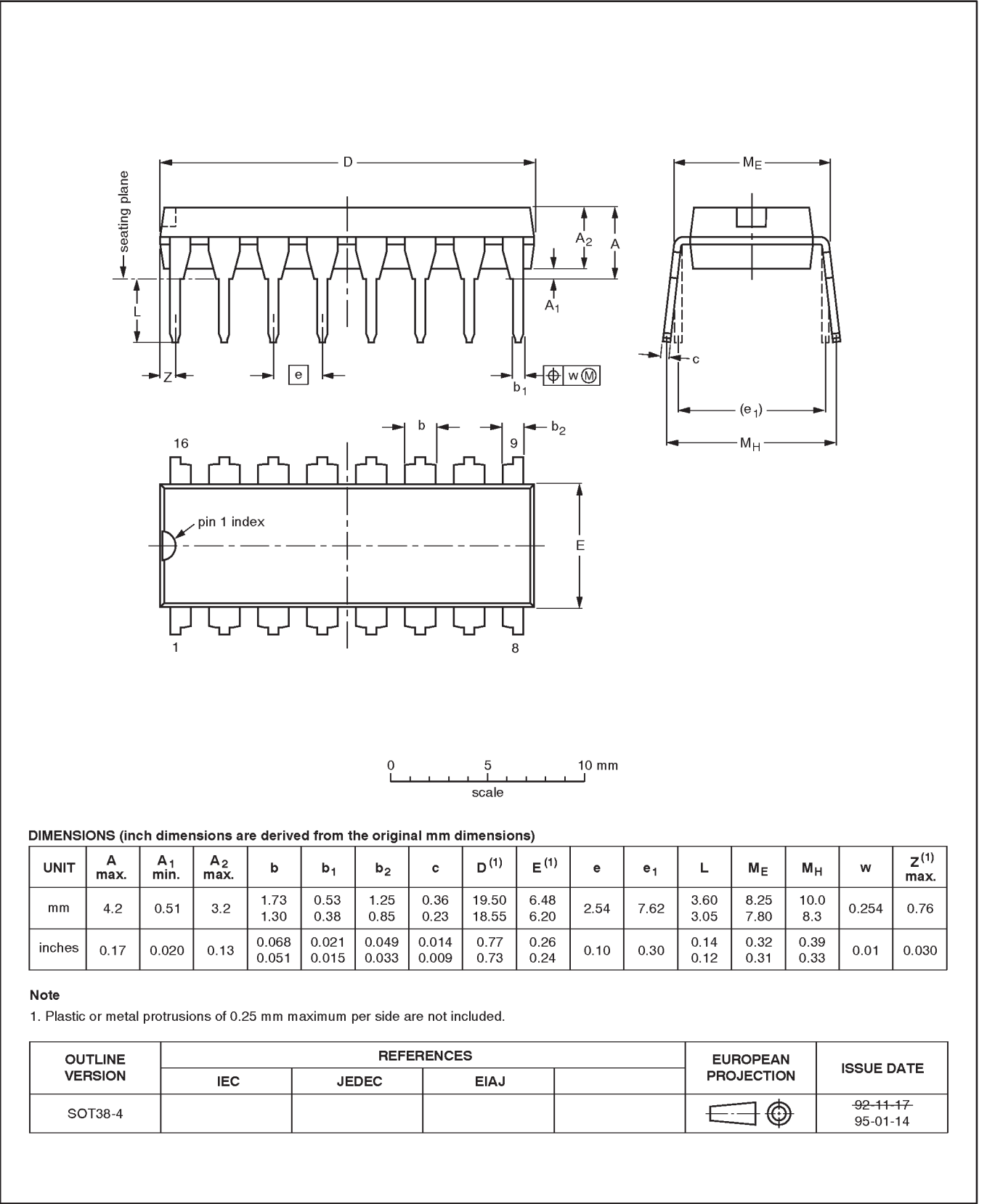


4-bit bidirectional universal shift register

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

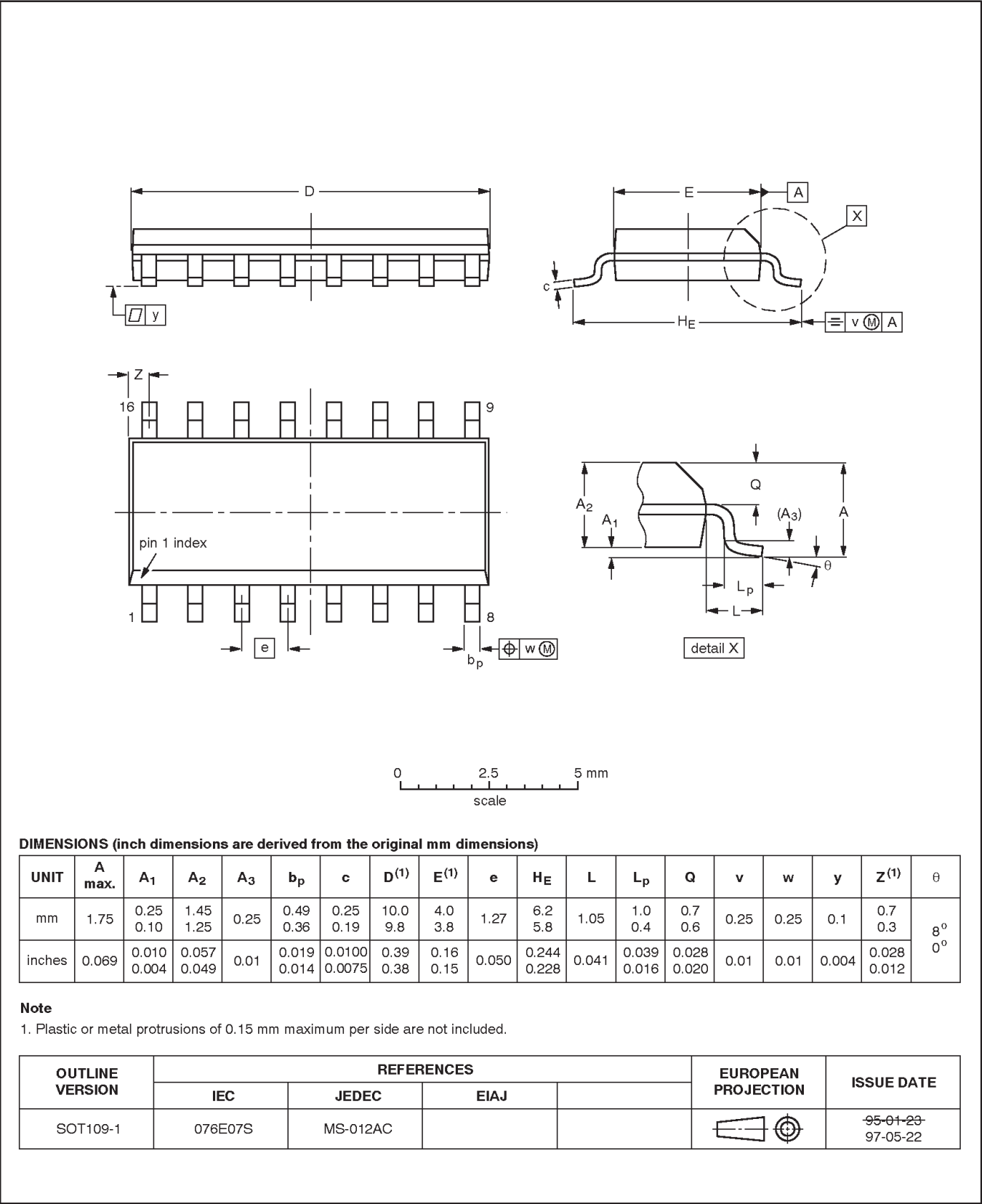


4-bit bidirectional universal shift register

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



4-bit bidirectional universal shift register

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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