

DATA SHEET

74F641

Octal bus transceiver with
common output enable,
non-inverting (open collector)

Product specification
Supersedes data of 1999 Jan 08
IC15 Data Handbook

2000 Jun 30

Octal bus transceiver with common output enable, non-inverting (open-collector)

74F641

FEATURES

- High-impedance NPN base inputs for reduced loading (20µA in High and Low states)
- Octal bidirectional bus interface
- Common Output Enable for both Transmit and Receive modes
- Open collector outputs sink 64mA
- Non-inverting

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	PKG DWG #
20-pin plastic DIP	N74F641N	SOT146-1
20-pin plastic SOL	N74F641D	SOT163-1

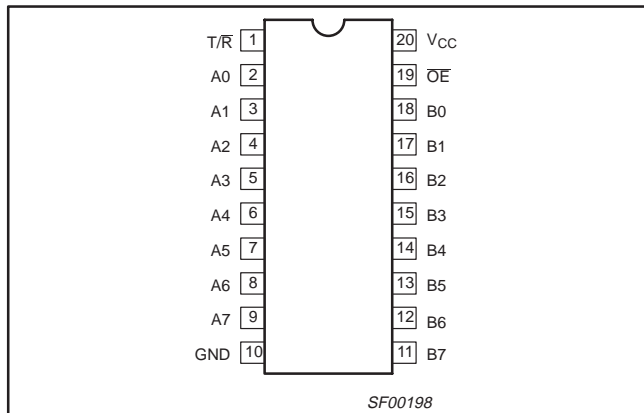
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F641	8.0ns	69mA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

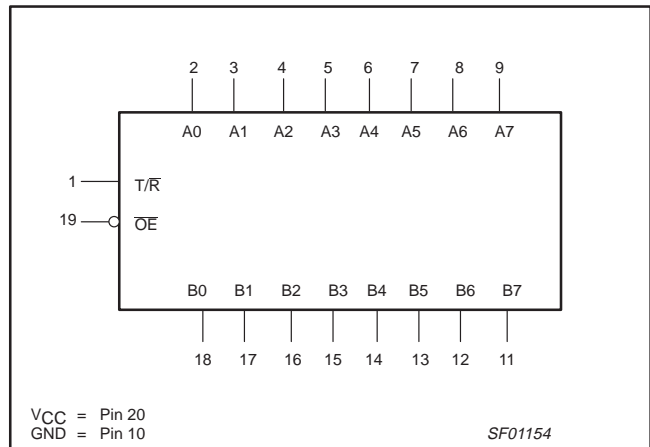
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 - A7, B0 - B7	Data inputs	1.0/0.033	20µA/20µA
T/R	Transmit/Receive input	2.0/0.067	40µA/40µA
\overline{OE}	Output Enable inputs	2.0/0.067	40µA/40µA
A0 - A7	Data outputs	OC/40	OC/24mA
B0 - B7	Data outputs	OC/106.7	OC/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state. OC = Open Collector.

PIN CONFIGURATION



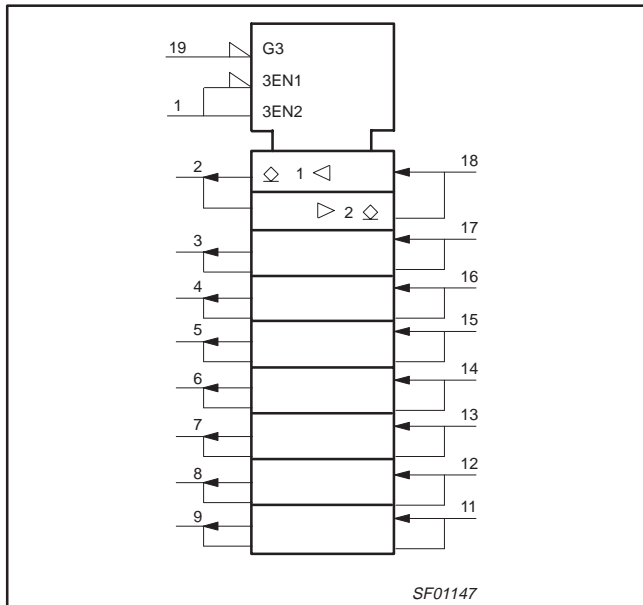
LOGIC SYMBOL



Octal bus transceiver with common output enable, non-inverting (open-collector)

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LOGIC SYMBOL (IEEE/IEC)

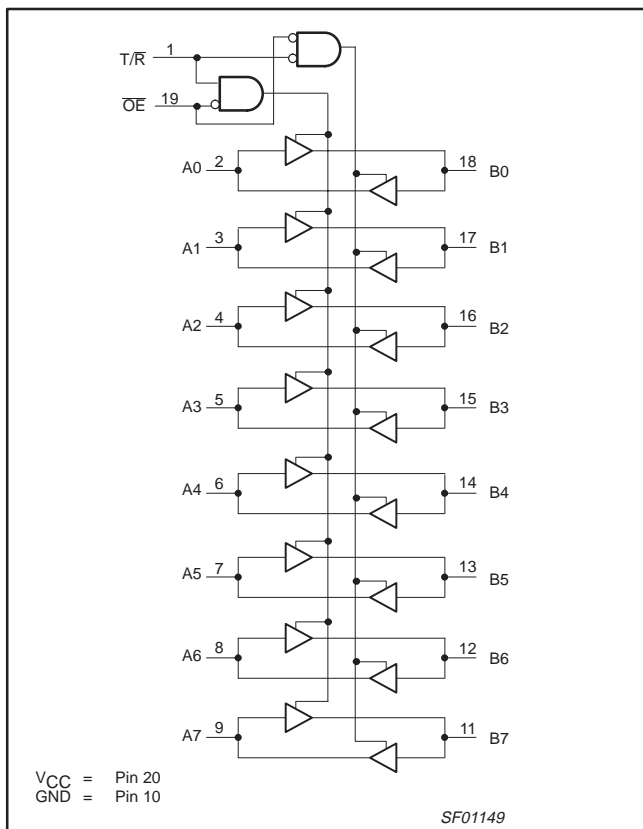


FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
OE	T/R	An	Bn
L	L	A=B	INPUTS
H	H	INPUTS	B=A
H	X	OFF	OFF

H = High voltage level
 L = Low voltage level
 X = Don't care
 OFF= High if pull-up resistor is connected to open collector output

LOGIC DIAGRAM



Octal bus transceiver with common output enable, non-inverting (open-collector)

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V _{CC}	Supply voltage		-0.5 to +7.0	V
V _{IN}	Input voltage		-0.5 to +7.0	V
I _{IN}	Input current		-30 to +5	mA
V _{OUT}	Voltage applied to output in High output state		-0.5 to +V _{CC}	V
I _{OUT}	Current applied to output in Low output state	A0–A7	48	mA
		B0–B7	128	mA
T _{amb}	Operating free-air temperature range		0 to +70	°C
T _{stg}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{IH}	High-level input voltage	2.0			V
V _{IL}	Low-level input voltage			0.8	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			4.5	V
I _{OL}	Low-level output current	A0–A7		24	mA
		B0–B7		64	mA
T _{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT		
			MIN	TYP ²	MAX			
I _{OH}	High-level output current	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, V _{OH} = MAX			250	μA		
V _{OL}	Low-level output voltage	A0–A7	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN,	I _{OL} = 24mA	±10%V _{CC}	0.35	0.50	V
				I _{OL} = 48mA	±5%V _{CC}	0.35	0.50	V
		B0–B7	I _{OL} = 48mA	±10%V _{CC}	0.38	0.55	V	
			I _{OL} = 64mA	±5%V _{CC}	0.42	0.55	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-0.73	-1.2	V	
I _I	Input current at maximum input voltage	T/R, OE	V _{CC} = 0.0V, V _I = 7.0V			100	μA	
		An, Bn	V _{CC} = 5.5V, V _I = 5.5V			1	mA	
I _{IH}	High-level input current	T/R, OE	V _{CC} = MAX, V _I = 2.7V			40	μA	
		An, Bn	V _{CC} = MAX, V _I = 2.7V			20	μA	
I _{IL}	Low-level input current	T/R, OE	V _{CC} = MAX, V _I = 0.5V			-40	μA	
		An, Bn	V _{CC} = MAX, V _I = 0.5V			-20	μA	
I _{CC}	Supply current (total)	74F641	I _{CCH}	V _{CC} = MAX	An=T/R=4.5, OE=GND	60	90	mA
			I _{CCL}		T/R=4.5V, An=OE=GND	78	120	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_{amb} = 25°C.

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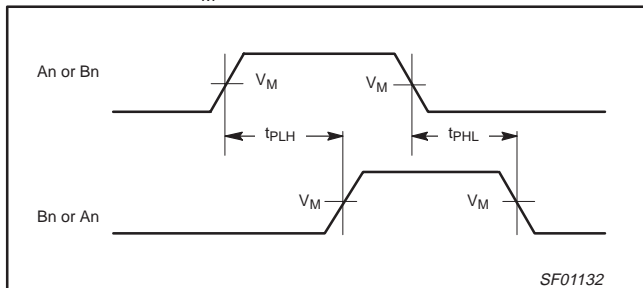
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AC ELECTRICAL CHARACTERISTICS – 74F641

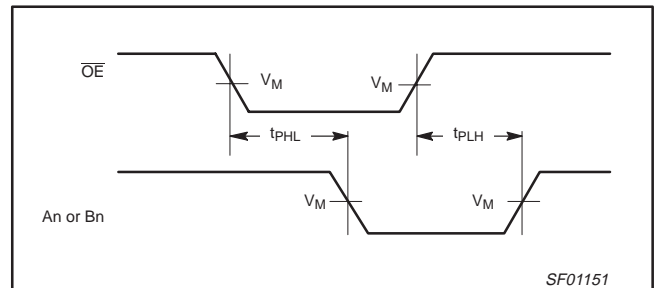
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V _{CC} = +5V T _{amb} = +25°C C _L = 50pF, R _L = 500Ω			V _{CC} = +5V ± 10% T _{amb} = 0°C to +70°C C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay An to Bn	Waveform 1	6.5 4.0	8.5 6.0	11.5 9.5	6.5 4.0	12.5 11.0	ns
t _{PLH} t _{PHL}	Propagation delay Bn to An	Waveform 1	6.0 3.5	8.0 5.5	11.5 7.5	6.0 3.5	12.0 8.0	ns
t _{PLH} t _{PHL}	Propagation delay OE to An	Waveform 2	7.0 5.0	10.5 7.0	12.5 9.0	7.0 5.0	13.0 10.0	ns
t _{PLH} t _{PHL}	Propagation delay OE to Bn	Waveform 2	8.0 3.5	9.0 7.5	12.5 9.5	8.0 5.5	13.5 10.5	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V.



Waveform 1. Propagation Delay for An to Bn or Bn to An



Waveform 2. Propagation Delay for OE to An or Bn Outputs (Bn or An Inputs in Low State)

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

Input Pulse Definition

TEST	SWITCH
t _{PLZ}	closed
t _{PZL}	closed
All other	open

DEFINITIONS:
 R_L = Load resistor; see AC electrical characteristics for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V _M	rep. rate	t _w	t _{TLH}	t _{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

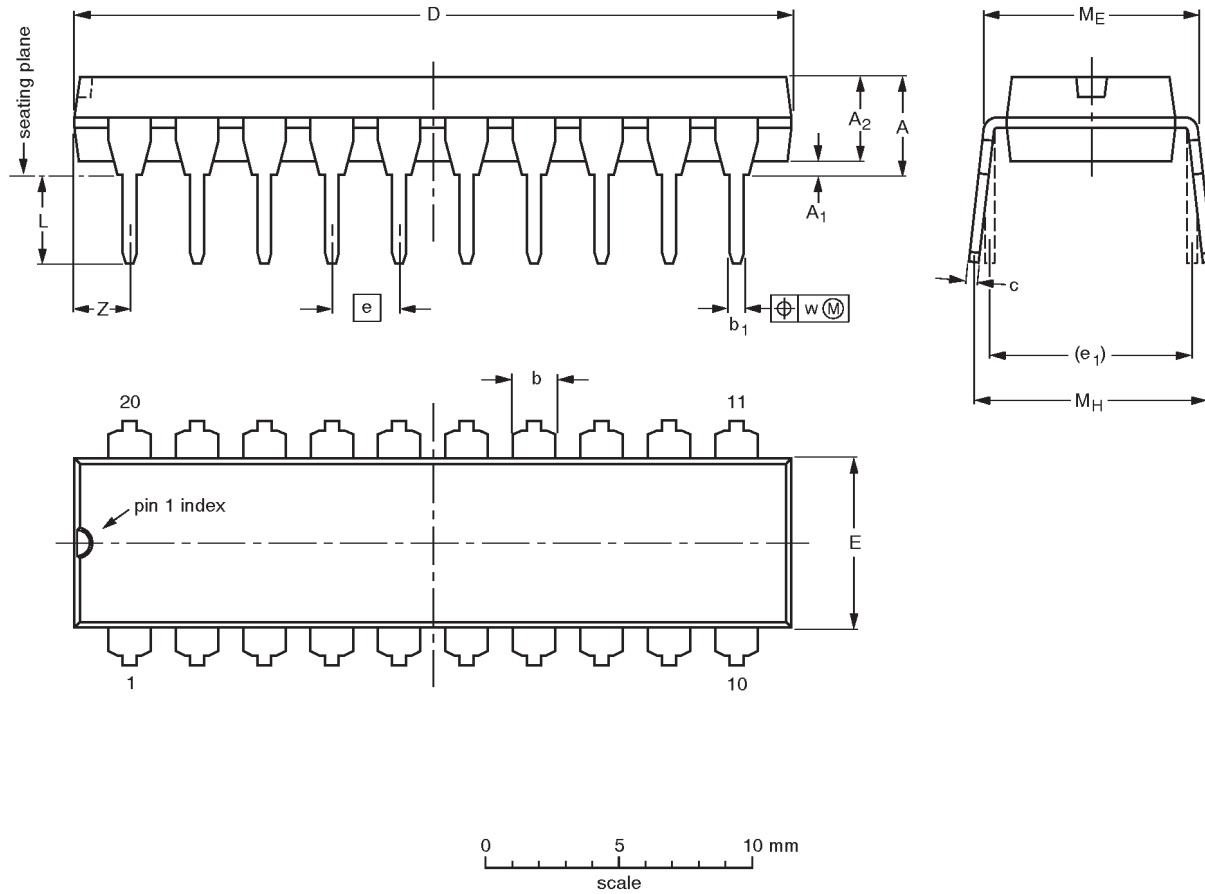
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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1




DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

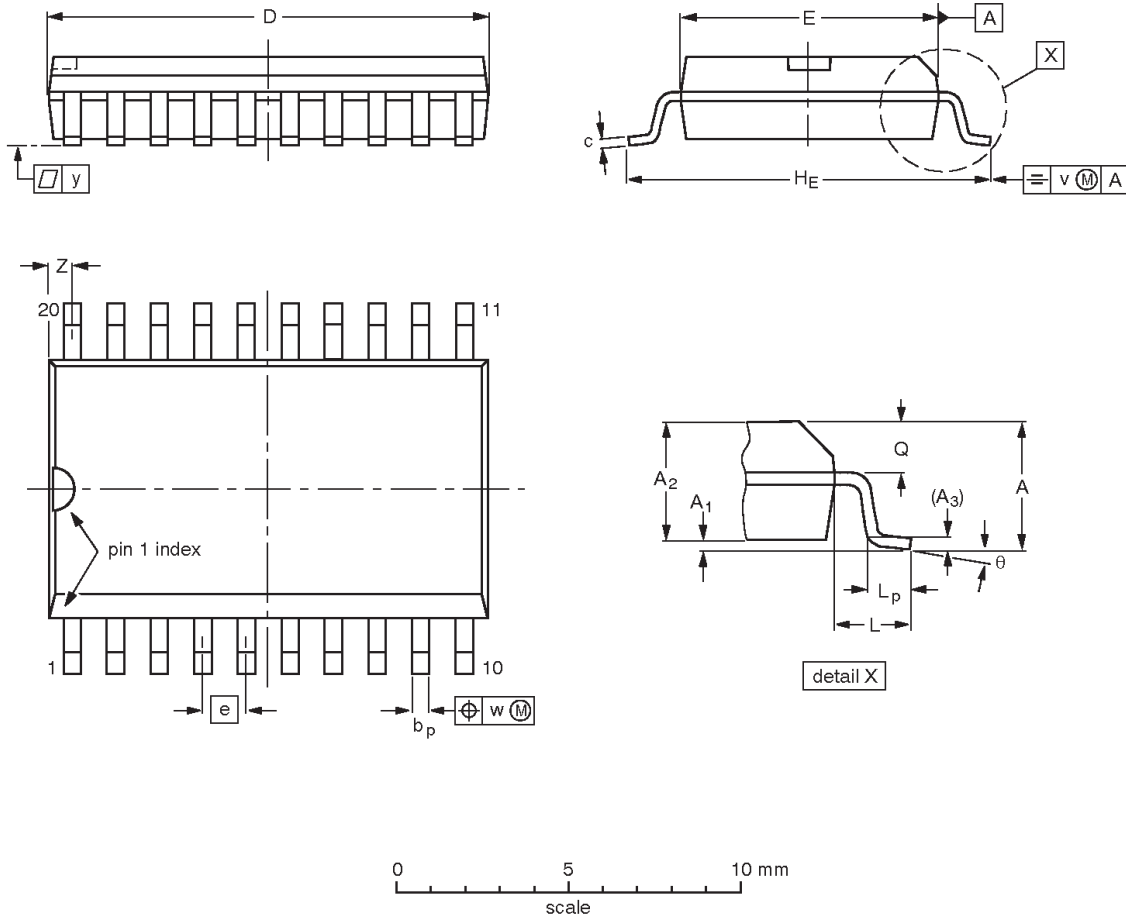
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Date of release: 06-00

Document order number:

9397-750 07277

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