DATA SHEET

74F646A
Octal transceiver/register, non-inverting (3-State)

74F648A
Octal transceiver/register, inverting (3-State)

Product data
2003 Feb 04
Replaces 74F646/646A/74F648/648A dated 1990 Sep 25

Philips
Semiconductors

PHILIPS

74F646A: *Octal transceiver/register, non-inverting (3-State)*
74F648A: *Octal transceiver/register, inverting (3-State)*

FEATURES

- Combines 74F245 and two 74F374 type functions in one chip
- High impedance base inputs for reduced loading (70 µA in HIGH and LOW states)
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Choice of non-inverting and inverting data paths
- Controlled ramp outputs for 74F646A/74F648A
- 3-state outputs
- 300 mil wide 24-pin slim DIP package

DESCRIPTION

The 74F646A and 74F648A transceivers/registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes HIGH. Output enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select pins (SAB, SBA) determine whether data is stored or transferred through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active LOW. In the isolation mode ($\overline{OE}$ = HIGH), data from bus A may be stored in the B register and/or data from bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
74F646A, 74F648A	185 MHz	105 mA

ORDERING INFORMATION

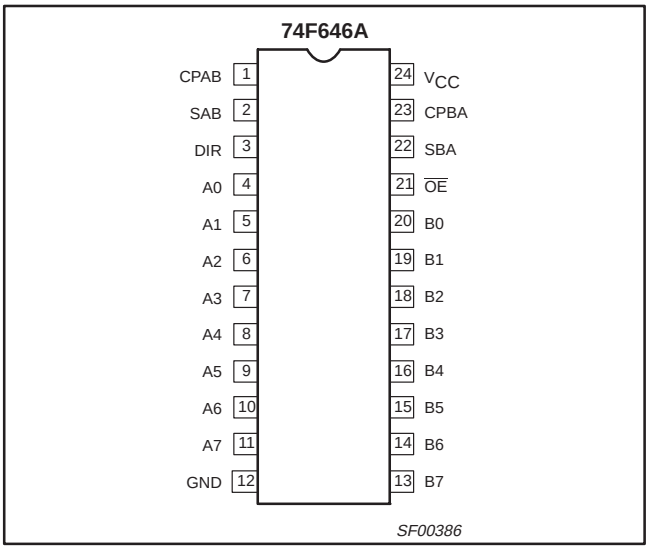
DESCRIPTION	ORDER CODE COMMERCIAL RANGE V_{CC} = 5 V ±10%, T_{amb} = 0 °C to +70 °C	PKG DWG #
24-pin plastic slim DIP (300 mil)	N74F646AN, N74F648AN	SOT222-1
24-pin plastic SOL	N74F646AD, N74F648AD	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

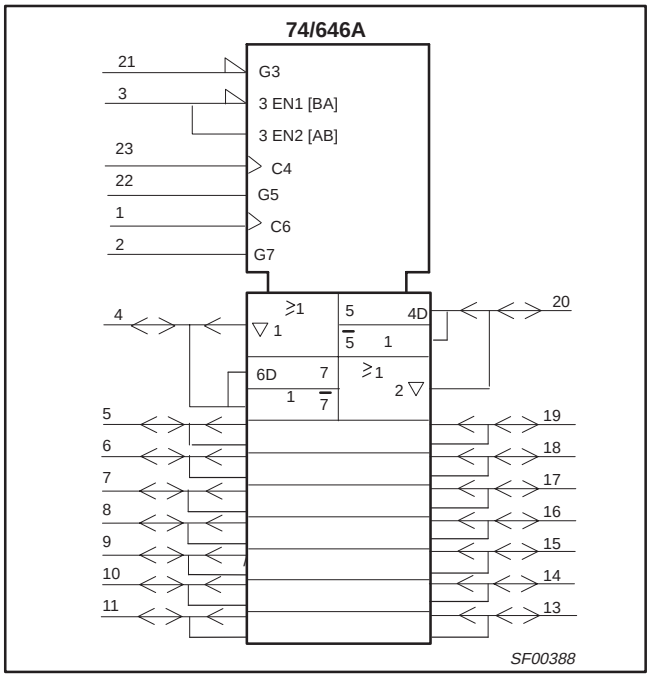
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH / LOW
A0-A7, B0-B7	A and B inputs	3.5 / 0.116	70 µA / 70 µA
CPAB	A-to-B clock input	1.0 / 0.033	20 µA / 20 µA
CPBA	B-to-A clock input	1.0 / 0.033	20 µA / 20 µA
SAB	A-to-B select input	1.0 / 0.033	20 µA / 20 µA
SBA	B-to-A select input	1.0 / 0.033	20 µA / 20 µA
DIR	Data flow directional control enable input	1.0 / 0.033	20 µA / 20 µA
$\overline{OE}$	Output enable input	1.0 / 0.033	20 µA / 20 µA
A0 - A7, B0 - B7	A, B outputs for N74F646A/N74F648A	750 / 80	15 mA / 48 mA

NOTE: One (1.0) FAST unit load is defined as: 20 µA in the HIGH state and 0.6 mA in the LOW state.

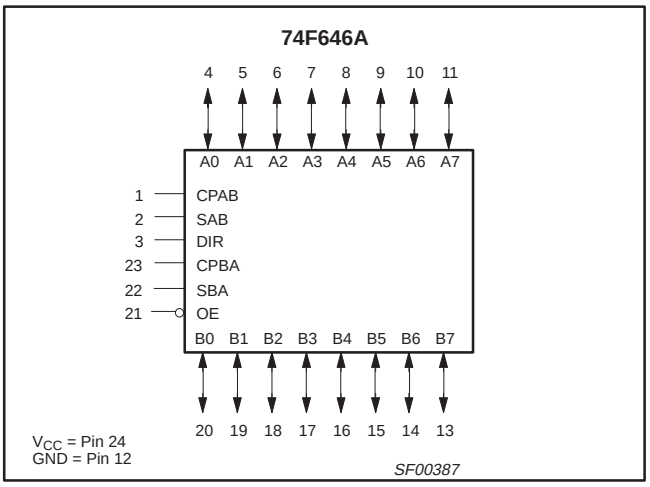
PIN CONFIGURATION



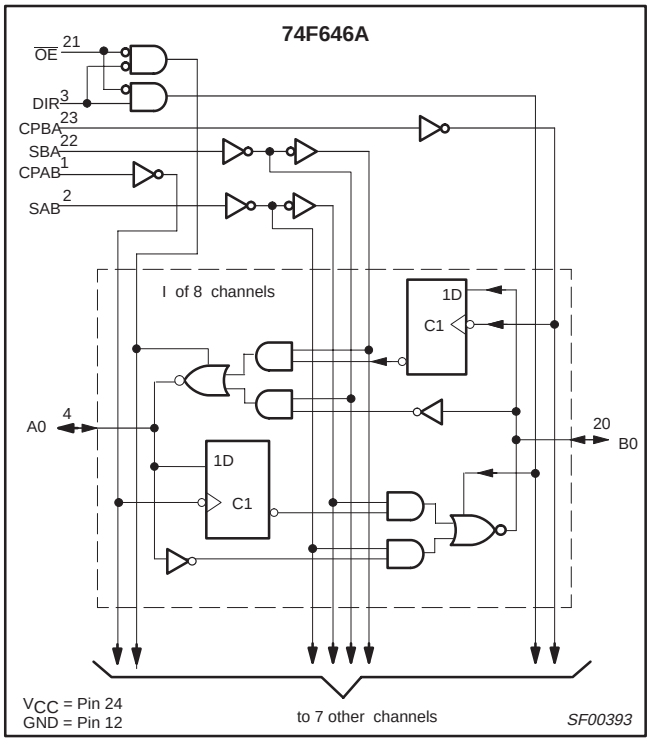
IEC/IEEE SYMBOL



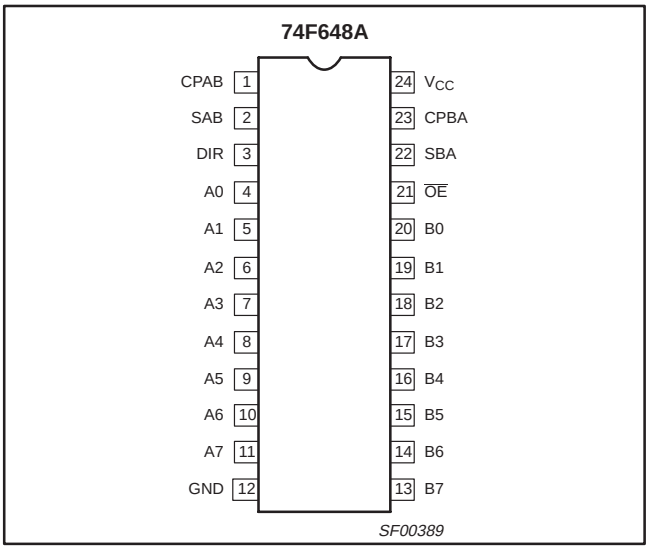
LOGIC SYMBOL



LOGIC DIAGRAM



PIN CONFIGURATION



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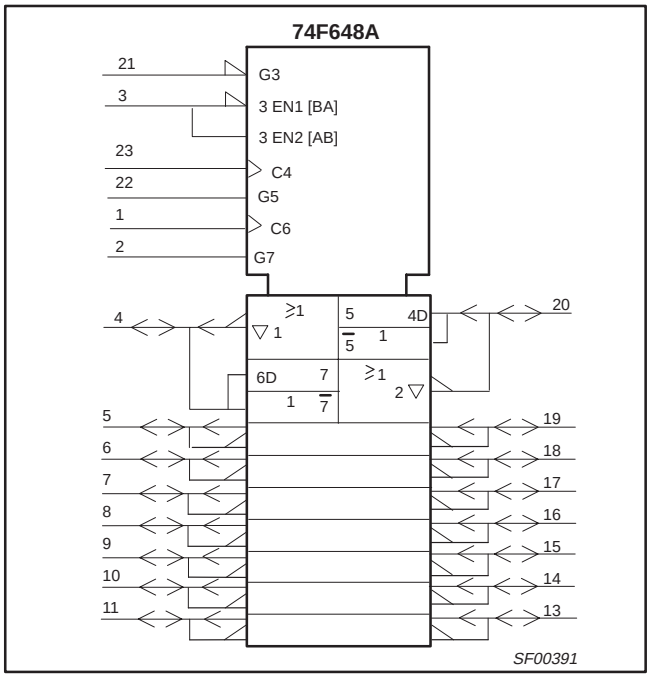

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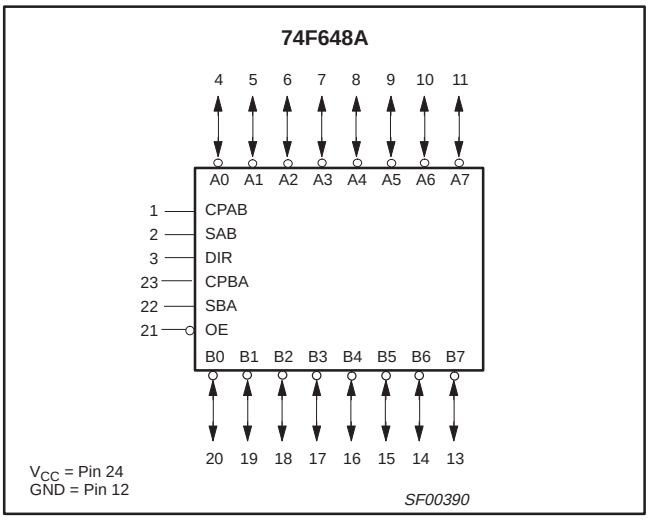
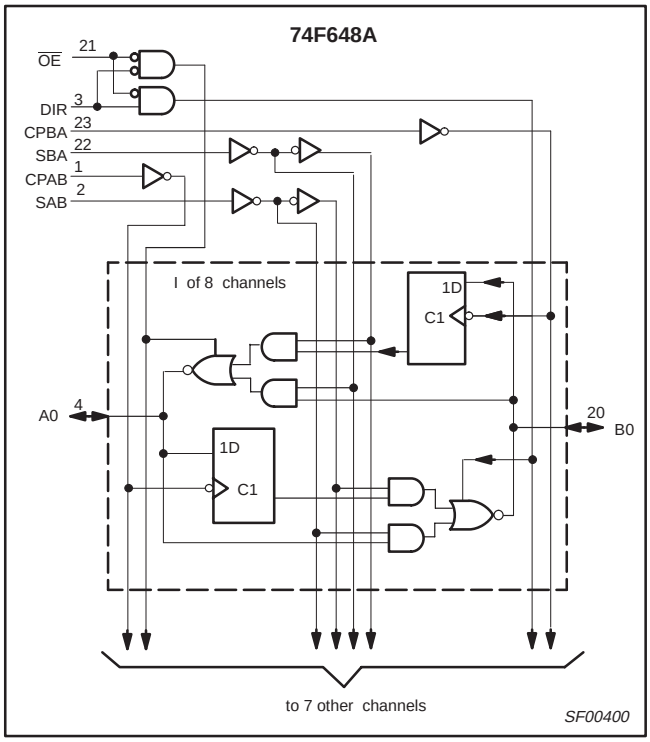


LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	An	Bn	74F646A	74F648A
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data	Store A and B data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus	Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus	Stored $\overline{A}$ data to B bus

NOTES:
1. H = High-voltage level
2. L = Low-voltage level
3. X = Don't care
4. ↑ = LOW-to-HIGH clock transition
5. * = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.

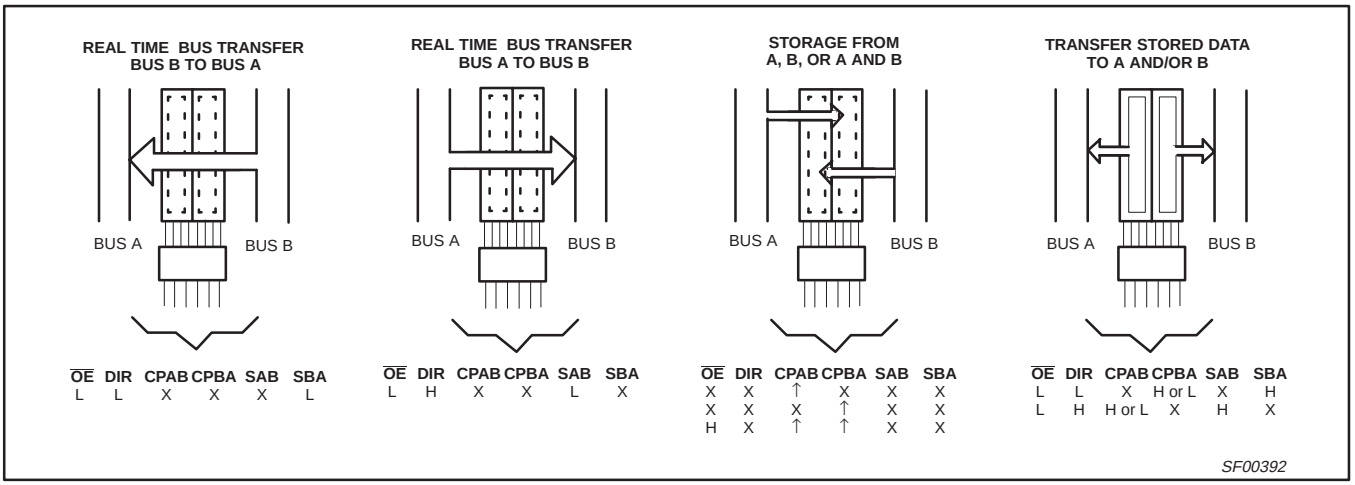
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in LOW output state	72	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0	–	–	V
V_{IL}	LOW-level input voltage	–	–	0.8	V
I_{Ik}	Input clamp current	–	–	–18	mA
I_{OH}	HIGH-level output current	–	–	–15	mA
I_{OL}	LOW-level output current	–	–	48	mA
T_{amb}	Operating free air temperature range	0	–	+70	°C

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74F646A and 74F648A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

BUS MANAGEMENT FUNCTIONS



DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	HIGH-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3 mA	±10%V_{CC}	2.4	–	–	V
					±5%V_{CC}	2.7	3.4	–	V
				I_{OH} = –15 mA	±10%V_{CC}	2.0	–	–	V
V_{OL}	LOW-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = 48 mA	±10%V_{CC}	–	0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			–	–0.73	–1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0 V, V_I = 7.0 V			–	–	100	µA
		A0-A7, B0-B7	V_{CC} = MAX, V_I = 5.5 V			–	–	1	mA
I_{IH}	HIGH-level input current	$\overline{OE}$, DIR, CPAB, CPBA, SAB, SBA	V_{CC} = MAX, V_I = 2.7 V			–	–	20	µA
I_{IL}	LOW-level input current		V_{CC} = MAX, V_I = 0.5 V			–	–	–20	µA
I_{OZH} + I_{IH}	Off-state output current, HIGH-level voltage applied	A0-A7, B0-B7	V_{CC} = MAX, V_O = 2.7 V			–	–	70	µA
I_{OZL} + I_{IL}	Off-state output current, LOW-level voltage applied		V_{CC} = MAX, V_O = 0.5 V			–	–	–70	µA
I_O	Output current[3]		V_{CC} = MAX, V_O = 2.25 V			–60	–	–150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			–	100	145	mA
		I_{CCL}				–	110	155	mA
		I_{CCZ}				–	105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, V_X = V_{CC} for all test conditions.
2. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
3. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS FOR 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 °C to +70 °C V_{CC} = +5.0 V ± 10% C_L = 50 pF, R_L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	165	185		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.5 4.5	7.0 7.0	10.5 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 2	4.0 2.0	6.0 5.0	9.0 8.0	3.5 2.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.5 3.5	6.5 8.0	9.5 10.0	4.0 3.0	10.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	3.0 3.0	5.5 5.5	9.0 10.0	2.5 2.5	10.0 10.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	3.0 3.5	5.0 6.0	8.0 8.5	3.0 3.0	8.5 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	1.5 2.5	4.0 5.5	6.5 8.0	1.0 2.0	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.0 3.0	4.5 5.0	7.5 8.0	1.5 2.0	8.5 8.5	ns

AC SET-UP REQUIREMENTS FOR 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0 V C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0 V ± 10% C_L = 50 pF, R_L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW An or Bn to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, HIGH or LOW CPAB or CPBA	Waveform 1	3.5 3.5			4.5 4.0		ns

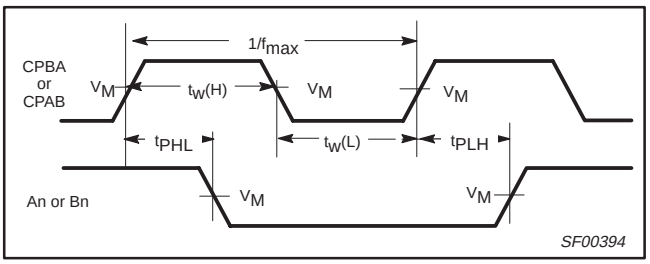
AC ELECTRICAL CHARACTERISTICS FOR 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0 V C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0 V ± 10% C_L = 50 pF, R_L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	160	185		135		ns
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to An or Bn	Waveform 1	5.0 5.5	7.0 7.5	9.5 10.0	4.5 4.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	Waveform 3	2.5 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to An or Bn	Waveform 2, 3	4.0 4.5	7.0 7.0	9.5 9.5	3.5 4.5	11.5 10.0	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	3.5 4.5	6.5 6.5	10.0 10.0	3.5 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output enable time DIR to An or Bn	Waveform 5 Waveform 6	3.5 4.0	5.5 6.5	8.5 9.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OE}$ to An or Bn	Waveform 5 Waveform 6	2.5 4.0	4.0 6.5	6.5 9.0	2.0 3.5	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time DIR to An or Bn	Waveform 5 Waveform 6	2.5 2.5	5.0 5.0	8.5 8.0	2.0 3.5	9.0 9.0	ns

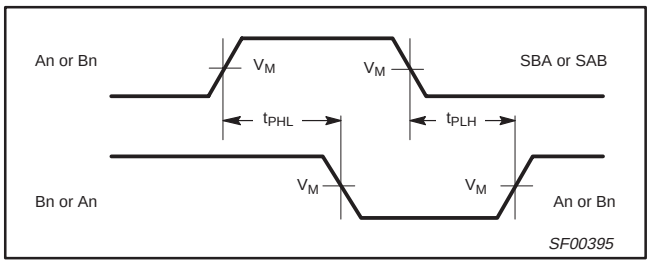
AC SET-UP REQUIREMENTS FOR 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25 °C V_{CC} = +5.0 V C_L = 50 pF, R_L = 500 Ω			T_{amb} = 0 °C to +70 °C V_{CC} = +5.0 V ± 10% C_L = 50 pF, R_L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su} (L)	Set-up time, HIGH or LOW An or Bn to CPAB or CPBA	Waveform 4	4.0 4.0			4.5 4.5		ns
t_h (H) t_h (L)	Hold time, HIGH or LOW An or Bn to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w (H) t_w (L)	Pulse width, HIGH or LOW CPAB or CPBA	Waveform 1	3.5 3.5			4.0 3.5		ns

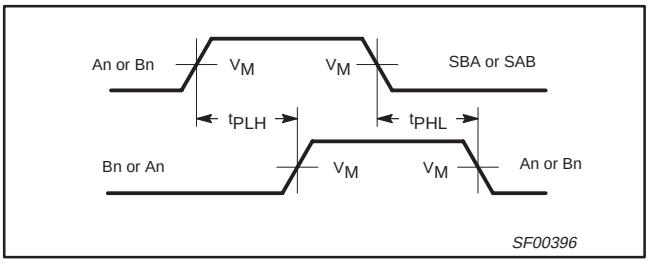
AC WAVEFORMS



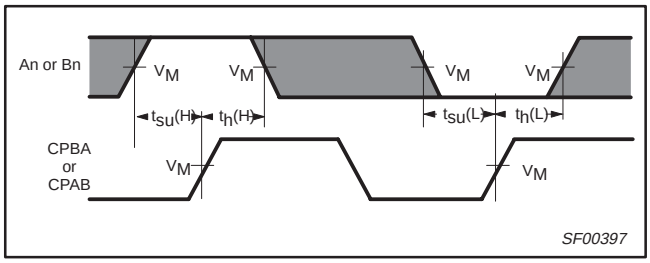
Waveform 1. Propagation delay for clock input to output clock pulse width, and maximum clock frequency



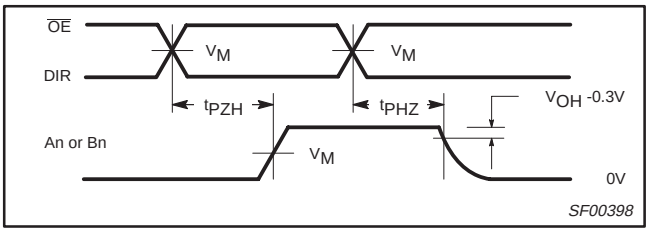
Waveform 2. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



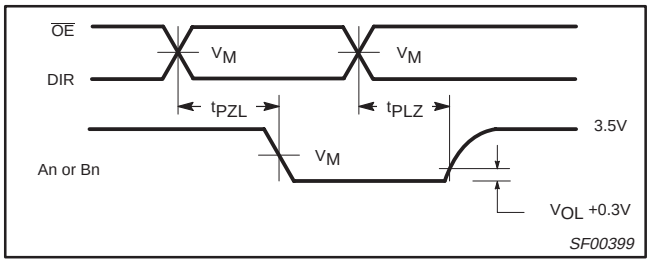
Waveform 3. Propagation delay for An to Bn or Bn to An and SAB or SBA to An or Bn



Waveform 4. Data set-up time and hold times



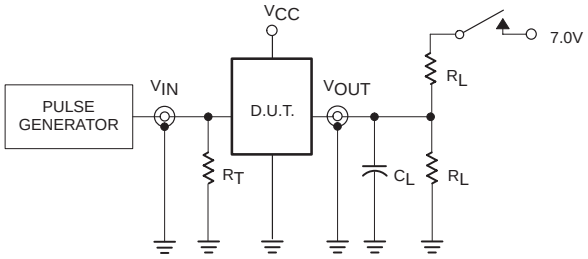
Waveform 5. 3-state output enable time to HIGH level and output disable time from HIGH level



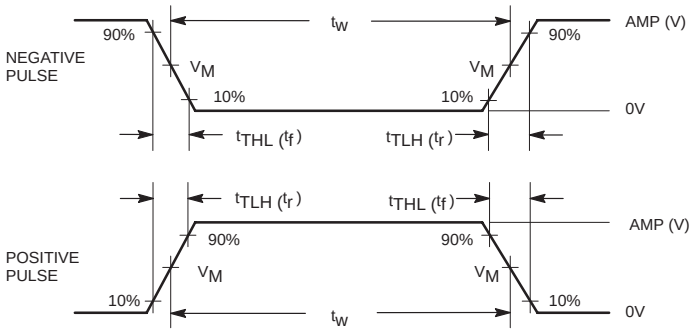
Waveform 6. 3-state output enable time to LOW level and output disable time from LOW level

NOTES:
1. For all waveforms, V_M = 1.5 V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collector Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

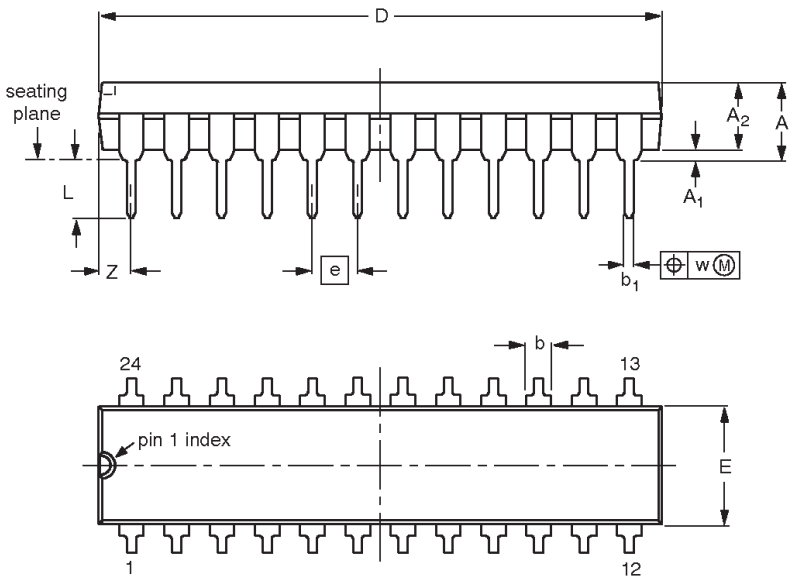
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

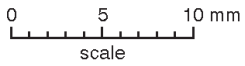
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00128

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

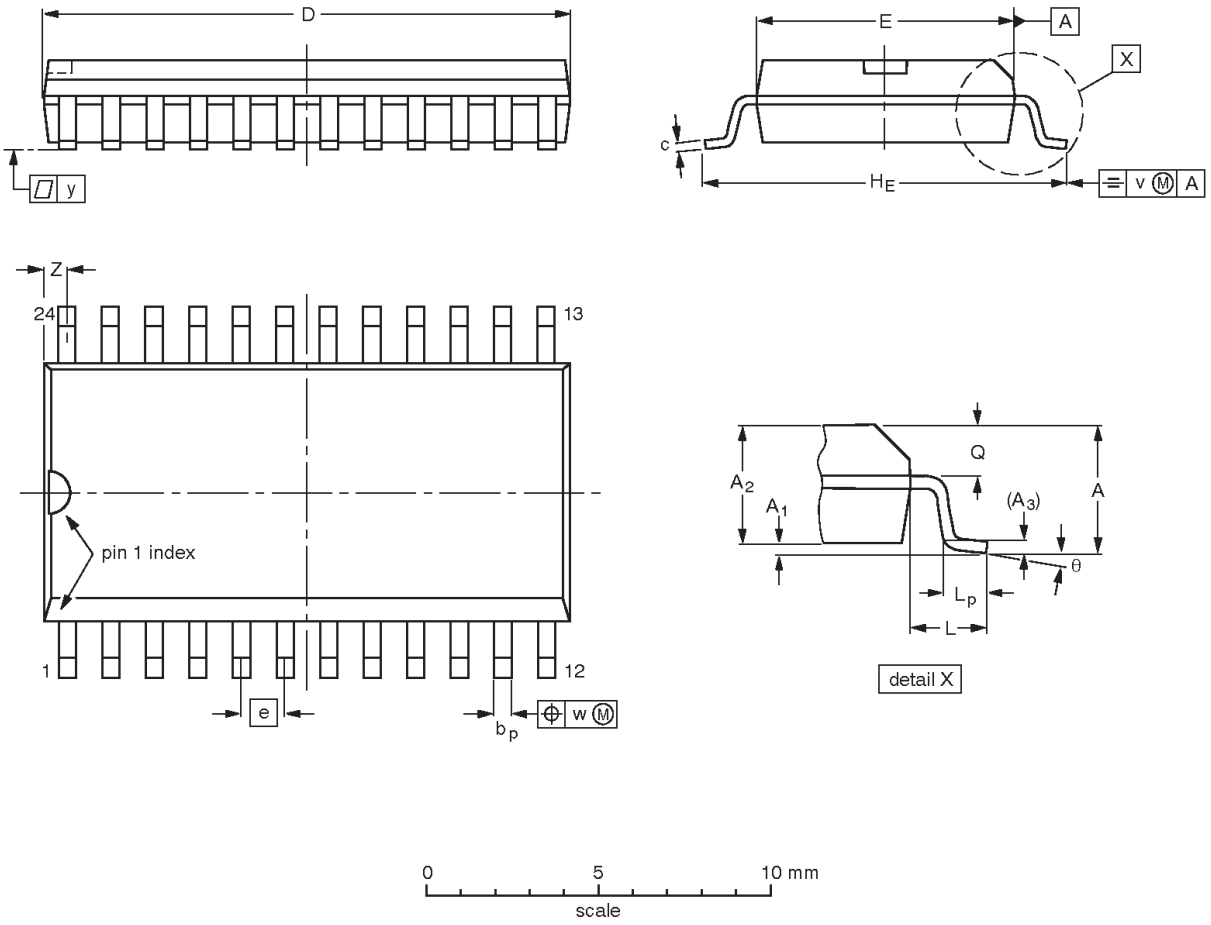
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001				~~99-04-28~~ 99-12-27

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013				~~97-05-22~~ 99-12-27

REVISION HISTORY

Rev	Date	Description
_4	20030204	**74F646A/74F648A Product data (9397 750 05151); ECN 853-1124 29306 of 17 December 2002. Supersedes 74F646/A/74F648/A_3 of 1990Sep25.** Modifications: ● Delete all references to non-A version specifications. The non-A versions of these devices have been discontinued.
_3	19900925	**74F646/A/74F648/A Product specification (9397 750 05151); ECN 853-1124 00515 of 25 September 1990.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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