

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT195** 4-bit parallel access shift register

Product specification  
File under Integrated Circuits, IC06

December 1990

## 4-bit parallel access shift register

## 74HC/HCT195

## FEATURES

- Asynchronous master reset
- J,  $\bar{K}$ , (D) inputs to the first stage
- Fully synchronous serial or parallel data transfer
- Shift right and parallel load capability
- Complement output from the last stage
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT195 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT195 performs serial, parallel, serial-to-parallel or parallel-to-serial data transfer at very high speeds. The "195" operates on two primary modes: shift right ( $Q_0 \rightarrow Q_1$ ) and parallel load, which are controlled

by the state of the parallel load enable ( $\overline{PE}$ ) input. Serial data enters the first flip-flop ( $Q_0$ ) via the J and  $\bar{K}$  inputs when the  $\overline{PE}$  input is HIGH and shifted one bit in the direction  $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$  following each LOW-to-HIGH clock transition. The J and  $\bar{K}$  inputs provide the flexibility of the JK type input for special applications and by tying the pins together, the simple D-type input for general applications. The "195" appears as four common clocked D flip-flops when the  $\overline{PE}$  input is LOW.

After the LOW-to-HIGH clock transition, data on the parallel inputs ( $D_0$  to  $D_3$ ) is transferred to the respective  $Q_0$  to  $Q_3$  outputs. Shift left operation ( $Q_3 \rightarrow Q_2$ ) can be achieved by tying the  $Q_n$  outputs to the  $D_{n-1}$  inputs and holding the  $\overline{PE}$  input LOW.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. There is no restriction on the activity of the J,  $\bar{K}$ ,  $D_n$  and  $\overline{PE}$  inputs for logic operation other than the set-up and hold time requirements. A LOW on the asynchronous master reset ( $\overline{MR}$ ) input sets all Q outputs LOW, independent of any other input condition.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	15	15	ns
f <sub>max</sub>	maximum clock frequency		57	57	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	105	105	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \quad \text{where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1,5 V

## ORDERING INFORMATION

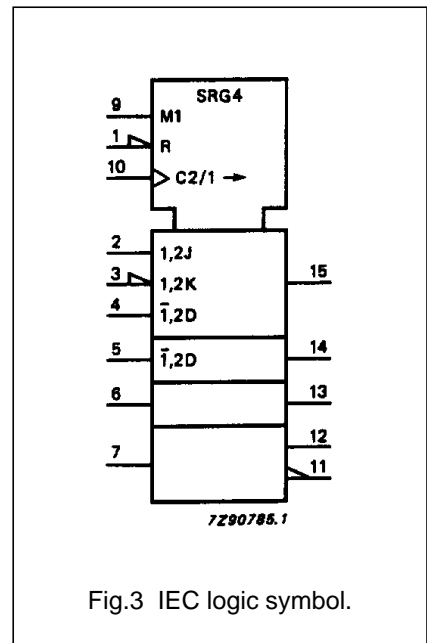
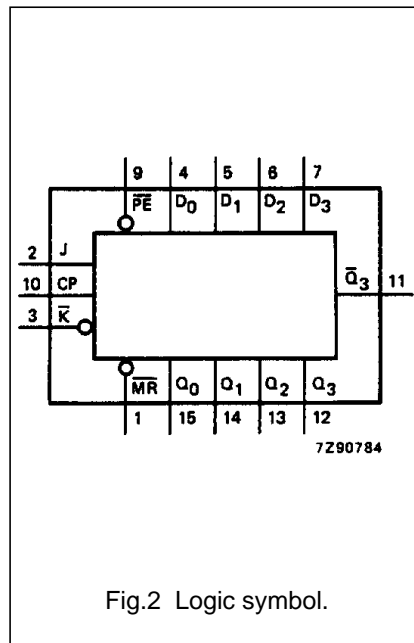
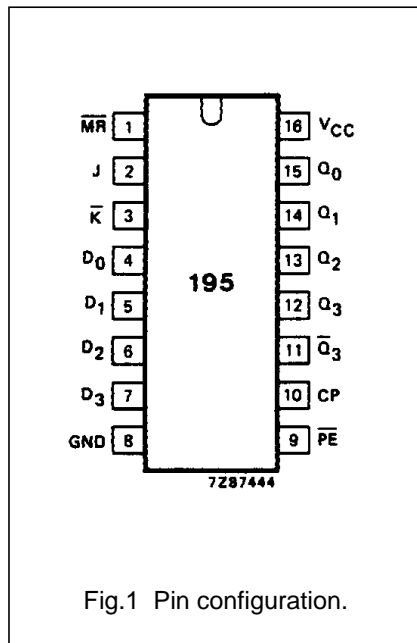
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{MR}$	master reset input (active LOW)
2	J	first stage J-input (active HIGH)
3	$\overline{K}$	first stage $\overline{K}$ -input (active LOW)
4, 5, 6, 7	D <sub>0</sub> to D <sub>3</sub>	parallel data inputs
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CP	clock input (LOW-to-HIGH edge-triggered)
11	$\overline{Q}_3$	inverted output from the last stage
15, 14, 13, 12	Q <sub>0</sub> to Q <sub>3</sub>	parallel outputs
16	V <sub>CC</sub>	positive supply voltage



4-bit parallel access shift register

74HC/HCT195

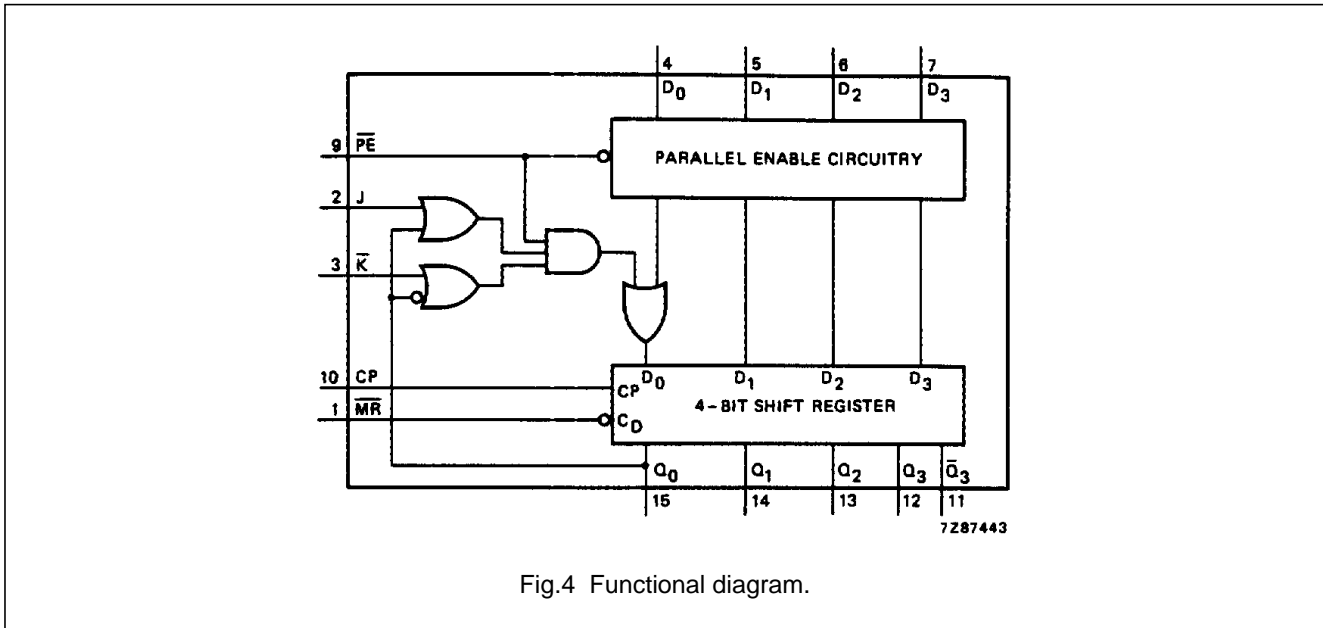


Fig.4 Functional diagram.

APPLICATIONS

- Serial data transfer
- Parallel data transfer
- Serial-to-parallel data transfer
- Parallel-to-serial data transfer

FUNCTION TABLE

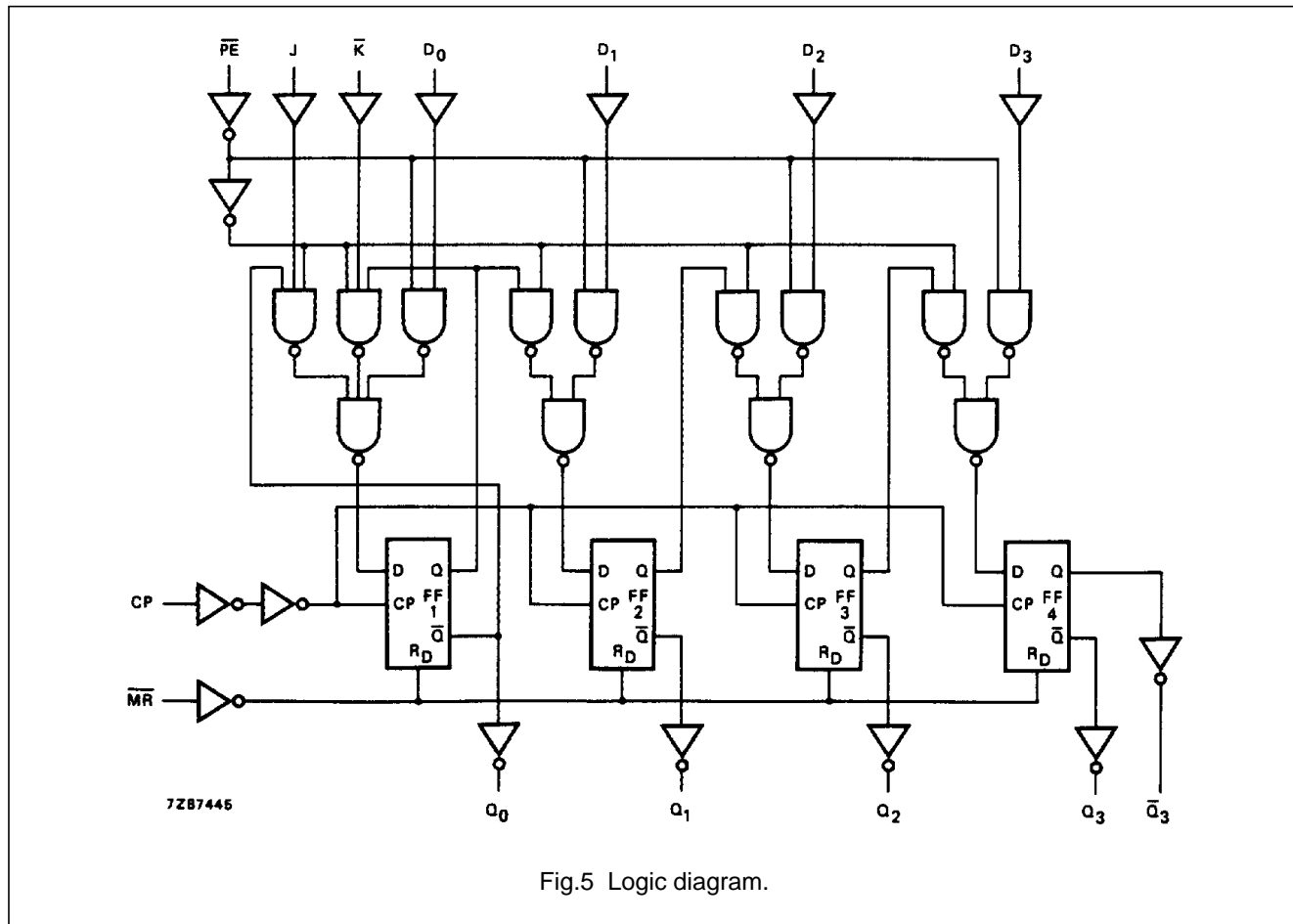
OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D <sub>n</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	$\overline{Q}_3$
asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
shift, set first stage	H	↑	h	h	h	X	H	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	$\overline{q}_2$
shift, reset first stage	H	↑	h	l	l	X	$\overline{L}$	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	$\overline{q}_2$
shift, toggle first stage	H	↑	h	h	l	X	q <sub>0</sub>	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	$\overline{q}_2$
shift, retain first stage	H	↑	h	l	h	X	q <sub>0</sub>	q <sub>0</sub>	q <sub>1</sub>	q <sub>2</sub>	$\overline{q}_2$
parallel load	H	↑	l	X	X	d <sub>n</sub>	d <sub>0</sub>	d <sub>1</sub>	d <sub>2</sub>	d <sub>3</sub>	$\overline{d}_3$

Notes

- H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition  
 q, d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH clock transition  
 X = don't care  
 ↑ = LOW-to-HIGH clock transition

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>w</sub>	master reset pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>rem</sub>	removal time MR to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t <sub>su</sub>	set-up time J to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Figs 8 and 9
t <sub>su</sub>	set-up time K̄, PĒ, D <sub>n</sub> to CP	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Figs 8 and 9
t <sub>h</sub>	hold time J, K̄, PĒ, D <sub>n</sub> to CP	3 3 3	-8 -3 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Figs 8 and 9
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	17 52 62		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig.6

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## 74HC/HCT195

**DC CHARACTERISTICS FOR HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{PE}$	0.65
all others	0.35

**AC CHARACTERISTICS FOR 74HCT**

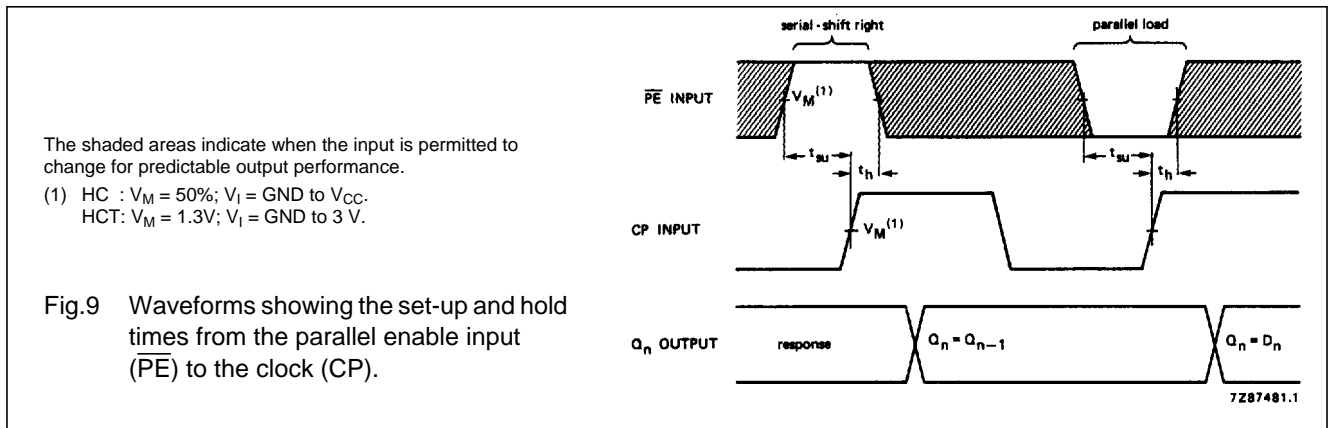
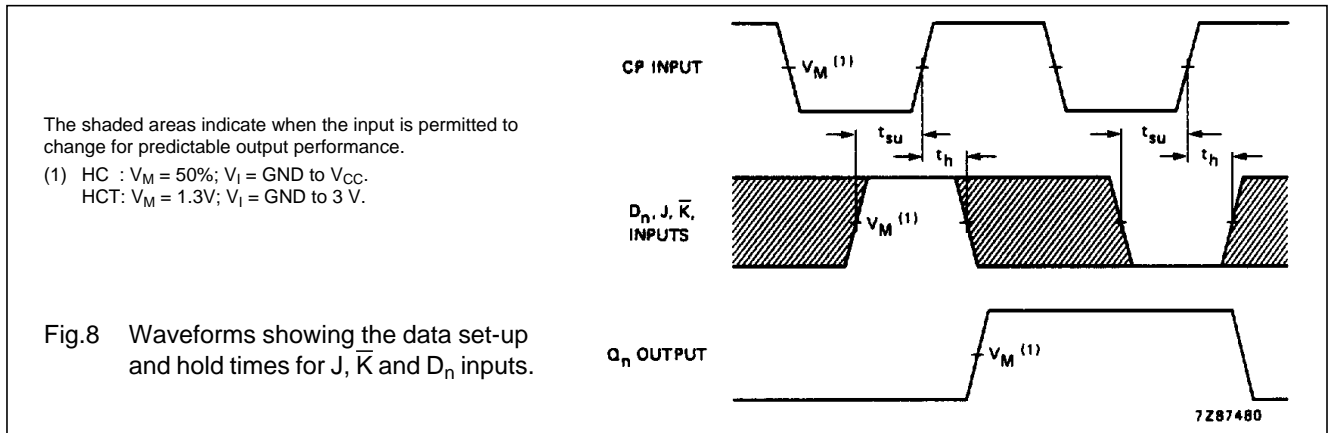
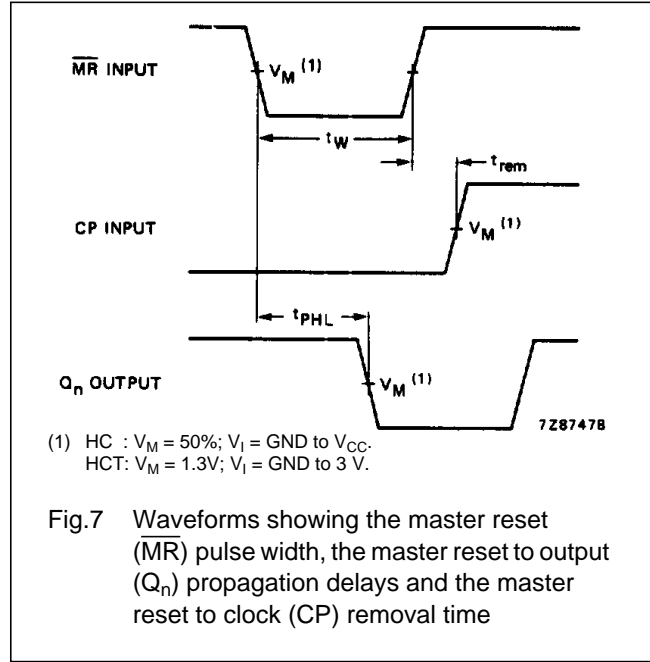
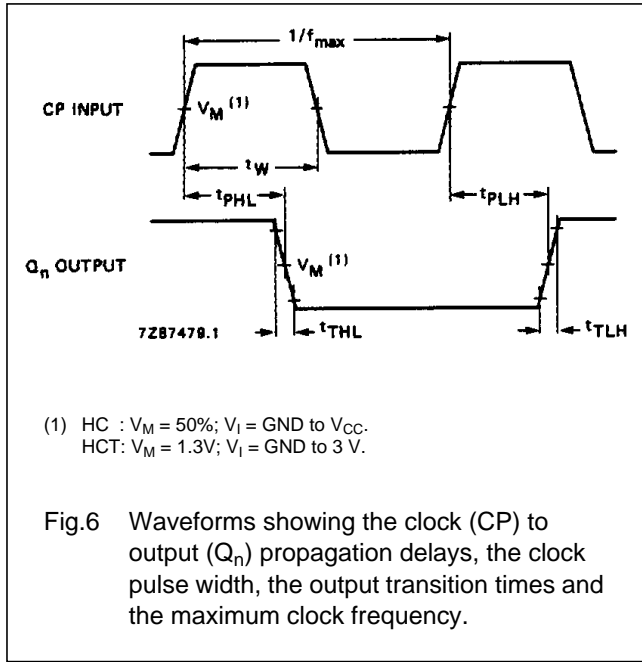
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		18	32		40		48	ns	4.5	Fig.6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		17	35		44		53	ns	4.5	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	20	6		25		30		ns	4.5	Fig.6
t <sub>W</sub>	master reset pulse width LOW	16	6		20		24		ns	4.5	Fig.8
t <sub>rem</sub>	removal time $\overline{MR}$ to CP	16	6		20		24		ns	4.5	Fig.8
t <sub>su</sub>	set-up time J, $\overline{K}$ , $\overline{PE}$ to CP	20	12		25		30		ns	4.5	Figs 8 and 9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	16	6		20		24		ns	4.5	Figs 8 and 9
t <sub>h</sub>	hold time J, $\overline{K}$ , $\overline{PE}$ , D <sub>n</sub> to CP	3	-5		3		3		ns	4.5	Figs 8 and 9
f <sub>max</sub>	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig.6

4-bit parallel access shift register

74HC/HCT195

AC WAVEFORMS





## 4-bit parallel access shift register

74HC/HCT195

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### **PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.