DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT40104
4-bit bidirectional universal shift register; 3-state

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

4-bit bidirectional universal shift register; 3-state

74HC/HCT40104

FEATURES

- Synchronous parallel or serial operating
- 3-state outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT40104 are high-speed Si-gate CMOS devices and are pin compatible with the “40104” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT40104 are universal shift registers featuring parallel inputs, parallel outputs, shift-right and shift-left serial inputs and 3-state outputs allowing the devices to be used in bus-organized systems.

In the parallel-load mode (S_0 and S_1 are HIGH), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP).

During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the shift-right (D_{SR}) and shift-left (D_{SL}) serial inputs, respectively.

Clearing the register is accomplished by setting both mode controls (S_0 and S_1) LOW and clocking the register. When the output enable input (OE) is LOW, all outputs assume the high-impedance OFF-state (Z).

APPLICATIONS

- Arithmetic unit bus registers
- Serial/parallel conversion
- General-purpose register for bus organized systems
- General-purpose registers

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	13	15	ns
f_{max}	maximum clock frequency		62	57	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	75	75	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	OE	3-state output enable input (active HIGH)
2	D_{SR}	serial data shift-right input
3, 4, 5, 6	D_0 to D_3	parallel data inputs
7	D_{SL}	serial data shift-left input
8	GND	ground (0 V)
9, 10	S_0, S_1	mode control inputs
11	CP	clock input (LOW-to-HIGH, edge-triggered)
15, 14, 13, 12	Q_0 to Q_3	3-state parallel outputs
16	V_{CC}	positive supply voltage

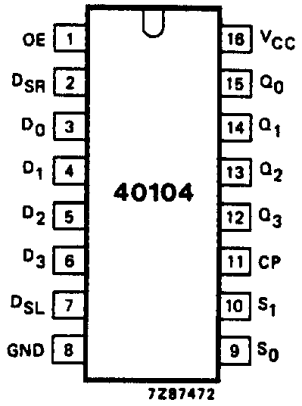


Fig.1 Pin configuration.

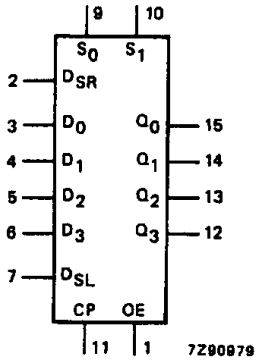


Fig.2 Logic symbol.

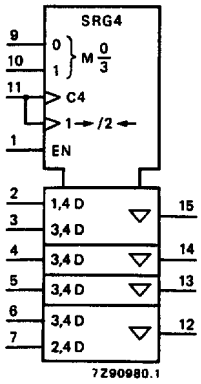


Fig.3 IEC logic symbol.

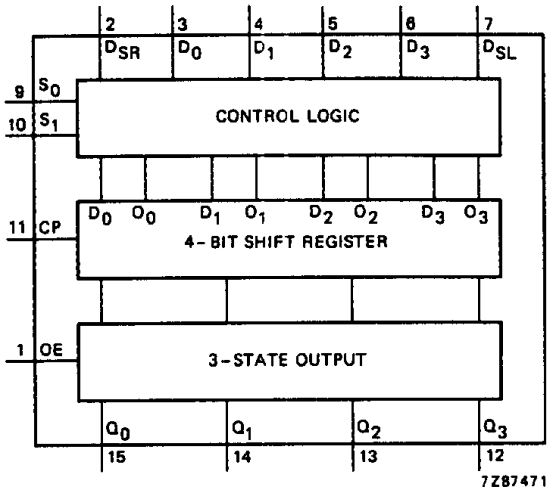


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS (OE = HIGH)					OUTPUTS at t_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	D_0 to D_3	Q_0	Q_1	Q_2	Q_3
reset	L	L	X	X	X	L	L	L	L
shift left	H H	L L	X X	L H	X X	Q_1 Q_1	Q_2 Q_2	Q_3 Q_3	L H
shift right	L L	H H	L H	X X	X X	L H	Q_0 Q_0	Q_1 Q_1	Q_2 Q_2
parallel load	H H	H H	X X	X X	L H	L H	L H	L H	L H

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   t_{n+1} = state after next LOW-to-HIGH transition of CP

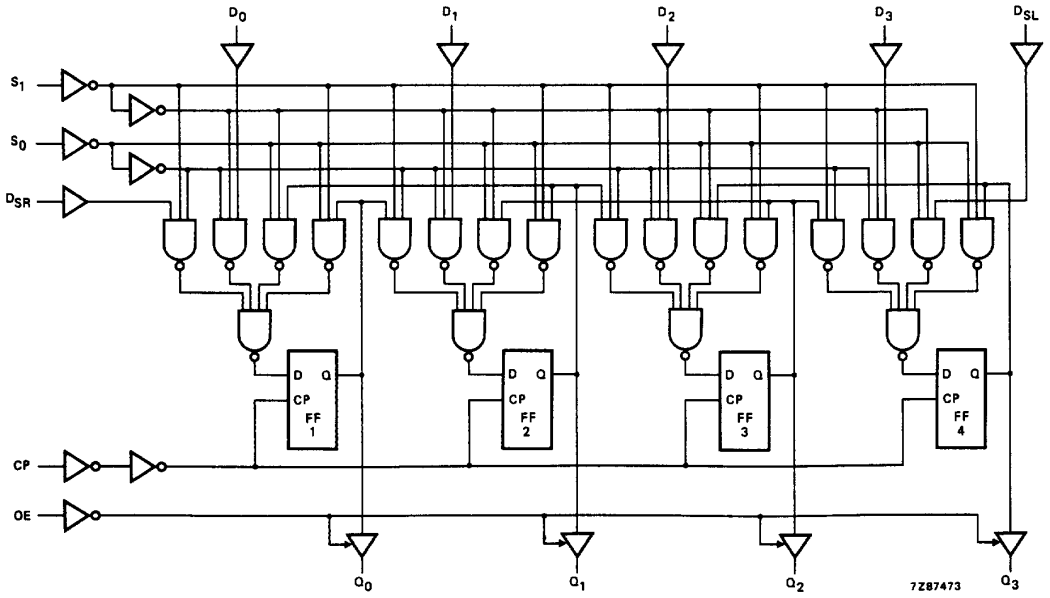


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n		44 16 13	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig.6
t_{PZH}/ t_{PZL}	3-state output enable time OE to Q_n		33 12 10	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{PHZ}/ t_{PLZ}	3-state output disable time OE to Q_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{THL}/ t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t_W	clock pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t_{su}	set-up time D_n, D_{SR}, D_{SL} to CP	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time S_0, S_1 to CP	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_h	hold time D_n, D_{SR}, D_{SL} to CP	2 2 2	−8 −3 −2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.8
t_h	hold time S_0, S_1 to CP	2 2 2	−14 −5 −4		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.8
f_{max}	maximum clock pulse frequency	6.0 30 35	19 56 67		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

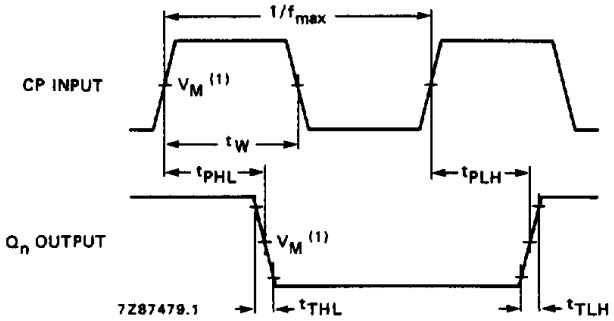
INPUT	UNIT LOAD COEFFICIENT
D_0 to D_3	0.35
D_{SR}, D_{SL}	0.35
CP	0.35
S_0, S_1	0.70
OE	1.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

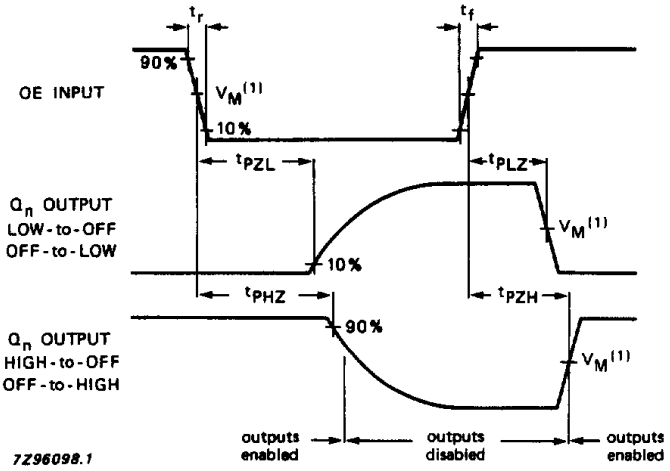
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n		18	34		43		51	ns	4.5	Fig.6
t_{PZH}/ t_{PZL}	3-state output enable time OE to Q_n		12	30		38		45	ns	4.5	Fig.8
t_{PHZ}/ t_{PLZ}	3-state output disable time OE to Q_n		21	35		44		53	ns	4.5	Fig.8
t_{THL}/ t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6
t_W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.6
t_{su}	set-up time D_n, D_{SR}, D_{SL} to CP	16	8		20		24		ns	4.5	Fig.8
t_{su}	set-up time S_0, S_1 to CP	20	9		25		30		ns	4.5	Fig.8
t_h	hold time D_n, D_{SR}, D_{SL} to CP	2	−2		2		2		ns	4.5	Fig.8
t_h	hold time S_0, S_1 to CP	2	−5		2		2		ns	4.5	Fig.8
f_{max}	maximum clock pulse frequency	27	52		22		18		MHz	4.5	Fig.6

AC WAVEFORMS



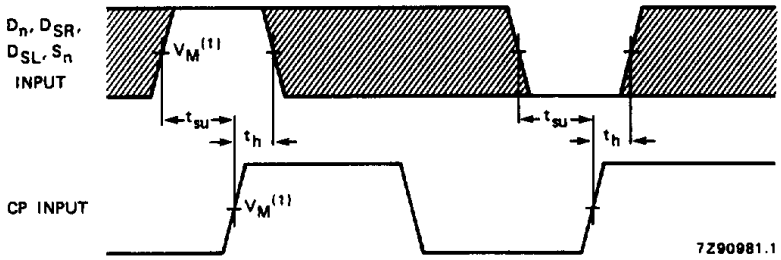
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the set-up and hold times from the D_n, D_{SR}, D_{SL} and S_n inputs to the clock (CP).

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.