

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT7597**

**8-bit shift register with input latches**

Product specification  
File under Integrated Circuits, IC06

December 1990

## 8-bit shift register with input latches

## 74HC/HCT7597

## FEATURES

- 8-bit parallel input latches
- Shift register has direct overriding load and clear
- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT7597 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT7597 both consist of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register.

When  $\overline{LE}$  is LOW, data at the  $D_n$  inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When  $\overline{LE}$  is HIGH the latches store the information that was present at the D-inputs, a set-up time preceding the LOW-to-HIGH transition of  $\overline{LE}$ .

The shift register has a positive edge-triggered clock, direct load (from storage) and clear inputs.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay	$C_L = 15\text{ pF}; V_{CC} = 5\text{ V}$			
	$SH_{CP}$ to Q		15	17	ns
	$\overline{LE}$ to Q		22	27	ns
	$\overline{PL}$ to Q		20	23	ns
	$D_7$ to Q		20	24	ns
$f_{max}$	maximum clock frequency $SH_{CP}$		99	79	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per package	notes 1, 2	29	30	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF;  $V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$ ; for HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

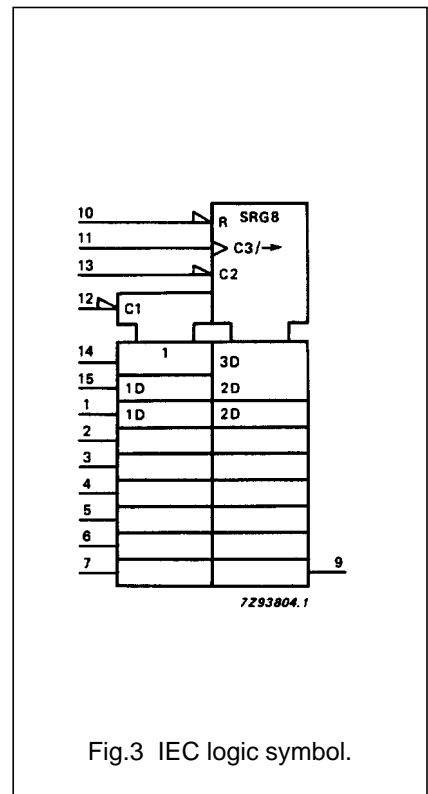
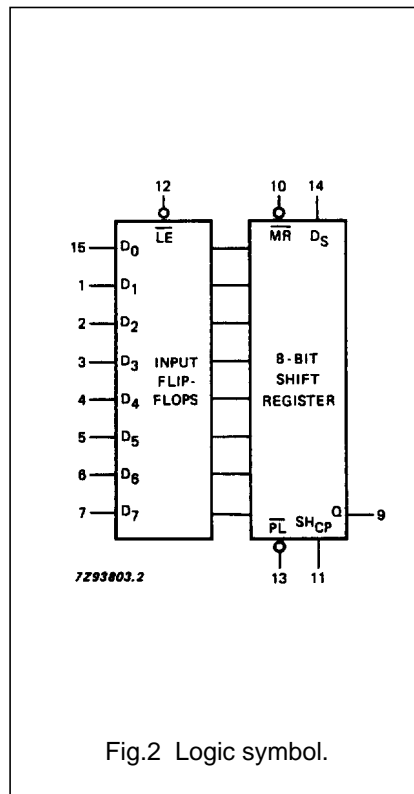
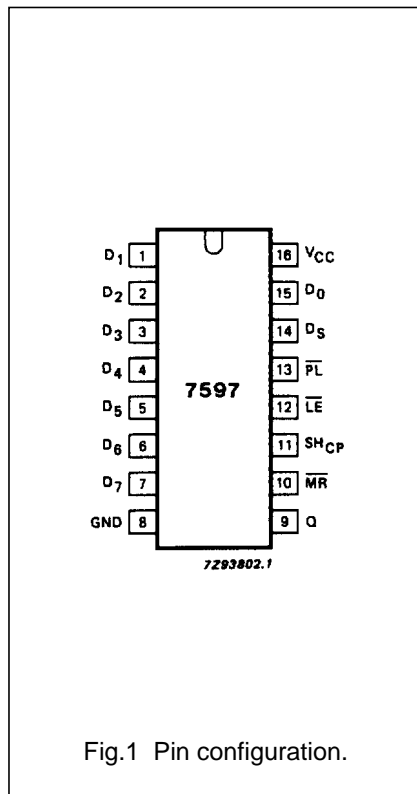
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# 8-bit shift register with input latches

# 74HC/HCT7597

## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8	GND	ground (0 V)
9	Q	serial data output
10	$\overline{\text{MR}}$	asynchronous reset input (active LOW)
11	SH <sub>CP</sub>	shift clock input (LOW-to-HIGH, edge-triggered)
12	$\overline{\text{LE}}$	latch enable input (active LOW)
13	$\overline{\text{PL}}$	parallel load input (active LOW)
14	D <sub>S</sub>	serial data input
15, 1, 2, 3, 4, 5, 6, 7	D <sub>0</sub> to D <sub>7</sub>	parallel data inputs
16	V <sub>CC</sub>	positive supply voltage



8-bit shift register with input latches

74HC/HCT7597

FUNCTION TABLE

$\overline{LE}$	$SH_{CP}$	$\overline{PL}$	$\overline{MR}$	FUNCTION
L	X	X	X	data enabled to input latches (transparent)
H	X	X	X	data stored into latches (non-transparent)
X	X	L	H	data transferred from input latches to shift register
X	X	L	L	invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	shift register cleared
X	↑	H	H	shift register clocked $Q_n = Q_{n-1}$ , $Q_0 = D_S$

Notes

- H = HIGH voltage level  
 L = LOW voltage level  
 X = don't care  
 ↑ = LOW-to-HIGH CP transition

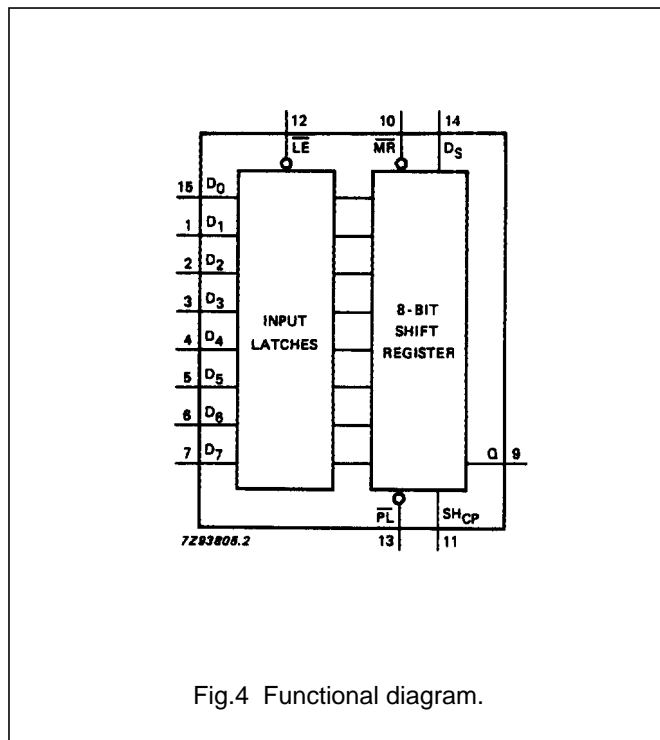


Fig.4 Functional diagram.

# 8-bit shift register with input latches

74HC/HCT7597

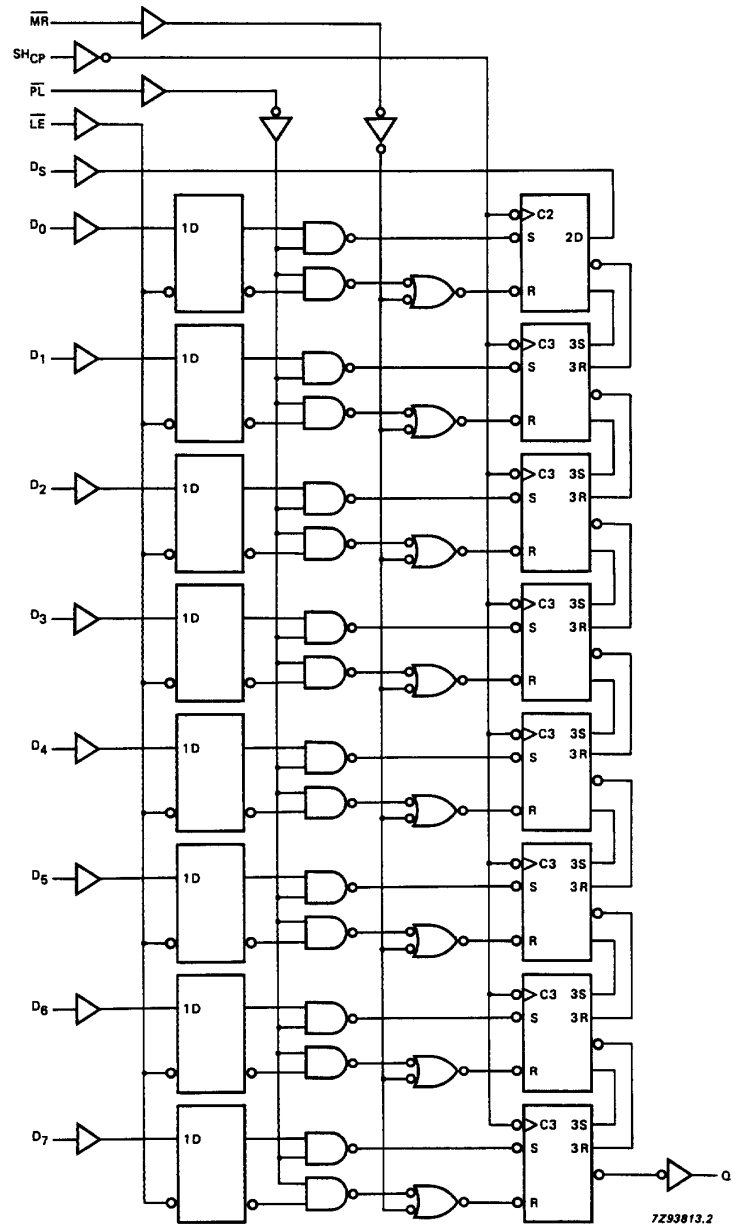


Fig.5 Logic diagram.

# 8-bit shift register with input latches

74HC/HCT7597

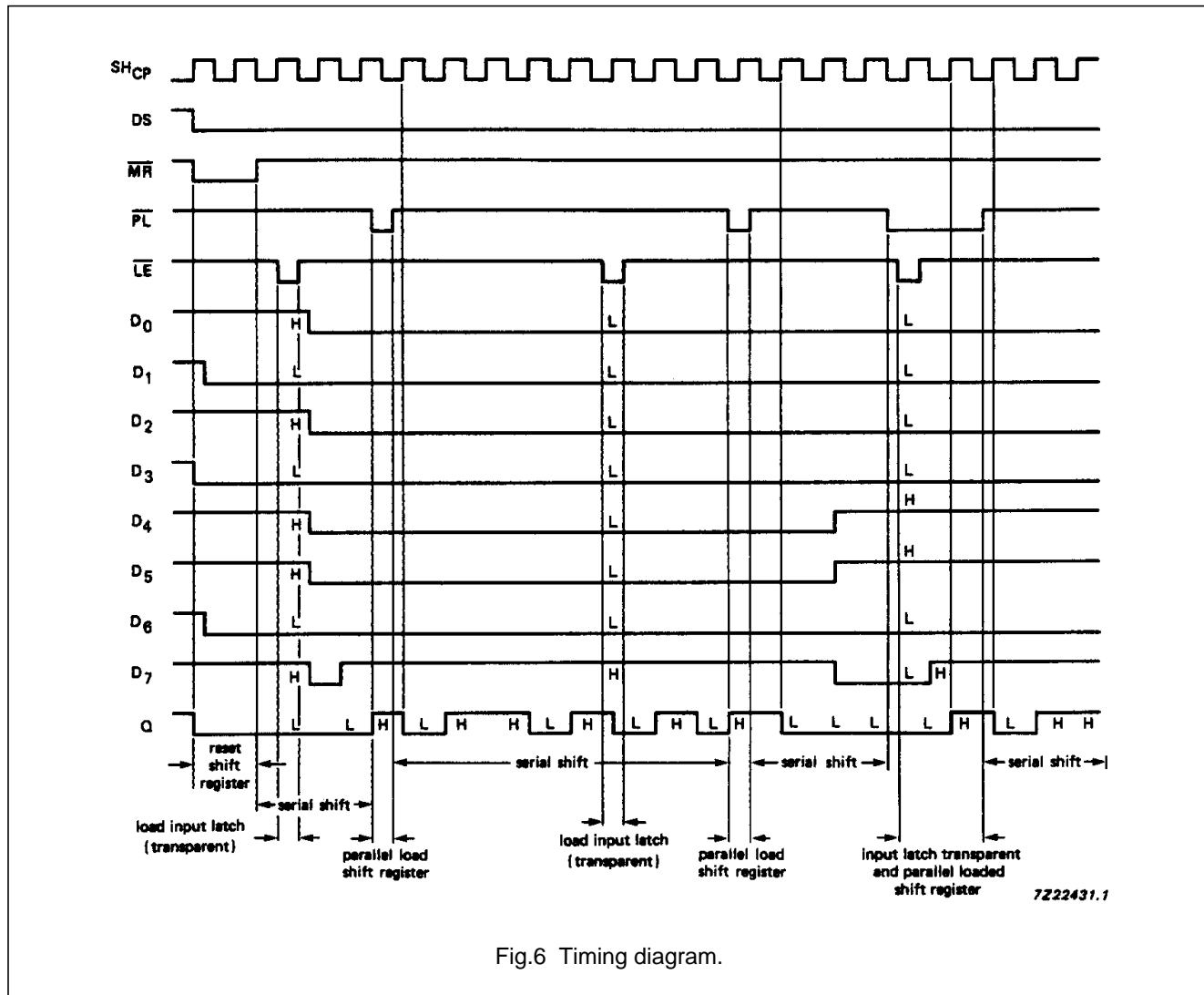


Fig.6 Timing diagram.

## 8-bit shift register with input latches

## 74HC/HCT7597

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay SH <sub>CP</sub> to Q		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub>	propagation delay MR to Q		52 19 15	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{\text{LE}}$ to Q		72 26 21	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $\overline{\text{PL}}$ to Q		63 23 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay D <sub>7</sub> to Q		63 23 18	190 38 32		240 48 41		285 57 48	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	SH <sub>CP</sub> pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	$\overline{\text{LE}}$ pulse width LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	$\overline{\text{MR}}$ pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>w</sub>	$\overline{\text{PL}}$ pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>rem</sub>	removal time $\overline{\text{MR}}$ to SH <sub>CP</sub>	50 10 9	-3 -1 -1		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.7

## 8-bit shift register with input latches

## 74HC/HCT7597

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>rem</sub>	removal time MR to PL	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.7
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	80 16 14	6 2 2		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>su</sub>	set-up time D <sub>S</sub> to SH <sub>CP</sub>	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>su</sub>	set-up time PL to SH <sub>CP</sub>	80 16 14	8 3 2		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>h</sub>	hold time D <sub>n</sub> to LE	4 4 4	-3 -1 -1		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig.7
t <sub>h</sub>	hold time D <sub>S</sub> to SH <sub>CP</sub>	2 2 2	-8 -3 -2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.7
t <sub>h</sub>	hold time PL to SH <sub>CP</sub>	2 2 2	-8 -3 -2		2 2 2		2 2 2		ns	2.0 4.5 6.0	Fig.7
f <sub>max</sub>	maximum pulse frequency SH <sub>CP</sub>	6.0 30 35	30 90 107		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7



## 8-bit shift register with input latches

## 74HC/HCT7597

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

$I_{CC}$  category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.

To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$D_S$	0.25
$D_n$	0.40
$\overline{PL}$ , $\overline{MR}$	1.50
$\overline{LE}$ , $SH_{CP}$	1.50

**AC CHARACTERISTICS FOR 74HCT**

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HCT							$V_{CC}$ (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay $SH_{CP}$ to Q		20	35		44		53	ns	4.5	Fig.7
$t_{PHL}$	propagation delay $\overline{MR}$ to Q		25	42		53		63	ns	4.5	Fig.7
$t_{PHL}/t_{PLH}$	propagation delay $\overline{LE}$ to Q		31	53		66		80	ns	4.5	Fig.7
$t_{PHL}/t_{PLH}$	propagation delay $\overline{PL}$ to Q		27	46		58		69	ns	4.5	Fig.7
$t_{PHL}/t_{PLH}$	propagation delay $D_7$ to Q		28	49		61		74	ns	4.5	Fig.7
$t_{THL}/t_{TLH}$	output transition time		7	15		19		22	ns	4.5	Fig.7
$t_W$	$SH_{CP}$ pulse width HIGH or LOW	16	6		20		24		ns	4.5	Fig.7
$t_W$	$\overline{LE}$ pulse width LOW	16	7		20		24		ns	4.5	Fig.7
$t_W$	$\overline{MR}$ pulse width LOW	20	11		25		30		ns	4.5	Fig.7
$t_W$	$\overline{PL}$ pulse width LOW	18	9		23		27		ns	4.5	Fig.7
$t_{rem}$	removal time $\overline{MR}$ to $SH_{CP}$	10	-1		13		15		ns	4.5	Fig.7
$t_{rem}$	removal time $\overline{MR}$ to $\overline{PL}$	20	9		25		30		ns	4.5	Fig.7

## 8-bit shift register with input latches

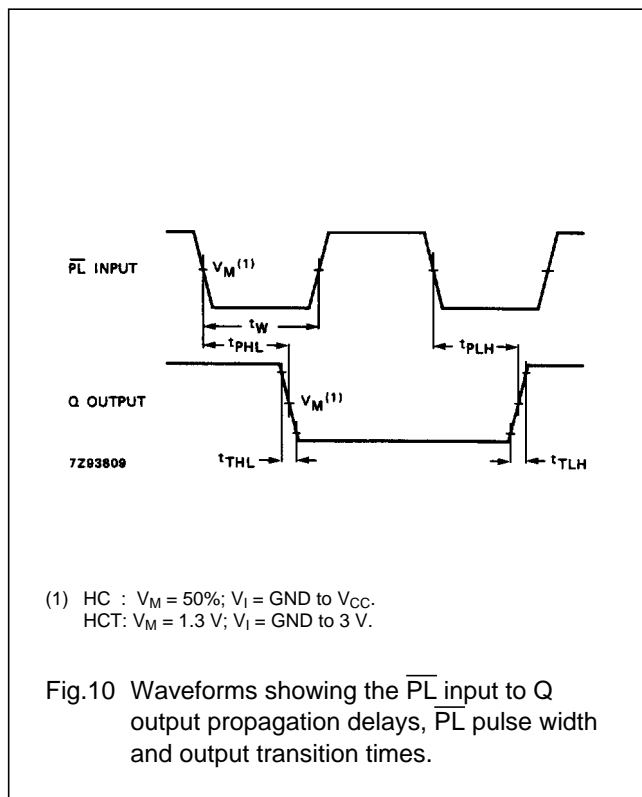
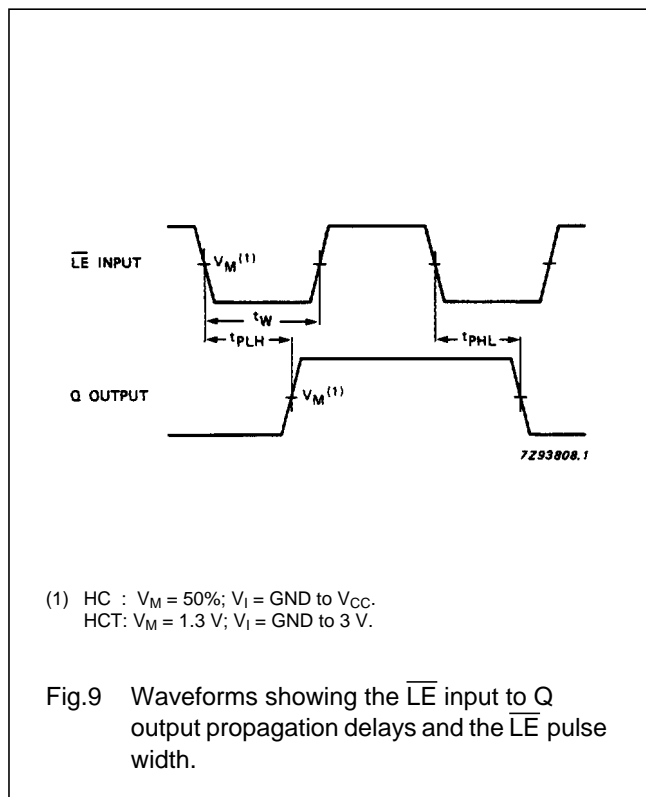
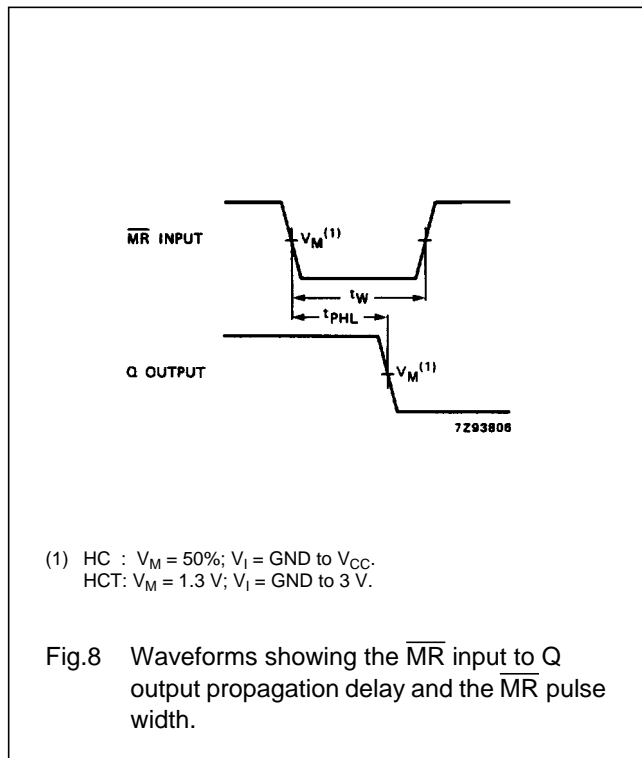
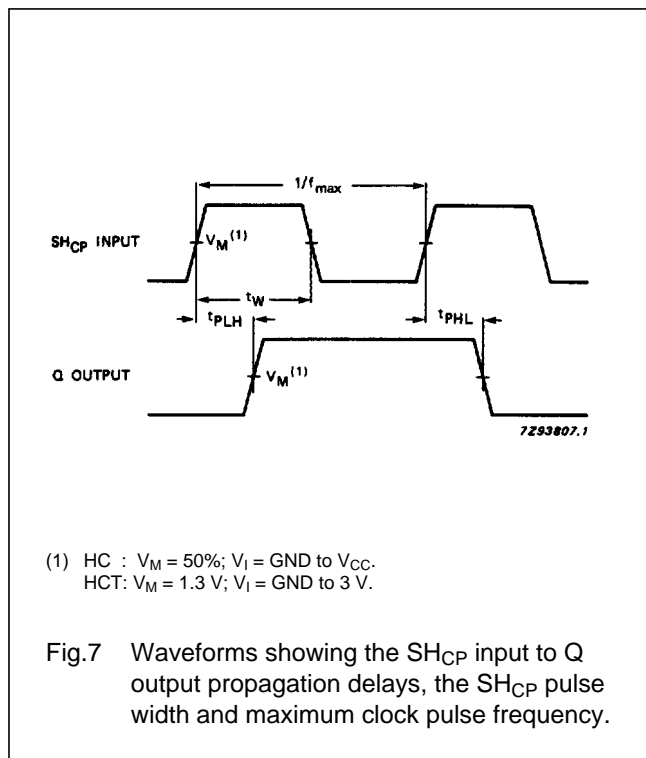
## 74HC/HCT7597

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>su</sub>	set-up time D <sub>n</sub> to LE	16	5		20		24		ns	4.5	Fig.7
t <sub>su</sub>	set-up time D <sub>S</sub> to SH <sub>CP</sub>	16	5		20		24		ns	4.5	Fig.7
t <sub>su</sub>	set-up time PL to SH <sub>CP</sub>	16	3		20		24		ns	4.5	Fig.7
t <sub>h</sub>	hold time D <sub>n</sub> to LE	4	-2		4		4		ns	4.5	Fig.7
t <sub>h</sub>	hold time D <sub>S</sub> to SH <sub>CP</sub>	2	-4		2		2		ns	4.5	Fig.7
t <sub>h</sub>	hold time PL to SH <sub>CP</sub>	2	-3		2		2		ns	4.5	Fig.7
f <sub>max</sub>	maximum pulse frequency SH <sub>CP</sub>	30	72		24		20		MHz	4.5	Fig.7

8-bit shift register with input latches

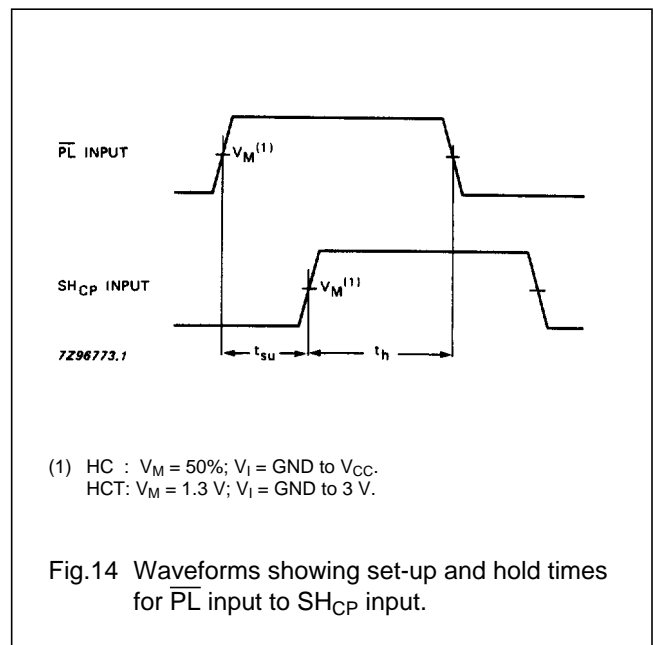
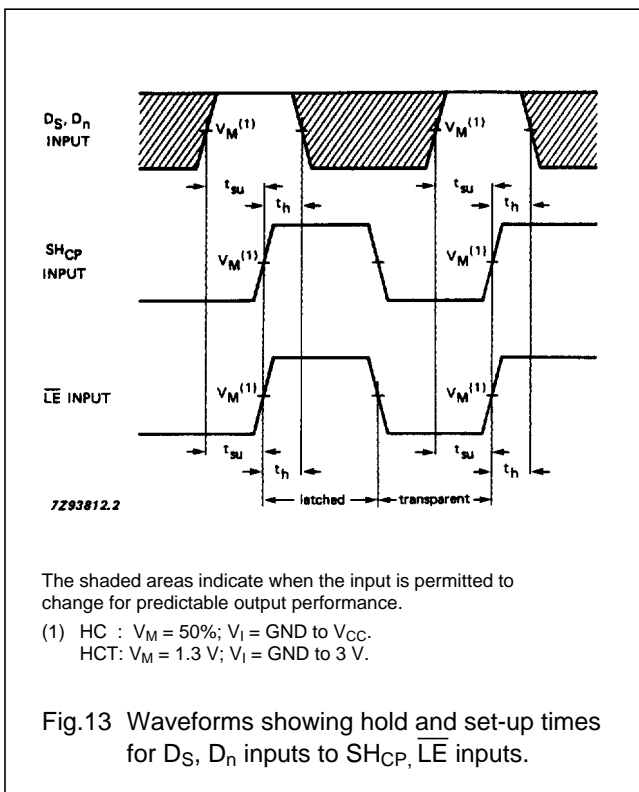
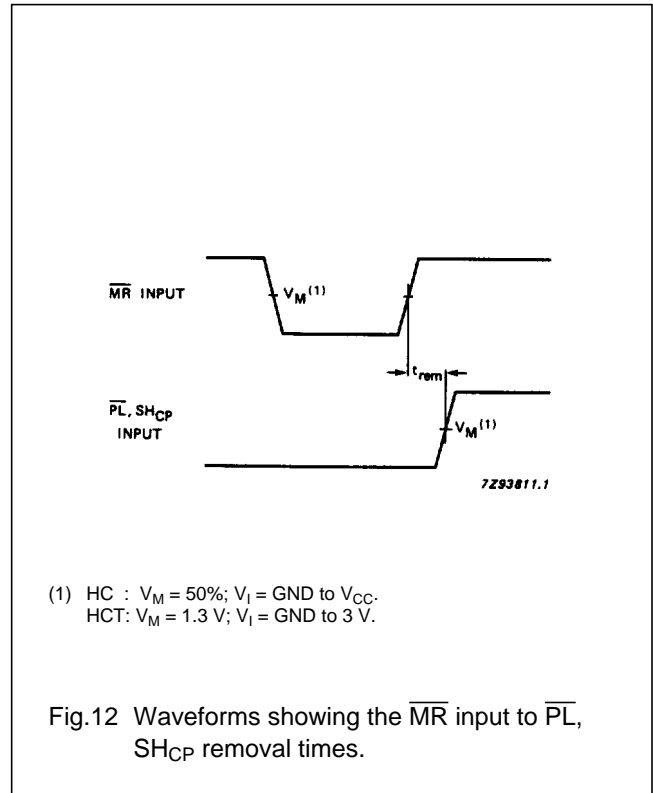
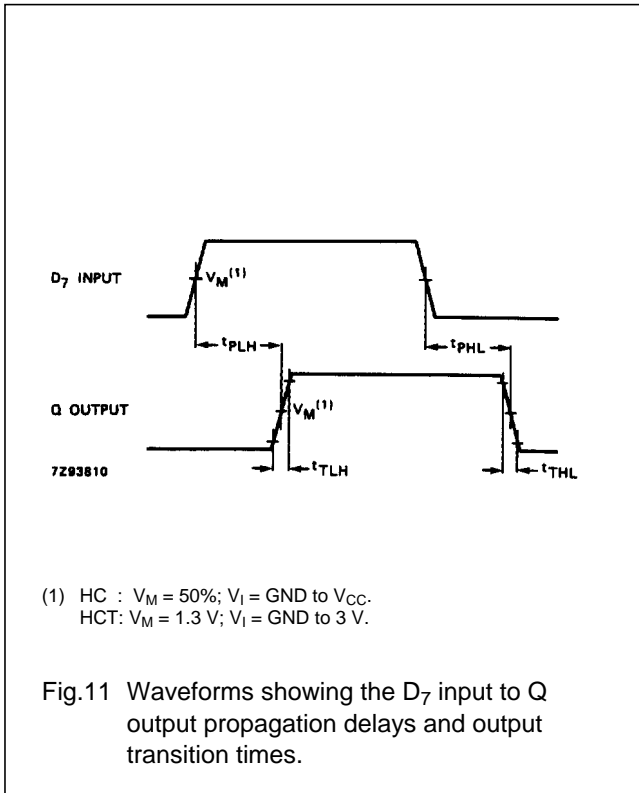
74HC/HCT7597

AC WAVEFORMS



8-bit shift register with input latches

74HC/HCT7597



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".