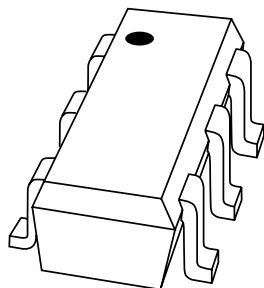


DATA SHEET



BF1102; BF1102R Dual N-channel dual gate MOS-FETs

Product specification
Supersedes data of 1999 Jul 01

2000 Apr 11

Dual N-channel dual gate MOS-FETs

BF1102; BF1102R

FEATURES

- Two low noise gain controlled amplifiers in a single package
- Specially designed for 5 V applications
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio.

APPLICATIONS

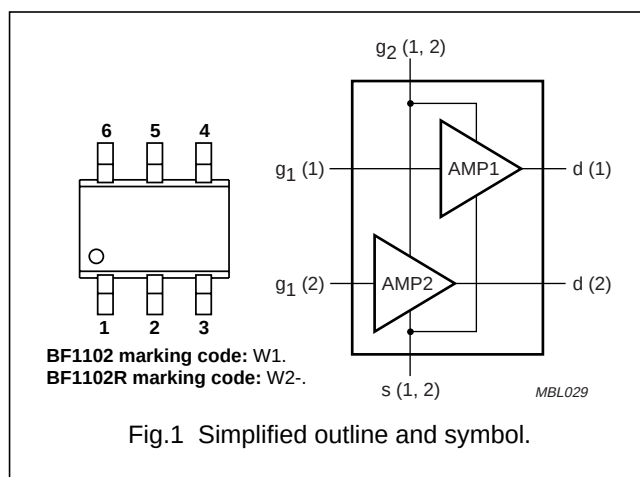
Gain controlled low noise amplifier for VHF and UHF applications such as television tuners and professional communications equipment.

DESCRIPTION

The BF1102 and BF1102R are both two equal dual gate MOS-FETs which have a shared source pin and a shared gate 2 pin. Both devices have interconnected source and substrate; an internal bias circuit enables DC stabilization and a very good cross-modulation performance at 5 V supply voltage; integrated diodes between the gates and source protect against excessive input voltage surges. Both devices have a SOT363 micro-miniature plastic package.

PINNING - SOT363

PIN	DESCRIPTION	
	BF1102	BF1102R
1	gate 1 (1)	gate 1 (1)
2	gate 2 (1 and 2)	source (1 and 2)
3	drain (1)	drain (1)
4	drain (2)	drain (2)
5	source (1 and 2)	gate 2 (1 and 2)
6	gate 1 (2)	gate 1 (2)



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET unless otherwise specified						
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current (DC)		–	–	40	mA
P_{tot}	total power dissipation	$T_s \leq 102^\circ\text{C}$; note 1	–	–	200	mW
$ y_{fs} $	forward transfer admittance	$I_D = 15\text{ mA}$	36	43	–	mS
C_{ig1-s}	input capacitance at gate 1	$I_D = 15\text{ mA}$	–	2.8	3.6	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	30	50	fF
F	noise figure	$f = 800\text{ MHz}$	–	2	2.8	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	100	–	–	dB μ V
T_j	operating junction temperature		–	–	150	$^\circ\text{C}$

Note

1. T_s is the temperature at the soldering point of the source lead.

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

Dual N-channel dual gate MOS-FETs

BF1102; BF1102R

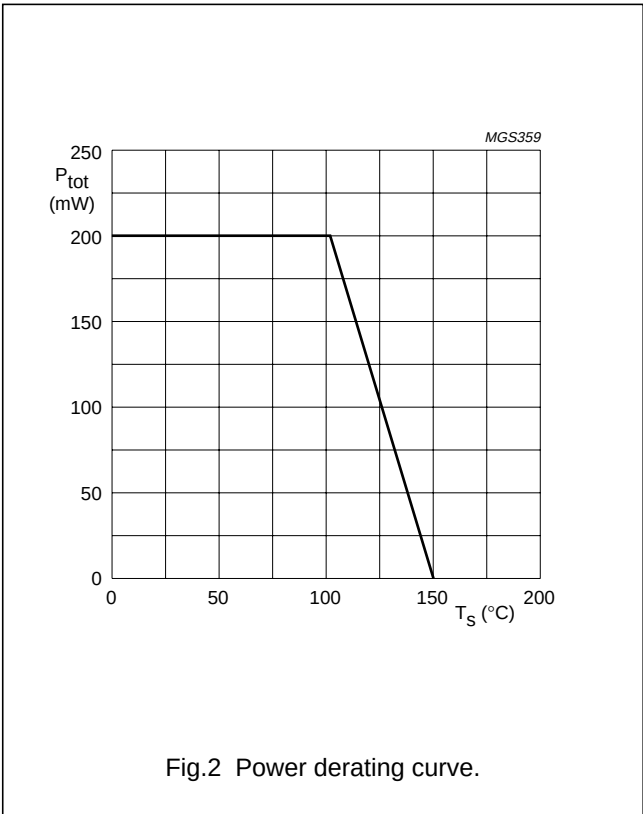
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET unless otherwise specified					
V _{DS}	drain-source voltage		–	7	V
I _D	drain current (DC)		–	40	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation	T _s ≤ 102 °C	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-s}	thermal resistance from junction to soldering point	240	K/W



Dual N-channel dual gate MOS-FETs

BF1102; BF1102R

STATIC CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET unless otherwise specified					
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\text{ }\mu\text{A}$	7	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{GS} = V_{DS} = 0$; $I_{G1-S} = 10\text{ mA}$	6	15	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{GS} = V_{DS} = 0$; $I_{G2-S} = 5\text{ mA}$	6	15	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{DS} = 5\text{ V}$; $V_{G1-S} = 4\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_G = 120\text{ k}\Omega$; note 1	12	20	mA
I_{G1-S}	gate 1 cut-off current	$V_{G1-S} = 5\text{ V}$; $V_{G2-S} = V_{DS} = 0$	–	50	nA
I_{G2-S}	gate 2 cut-off current	$V_{G2-S} = 5\text{ V}$; $V_{G1-S} = V_{DS} = 0$	–	20	nA

Note

1. R_{G1} connects gate 1 to $V_{GG} = 5\text{ V}$.

DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 15\text{ mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET unless otherwise specified (note 1)						
$ y_{fs} $	forward transfer admittance	$T_j = 25\text{ }^{\circ}\text{C}$	36	43	50	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	2	2.8	3.6	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$; (note 2)	–	–	7	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	1.6	2.5	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	30	50	fF
F	noise figure	$f = 800\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	2	2.8	dB
X_{mod}	cross-modulation	$f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; (note 3) input level for $k = 1\%$ at 0 dB AGC input level for $k = 1\%$ at 40 dB AGC	85 100	– –	– –	dB μ V dB μ V

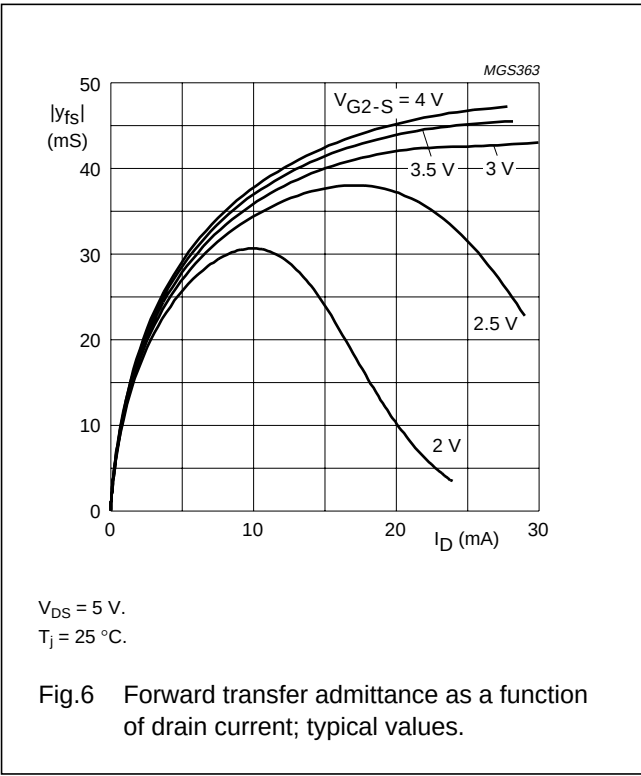
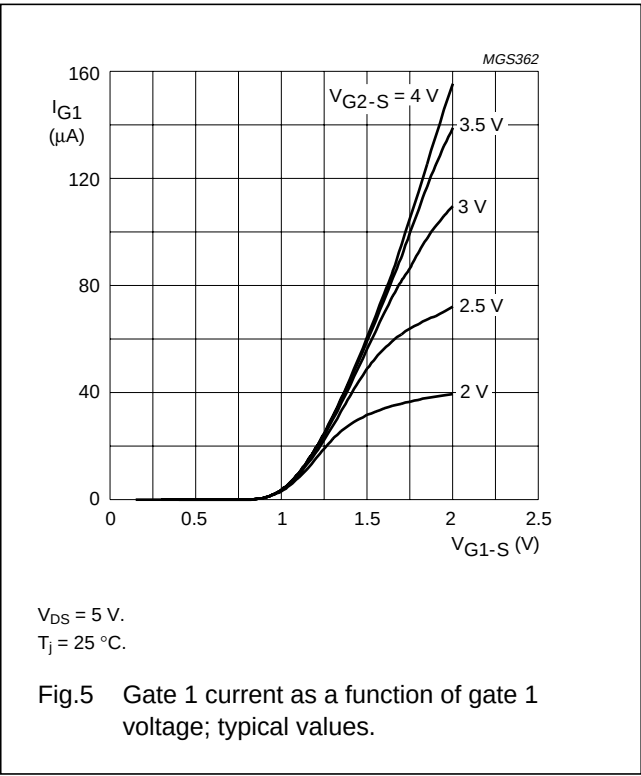
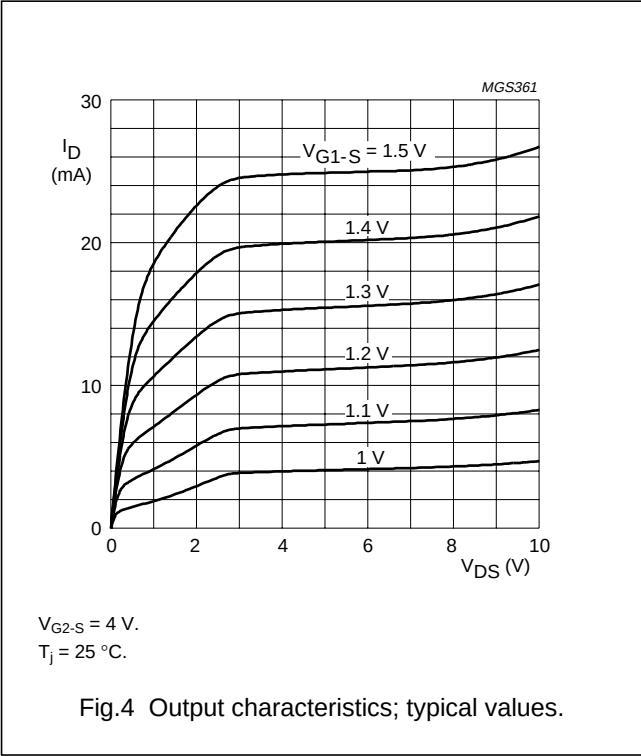
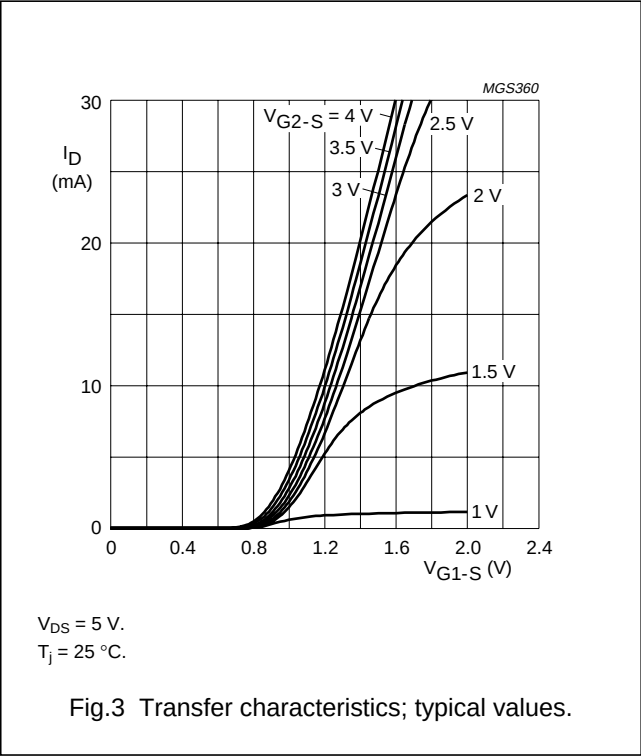
Notes

1. Not used MOS-FET: $V_{G1-S} = 0$; $V_{DS} = 0$.
2. Gate 2 capacitance of both MOS-FETs.
3. Measured in test circuit of Fig.20.

Dual N-channel dual gate MOS-FETs

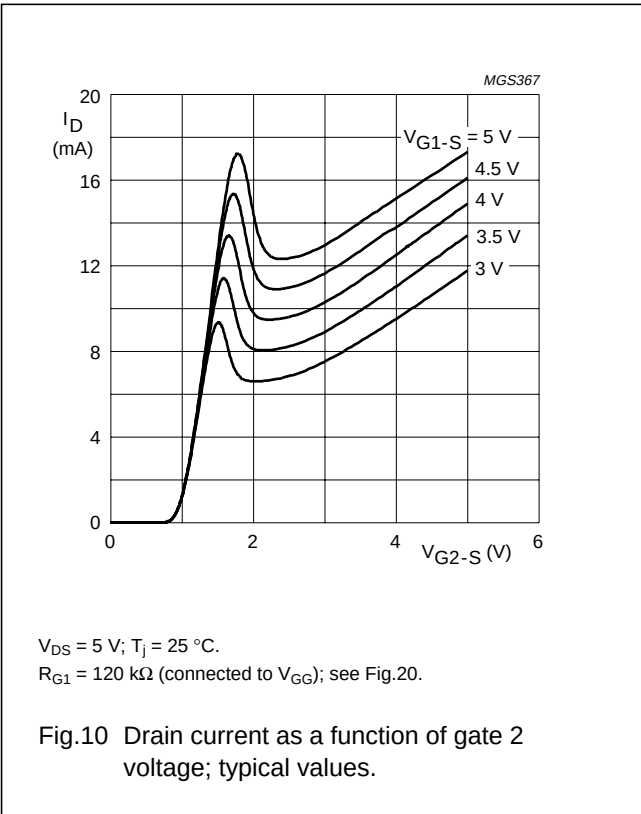
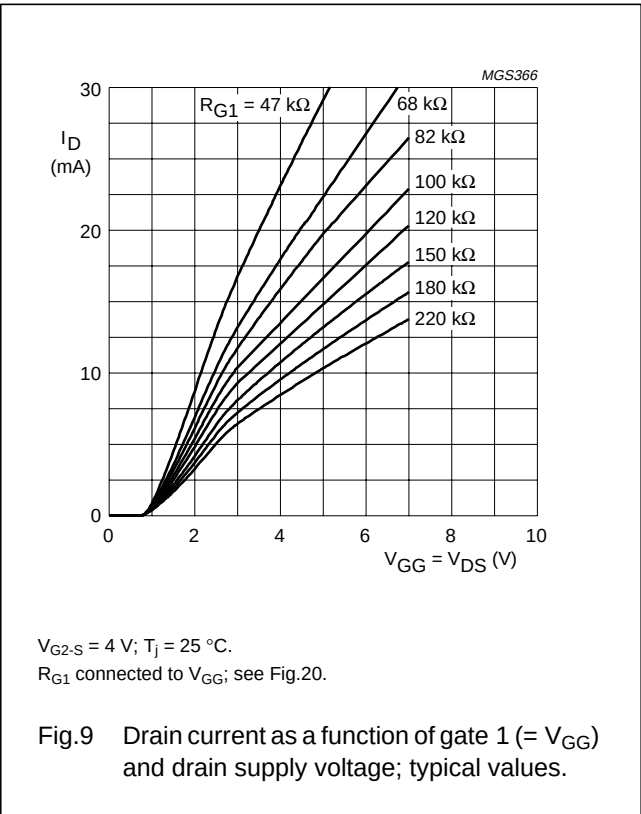
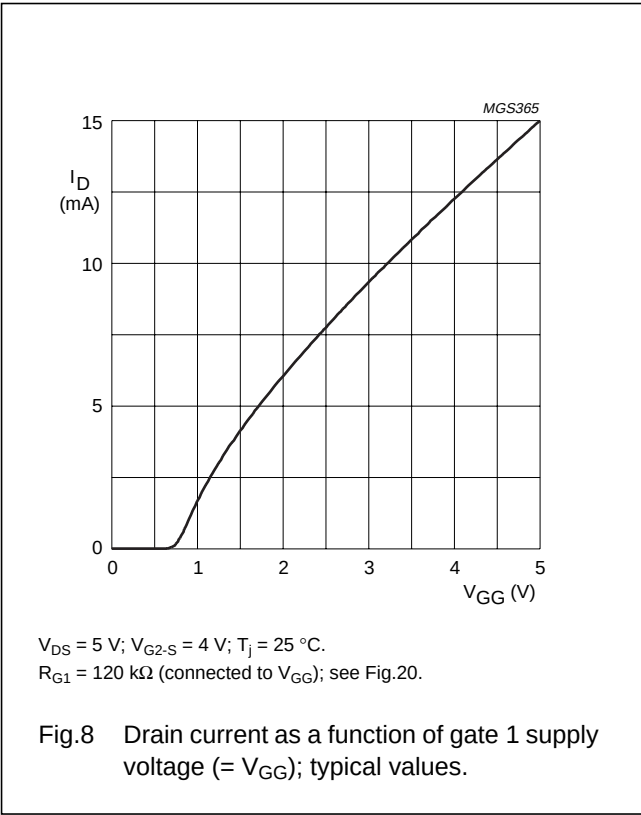
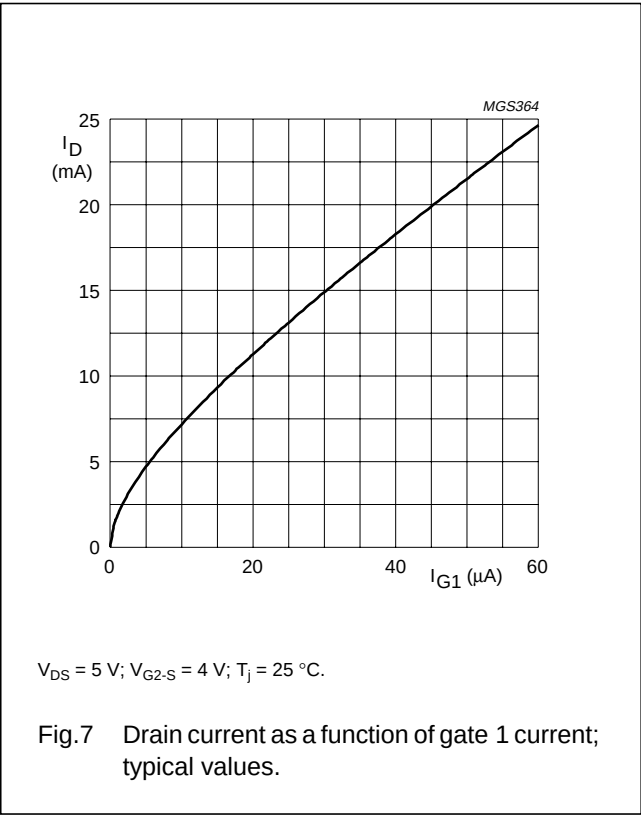
BF1102; BF1102R

ALL GRAPHS FOR ONE MOS-FET



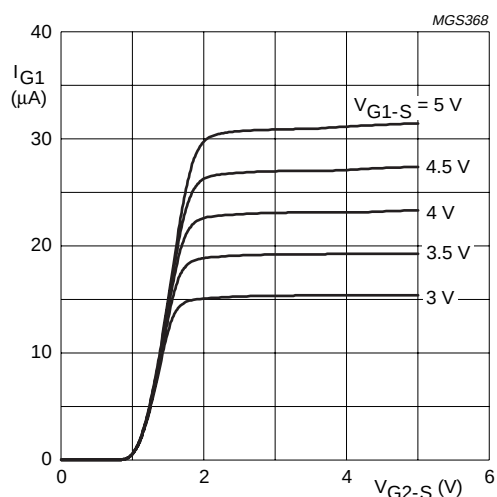
Dual N-channel dual gate MOS-FETs

BF1102; BF1102R



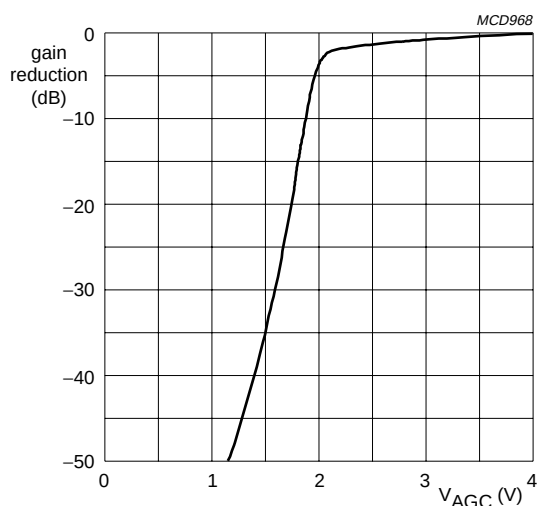
Dual N-channel dual gate MOS-FETs

BF1102; BF1102R



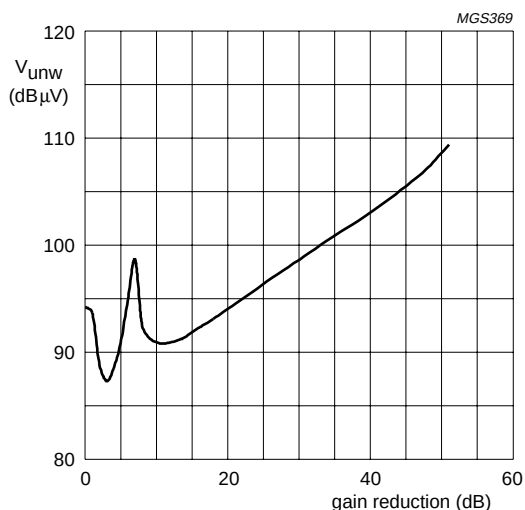
$V_{DS} = 5 \text{ V}$; $T_j = 25^\circ\text{C}$.
 $R_{G1} = 120 \text{ k}\Omega$ (connected to V_{GG}); see Fig.20.

Fig.11 Gate 1 current as a function of gate 2 voltage; typical values.



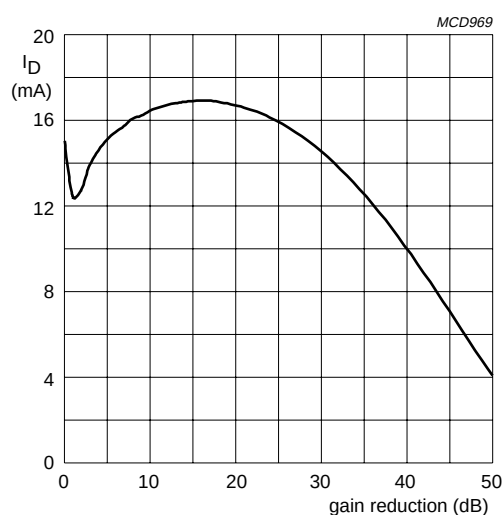
$V_{DS} = 5 \text{ V}$; $V_{GG} = 5 \text{ V}$; $f = 50 \text{ MHz}$; $T_{amb} = 25^\circ\text{C}$;
 $R_{G1} = 120 \text{ k}\Omega$ (connected to V_{GG}); see Fig.20.

Fig.12 Typical gain reduction as a function of the AGC voltage; see Fig.20.



$V_{DS} = 5 \text{ V}$; $V_{GG} = 5 \text{ V}$; $f_w = 50 \text{ MHz}$; $f_{unw} = 60 \text{ MHz}$; $T_{amb} = 25^\circ\text{C}$;
 $R_{G1} = 120 \text{ k}\Omega$ (connected to V_{GG}); see Fig.20.

Fig.13 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values.

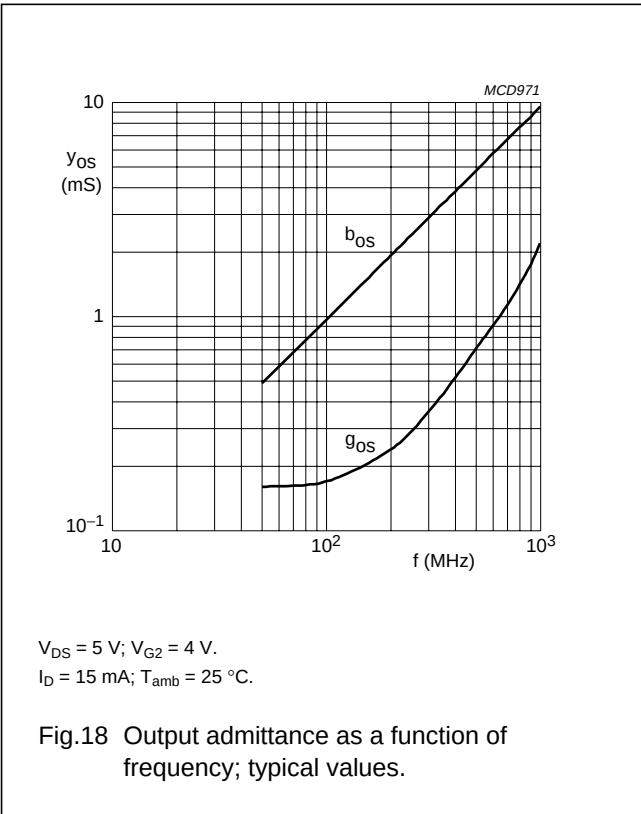
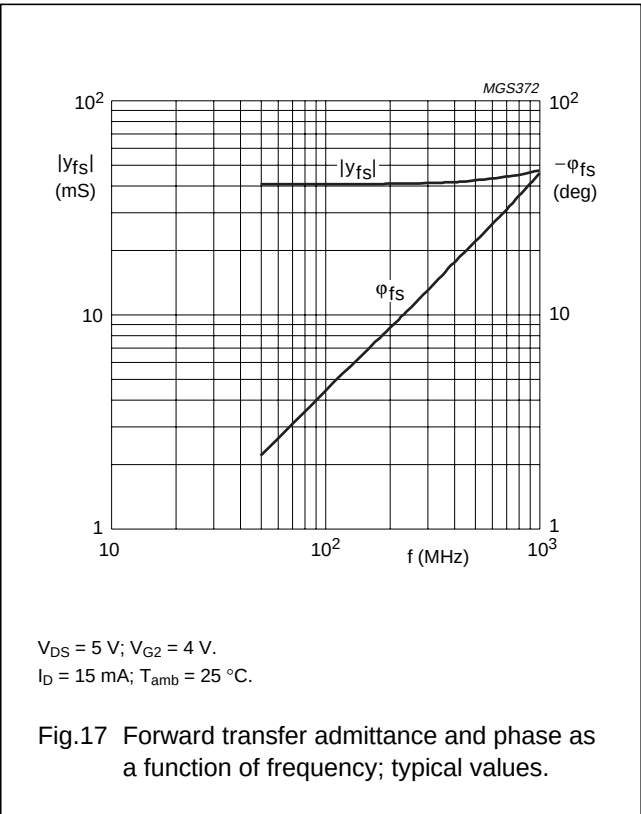
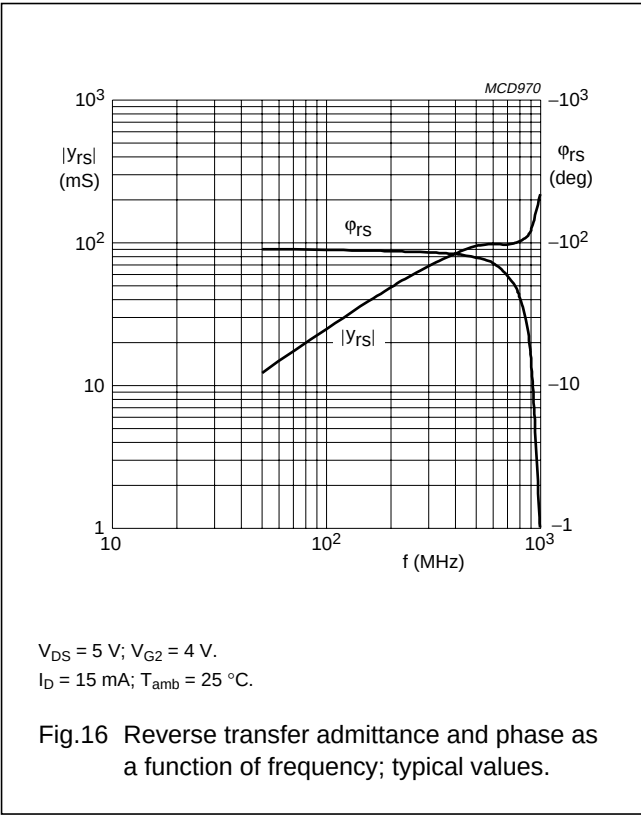
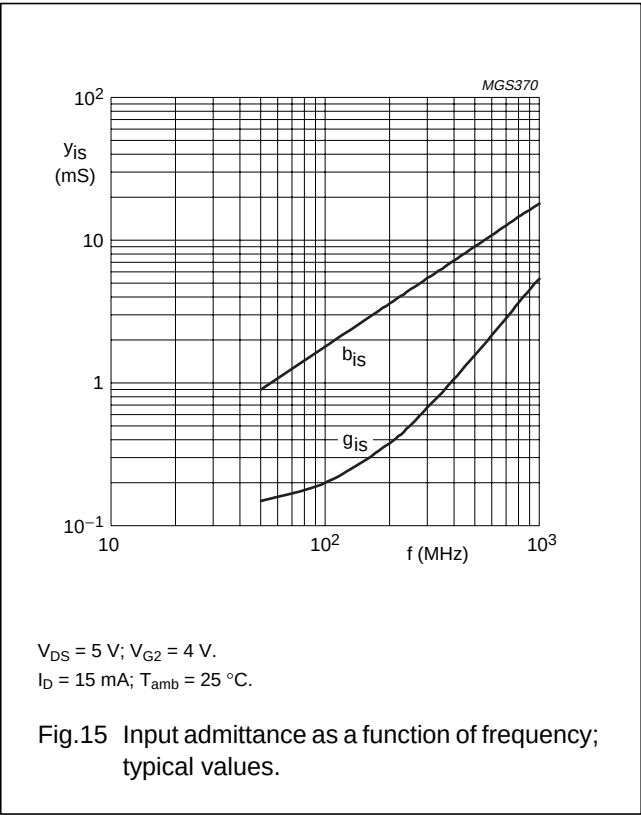


$V_{DS} = 5 \text{ V}$; $V_{GG} = 5 \text{ V}$; $f = 50 \text{ MHz}$; $T_{amb} = 25^\circ\text{C}$;
 $R_{G1} = 120 \text{ k}\Omega$ (connected to V_{GG}); see Fig.20.

Fig.14 Drain current as a function of gain reduction; typical values.

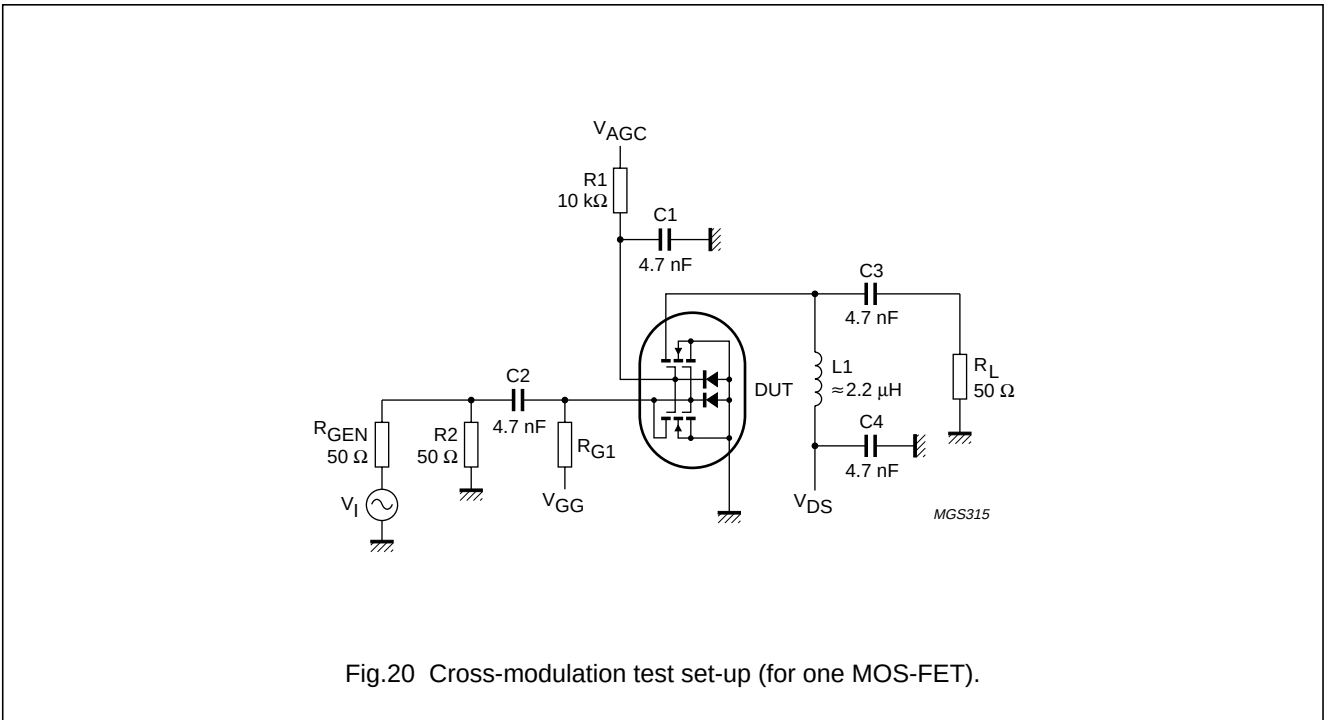
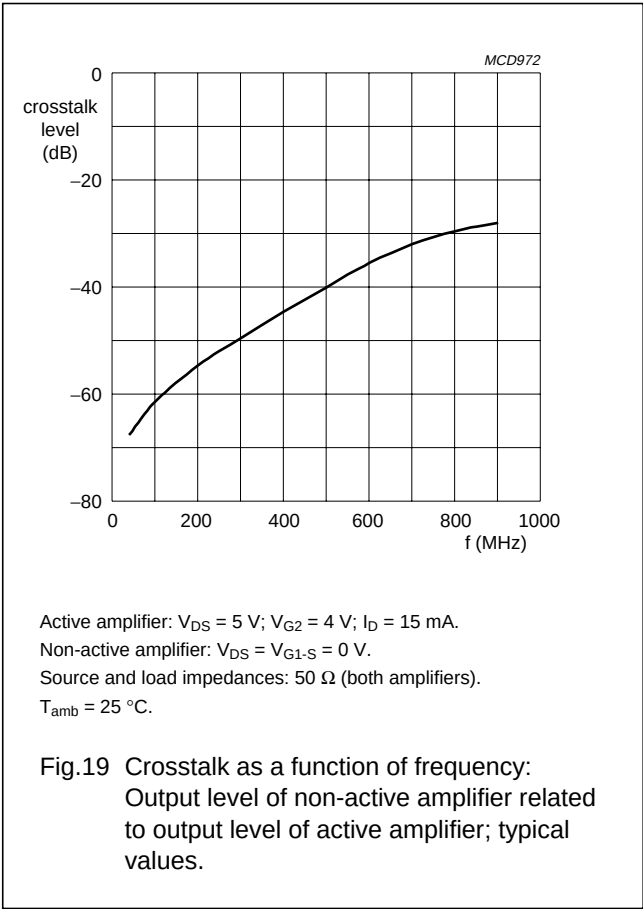
Dual N-channel dual gate MOS-FETs

BF1102; BF1102R



Dual N-channel dual gate MOS-FETs

BF1102; BF1102R



Dual N-channel dual gate MOS-FETs

BF1102; BF1102R

Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ °C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	-5.6	4.069	173.5	0.001	95.4	0.986	-3.0
100	0.981	-11.1	4.042	167.0	0.002	81.3	0.983	-6.0
200	0.961	-21.9	3.926	154.4	0.005	75.8	0.976	-12.0
300	0.933	-32.1	3.778	142.4	0.006	69.6	0.960	-17.7
400	0.899	-42.0	3.593	130.6	0.007	65.6	0.945	-23.2
500	0.867	-51.1	3.412	119.6	0.007	64.4	0.928	-29.1
600	0.834	-59.9	3.216	109.2	0.007	67.5	0.914	-34.1
700	0.805	-67.9	3.010	99.0	0.006	78.7	0.901	-39.8
800	0.779	-75.7	2.804	89.2	0.007	92.7	0.886	-45.1
900	0.758	-82.1	2.656	80.3	0.007	120.7	0.889	-49.7
1000	0.740	-89.0	2.509	69.9	0.009	125.5	0.890	-55.7

Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ °C}$

f (MHz)	F _{min} (dB)	Γ _{opt}		R _n (Ω)
		(ratio)	(deg)	
800	2	0.621	61.61	25.85

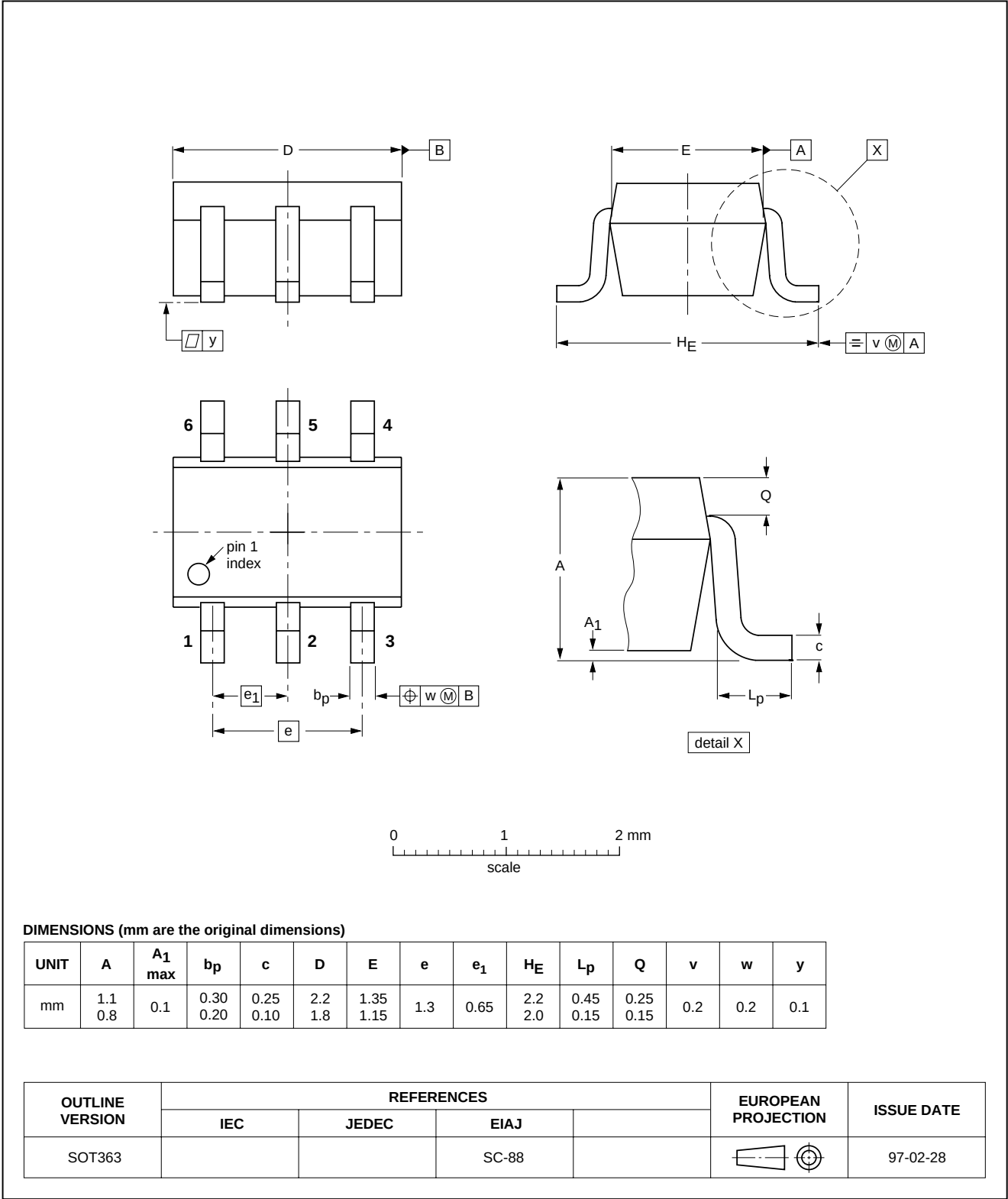
Dual N-channel dual gate MOS-FETs

BF1102; BF1102R

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



Dual N-channel dual gate MOS-FETs

BF1102; BF1102R

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS ⁽¹⁾
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Dual N-channel dual gate MOS-FETs

BF1102; BF1102R

NOTES

Dual N-channel dual gate MOS-FETs

BF1102; BF1102R

NOTES

Dual N-channel dual gate MOS-FETs

BF1102; BF1102R

NOTES

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