

DATA SHEET

BLW33 UHF linear power transistor

Product specification

August 1986

UHF linear power transistor

BLW33

DESCRIPTION

N-P-N silicon planar epitaxial transistor primarily intended for use in **linear u.h.f. amplifiers** for television transmitters and transposers. The **excellent d.c. dissipation properties** for class-A operation are obtained by means of diffused emitter ballasting resistors and a multi-base structure, providing an optimum temperature profile on the crystal

area. The combination of optimum thermal design and the application of **gold sandwich metallization** realizes excellent reliability properties.

The transistor has a ¼" capstan envelope with ceramic cap.

QUICK REFERENCE DATA

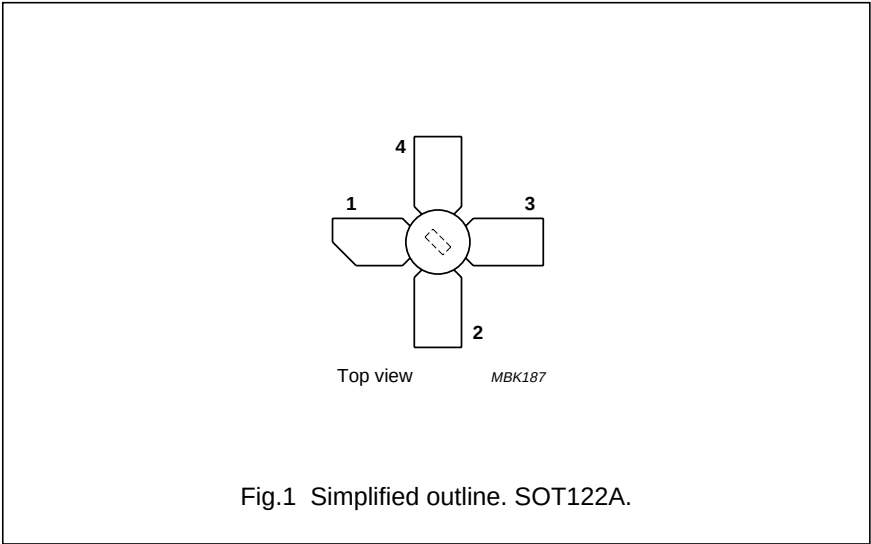
R.F. performance

MODE OF OPERATION	f _{vision} MHz	V _{CE} V	I _c mA	T _h °C	d _{im} ⁽¹⁾ dB	P _{o sync} ⁽¹⁾ W	G _p dB
class-A; linear amplifier	860	25	300	70	−60	> 1,0	> 10,0
	860	25	300	25	−60	typ. 1,15	typ. 10,5

Note

1. Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

PIN CONFIGURATION



PINNING - SOT122A.

PIN	DESCRIPTION
1	collector
2	emitter
3	base
4	emitter

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

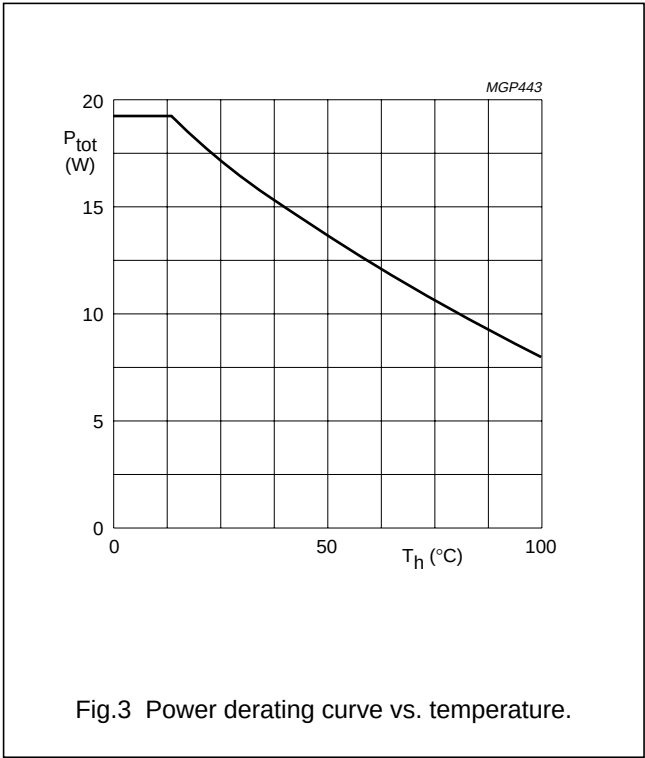
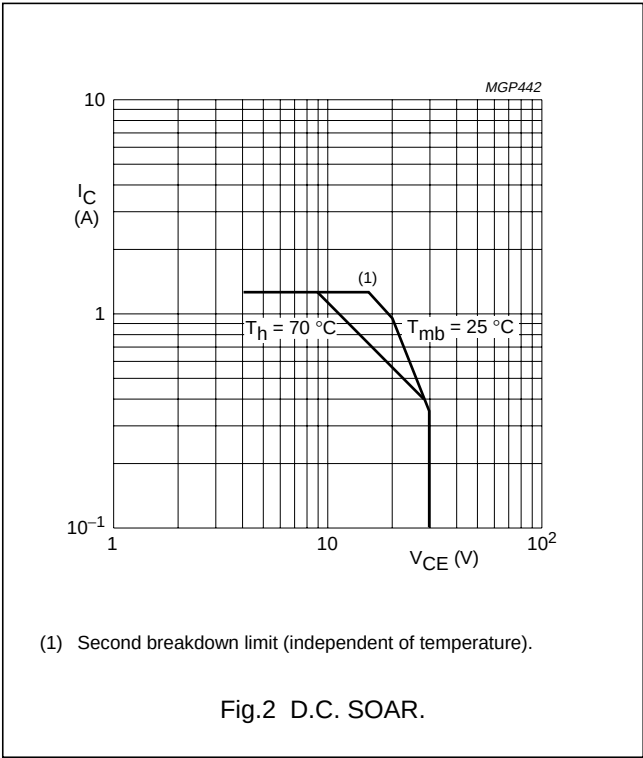
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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-emitter voltage			
(peak value); $V_{BE} = 0$	V_{CESM}	max.	50 V
open base	V_{CEO}	max.	30 V
Emitter-base voltage (open collector)	V_{EBO}	max.	4 V
Collector current			
d.c. or average	I_C	max.	1,25 A
(peak value); $f > 1$ MHz	I_{CM}	max.	1,9 A
Total power dissipation up to $T_{mb} = 25\text{ }^{\circ}\text{C}$	P_{tot}	max.	19,3 W
Storage temperature	T_{stg}		-65 to +150 $^{\circ}\text{C}$
Operating junction temperature	T_j	max.	200 $^{\circ}\text{C}$



THERMAL RESISTANCE (see Fig.4)

From junction to mounting base			
(dissipation = 7,5 W; $T_{mb} = 74,5\text{ }^{\circ}\text{C}$; i.e. $T_h = 70\text{ }^{\circ}\text{C}$)	$R_{th\ j-mb}$	=	10,1 K/W
From mounting base to heatsink	$R_{th\ mb-h}$	=	0,6 K/W

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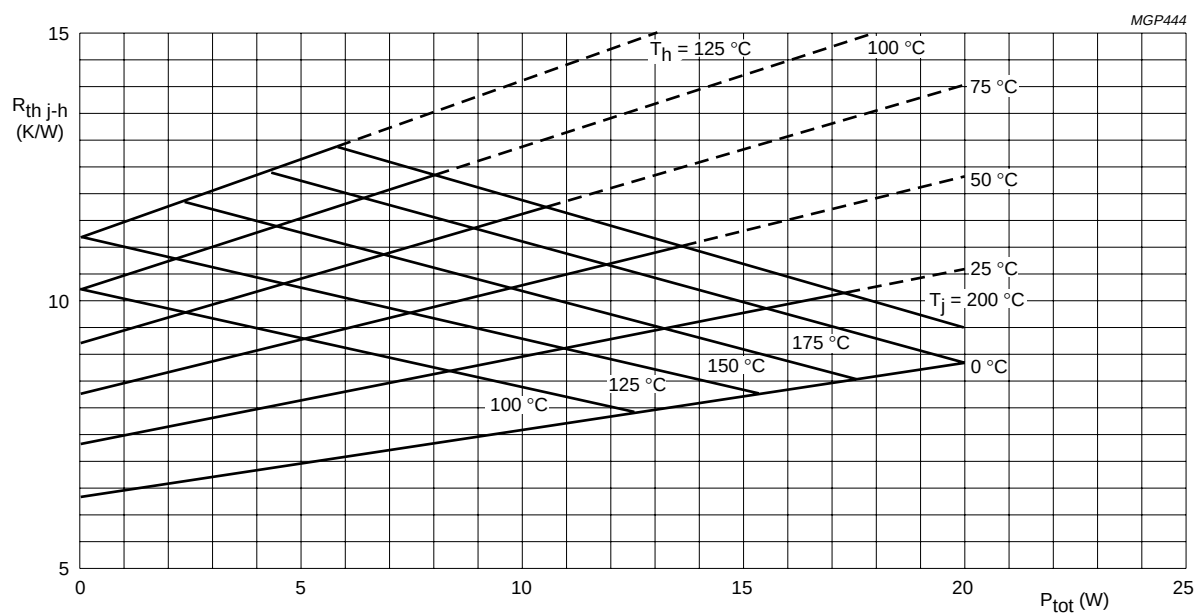


Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters. ($R_{th\ mb-h} = 0,6\text{ K/W.}$)

Example

Nominal class-A operation: $V_{CE} = 25\text{ V}$; $I_C = 300\text{ mA}$; $T_h = 70\text{ °C}$.

Fig.4 shows:	$R_{th\ j-h}$	max.	10,7 K/W
	T_j	max.	150 °C
Typical device:	$R_{th\ j-h}$	typ.	8,25 K/W
	T_j	typ.	132 °C

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CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Collector-emitter breakdown voltage

$V_{BE} = 0$; $I_C = 4\text{ mA}$

$V_{(BR)CES} > 50\text{ V}$

open base; $I_C = 30\text{ mA}$

$V_{(BR)CEO} > 30\text{ V}$

Emitter-base breakdown voltage

open collector; $I_E = 2\text{ mA}$

$V_{(BR)EBO} > 4\text{ V}$

Collector cut-off current

$V_{BE} = 0$; $V_{CE} = 30\text{ V}$

$I_{CES} < 1,0\text{ mA}$

$V_{BE} = 0$; $V_{CE} = 30\text{ V}$; $T_j = 175\text{ }^{\circ}\text{C}$

$I_{CES} < 2,5\text{ mA}$

D.C. current gain

$I_C = 300\text{ mA}$; $V_{CE} = 25\text{ V}$

$h_{FE} > 20$
typ. 40

$I_C = 300\text{ mA}$; $V_{CE} = 25\text{ V}$; $T_j = 175\text{ }^{\circ}\text{C}$

$h_{FE} < 120$

Collector-emitter saturation voltage ⁽¹⁾

$I_C = 600\text{ mA}$; $I_B = 60\text{ mA}$

V_{CEsat} typ. 450 mV

Transition frequency at $f = 500\text{ MHz}$ ⁽²⁾

$-I_E = 300\text{ mA}$; $V_{CB} = 25\text{ V}$

f_T typ. 3,4 GHz

$-I_E = 600\text{ mA}$; $V_{CB} = 25\text{ V}$

f_T typ. 3,1 GHz

Collector capacitance at $f = 1\text{ MHz}$

$I_E = I_e = 0$; $V_{CB} = 25\text{ V}$

C_c typ. 6,6 pF

Feedback capacitance at $f = 1\text{ MHz}$

$I_C = 20\text{ mA}$; $V_{CE} = 25\text{ V}$

C_{re} typ. 3,5 pF

Collector-stud capacitance

C_{cs} typ. 1,2 pF

Notes

1. Measured under pulse conditions: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0,02$.
2. Measured under pulse conditions: $t_p \leq 50\text{ }\mu\text{s}$; $\delta \leq 0,01$.

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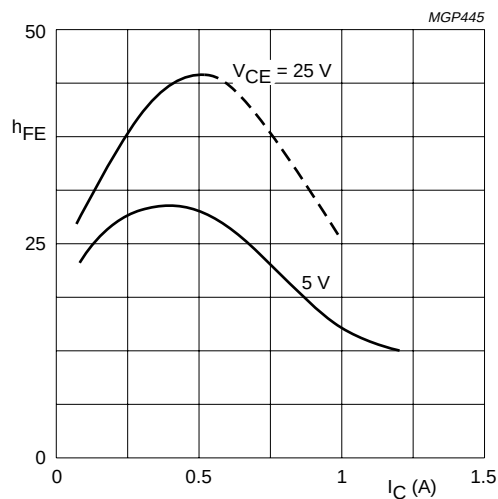


Fig.5 Typical values; $T_j = 25\text{ }^{\circ}\text{C}$.

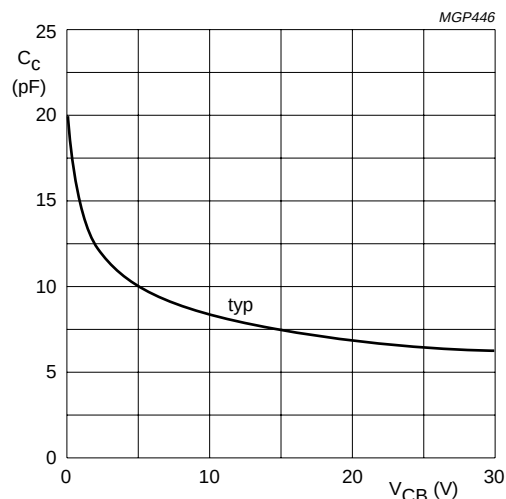


Fig.6 $I_E = I_e = 0$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$.

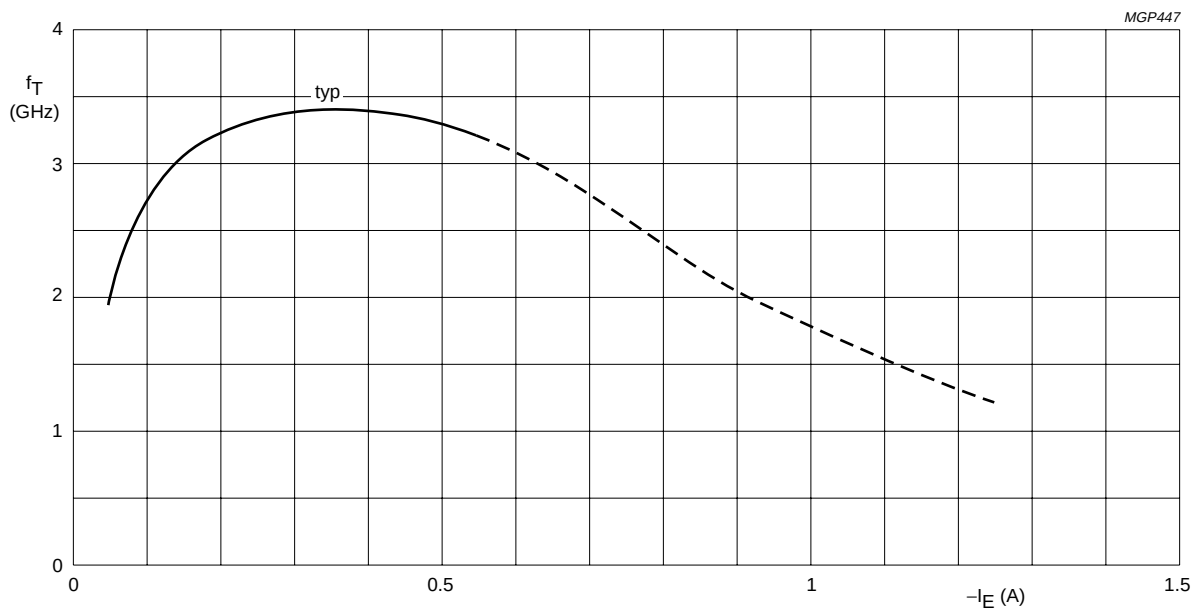


Fig.7 $V_{CB} = 25\text{ V}$; $f = 500\text{ MHz}$; $T_j = 25\text{ }^{\circ}\text{C}$.

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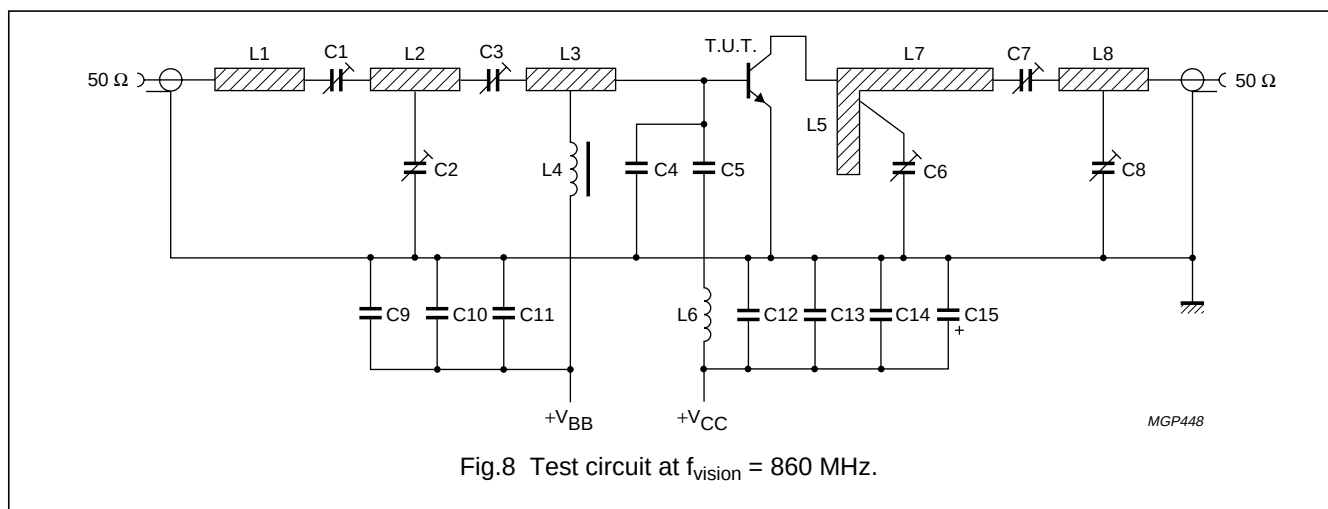
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APPLICATION INFORMATION

f_{vision} (MHz)	V_{CE} (V)	I_{C} (mA)	T_{h} (°C)	d_{im} (dB) ⁽¹⁾	$P_{\text{o sync}}$ (W) ⁽¹⁾	G_{p} (dB)
860	25	300	70	-60	> 1,0	> 10
860	25	300	70	-60	typ. 1,07	typ. 10,5
860	25	300	25	-60	typ. 1,15	typ. 10,5

Note

1. Three-tone test method (vision carrier -8 dB, sound carrier -7 dB, sideband signal -16 dB), zero dB corresponds to peak sync level.



List of components:

- C1 = C3 = 2 to 18 pF film dielectric trimmer (cat. no. 2222 809 05003)
- C2 = C6 = C8 = 1 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001) placed 24 mm, 8 mm and 46 mm respectively from transistor edge
- C4 = C5 = 4,3 pF multilayer ceramic chip capacitor (ATC 100A-4R3-C-PX-50)
- C7 = 1,8 to 10 pF film dielectric trimmer (cat. no. 2222 809 05002)
- C9 = C12 = 1 nF chip capacitor
- C10 = 100 nF polyester capacitor
- C11 = C13 = 470 nF polyester capacitor
- C14 = 10 nF polyester capacitor
- C15 = 3,3 μ F/40 F solid aluminium electrolytic capacitor
- L1 = stripline (5,2 mm $\times$ 4,5 mm)
- L2 = stripline (13,2 mm $\times$ 4,5 mm)
- L3 = stripline (15,0 mm $\times$ 4,5 mm)
- L4 = micro choke 0,47 μ H (cat. no. 4322 057 04770)
- L5 = stripline (see Fig.9 printed-circuit board layout)
- L6 = 4 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 5,5 mm; leads 2 $\times$ 4 mm
- L7 = stripline (37,0 mm $\times$ 4,5 mm)
- L8 = stripline (13,5 mm $\times$ 4,5 mm)

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L1; L2; L3; L5; L7 and L8 are striplines on a double Cu-clad printed-circuit board with PTFE fibre-glass dielectric ($\epsilon_r = 2,74$); thickness 1/16".

For bias circuit see Fig.10.

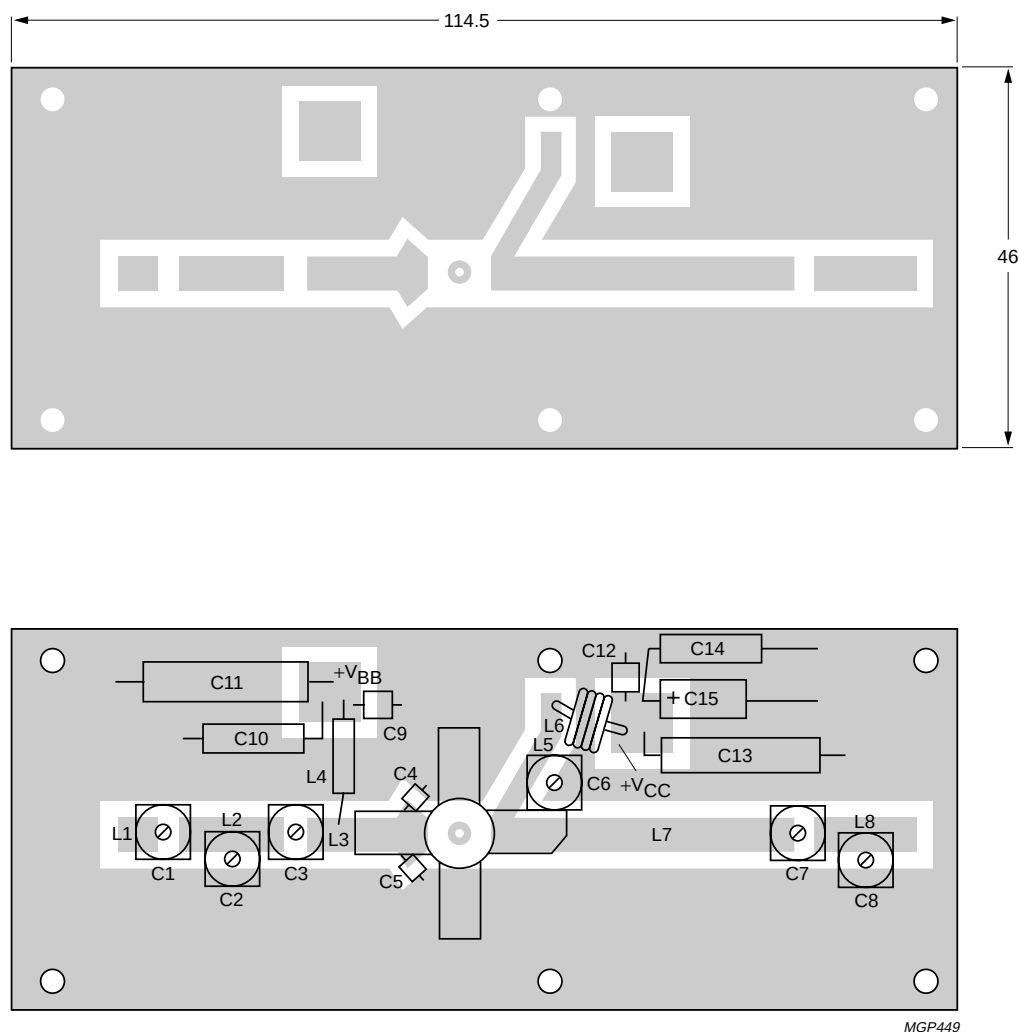


Fig.9 Component layout and printed-circuit board for 860 MHz test circuit.

The circuit and the components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets, whilst under the emitter leads Cu straps are used for a direct contact between upper and lower sheets.

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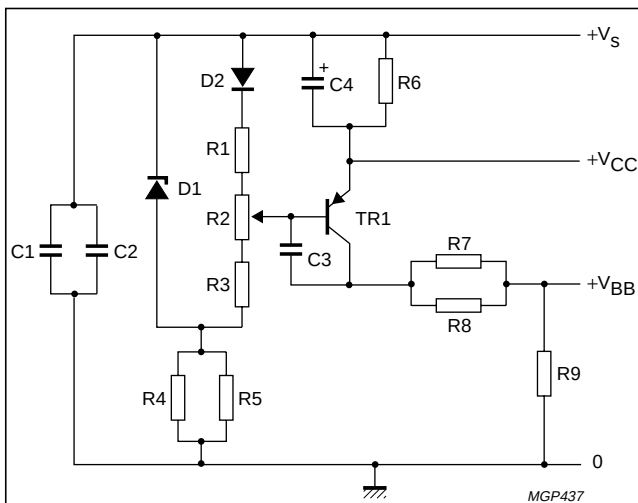


Fig.10 Bias circuit for class-A amplifier at $f_{\text{vision}} = 860 \text{ MHz}$.

List of components:

- C1 = 100 pF ceramic capacitor
- C2 = C3 = 100 nF polyester capacitor
- C4 = 10 $\mu\text{F}/25 \text{ V}$ solid aluminium electrolytic capacitor
- R1 = 150 Ω carbon resistor (0,25 W)
- R2 = 100 Ω preset potentiometer (0,1 W)
- R3 = 82 Ω carbon resistor (0,25 W)
- R4 = R5 = 2,2 k Ω carbon resistor (0,25 W)
- R6 = 6 Ω ; parallel connection of $2 \times 12 \Omega$ carbon resistors (0,5 W each)
- R7 = R8 = 820 Ω carbon resistor (0,25 W)
- R9 = 33 Ω carbon resistor (0,25 W)
- D1 = BZY88-C3V3
- D2 = BY206
- TR1 = BD136

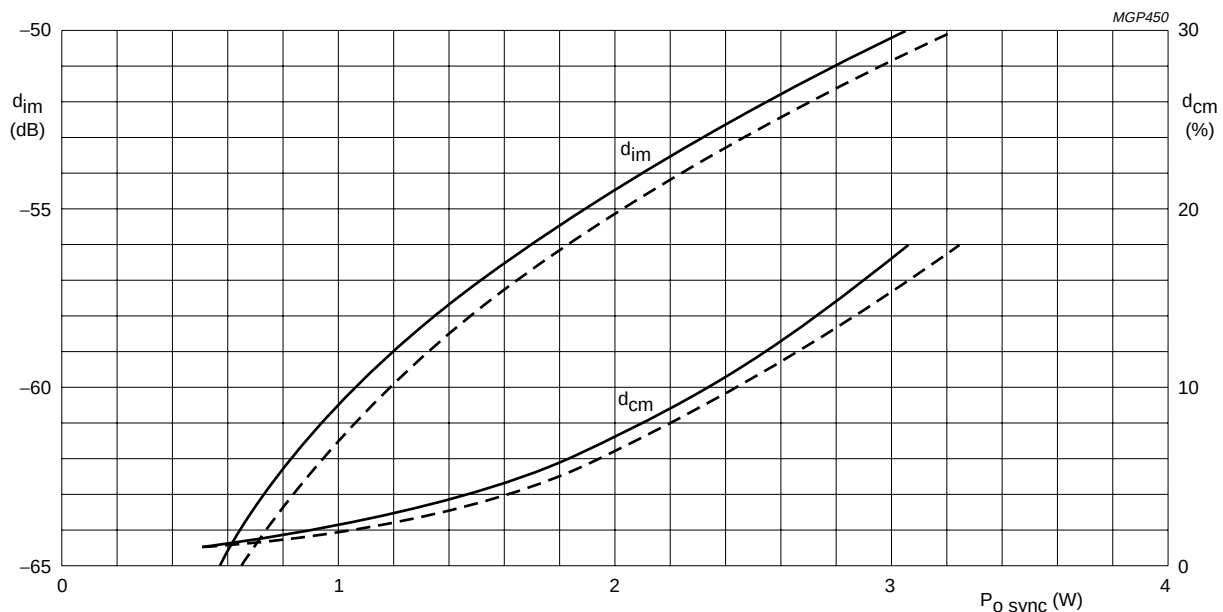


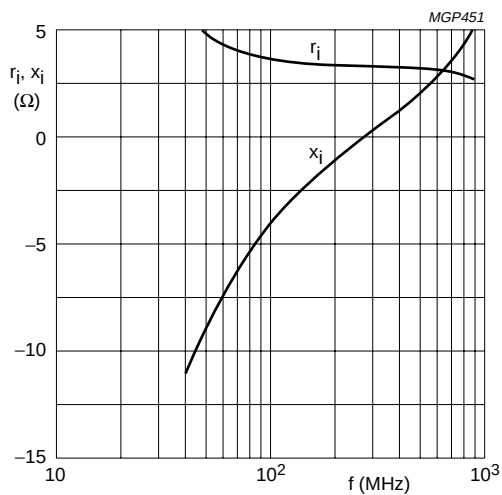
Fig.11 Intermodulation distortion ($d_{\text{im}}^{(1)}$) and cross-modulation distortion ($d_{\text{cm}}^{(2)}$) as a function of output power. Typical values; $V_{\text{CE}} = 25 \text{ V}$; $I_{\text{C}} = 300 \text{ mA}$; $f_{\text{vision}} = 860 \text{ MHz}$; --- $T_{\text{h}} = 25 \text{ }^{\circ}\text{C}$; — $T_{\text{h}} = 70 \text{ }^{\circ}\text{C}$.

Information for wideband application from 470 to 860 MHz available on request.

- Three-tone test method (vision carrier -8 dB , sound carrier -7 dB , sideband signal -16 dB), zero dB corresponds to peak sync level.
Intermodulation distortion of input signal $\leq -75 \text{ dB}$.
- Two-tone test method (vision carrier 0 dB , sound carrier -7 dB), zero dB corresponds to peak sync level.
Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to -20 dB .

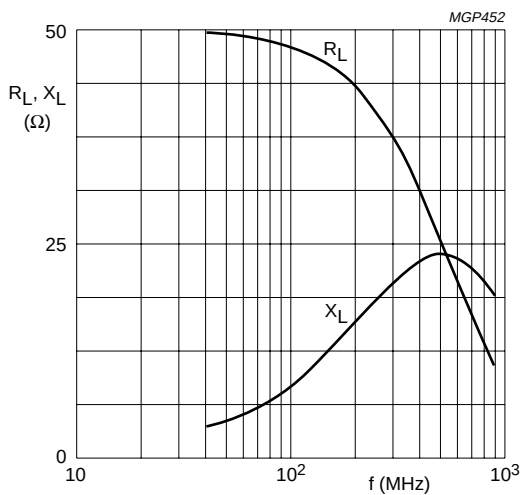
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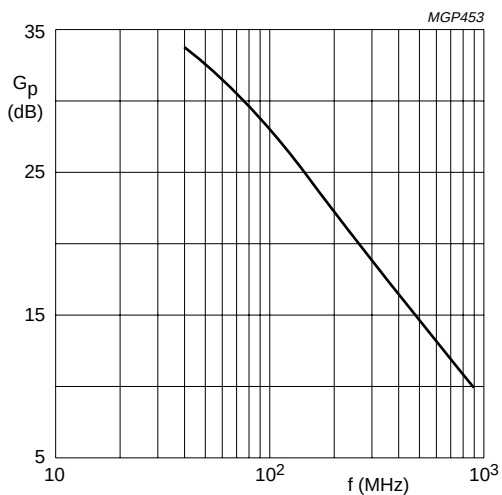
Typical values; $V_{CE} = 25\text{ V}$;
 $I_C = 300\text{ mA}$; $T_h = 70\text{ }^\circ\text{C}$.

Fig.12 Input impedance (series components).



Typical values; $V_{CE} = 25\text{ V}$;
 $I_C = 300\text{ mA}$; $T_h = 70\text{ }^\circ\text{C}$.

Fig.13 Load impedance (series components).



Typical values; $V_{CE} = 25\text{ V}$;
 $I_C = 300\text{ mA}$; $T_h = 70\text{ }^\circ\text{C}$.

Fig.14

Ruggedness

The BLW33 is capable of withstanding a load mismatch (VSWR = 50 through all phases) under the following conditions:

$f = 860\text{ MHz}$; $V_{CE} = 25\text{ V}$; $I_C = 300\text{ mA}$;
 $T_h = 70\text{ }^\circ\text{C}$ and $P_L = 2\text{ W}$.

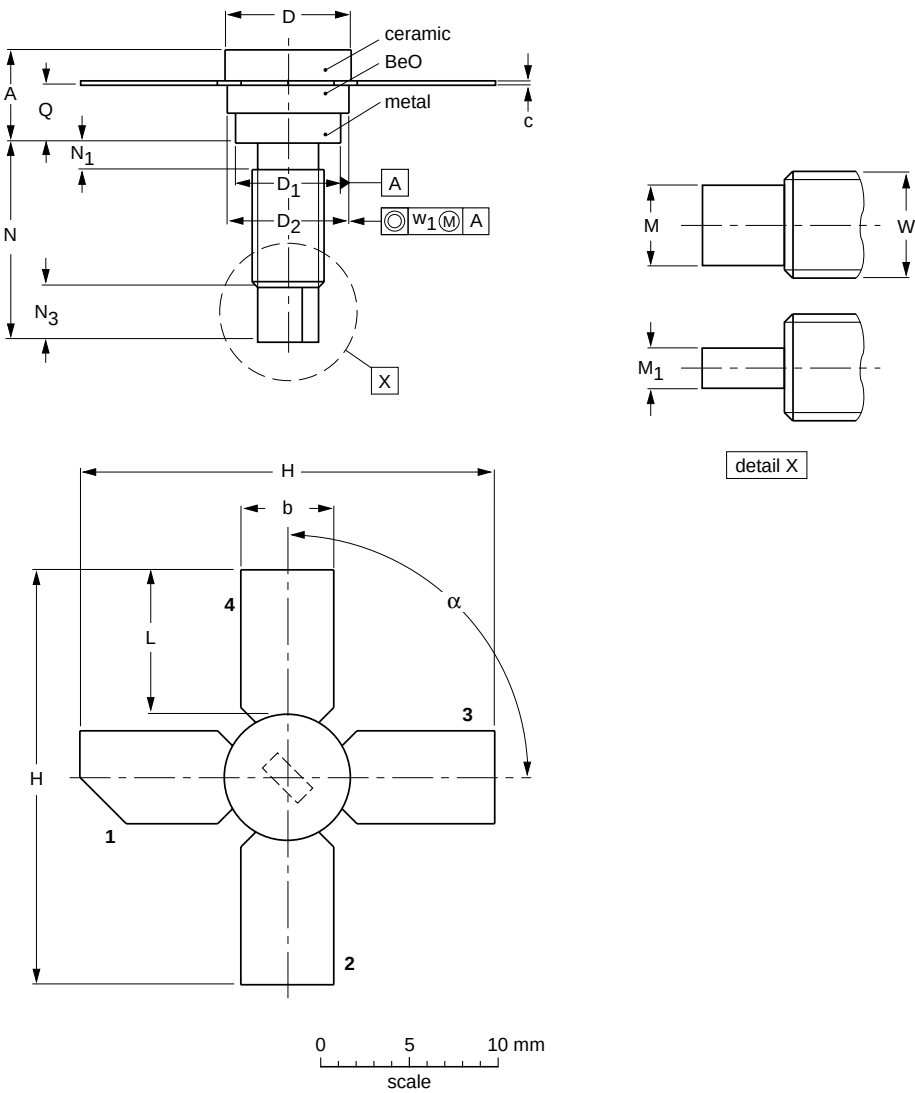
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PACKAGE OUTLINE

Studded ceramic package; 4 leads

SOT122A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	D ₂	H	L	M ₁	M	N	N ₁ max.	N ₃	Q	W	w ₁	α
mm	5.97 4.74	5.85 5.58	0.18 0.14	7.50 7.23	6.48 6.22	7.24 6.93	27.56 25.78	9.91 9.14	3.18 2.66	1.66 1.39	11.82 11.04	1.02	3.86 2.92	3.38 2.74	8-32 UNC	0.381	90°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT122A						97-04-18

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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