

**Triacs
sensitive gate**

BT134W series E

GENERAL DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope suitable for surface mounting, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

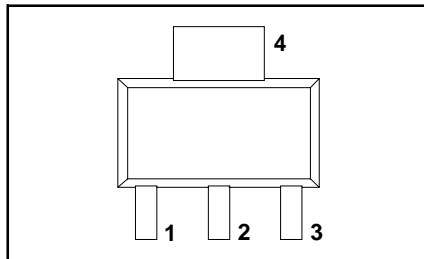
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.		UNIT
		500E	600E	
V_{DRM}	Repetitive peak off-state voltages	500	600	V
$I_{T(RMS)}$	RMS on-state current	1	1	A
I_{TSM}	Non-repetitive peak on-state current	10	10	A

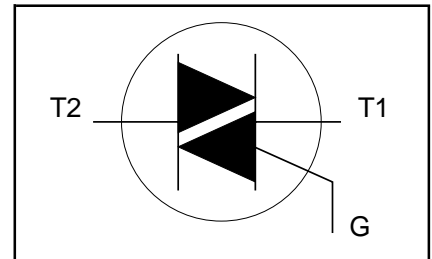
PINNING - SOT223

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-500 500 ¹	-600 600 ¹	
V_{DRM}	Repetitive peak off-state voltages		-	-500 500 ¹	-600 600 ¹	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 108^\circ\text{C}$	-	1		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25^\circ\text{C}$ prior to surge	-	10		A
		$t = 20\text{ ms}$	-	11		A
		$t = 16.7\text{ ms}$	-	0.5		A ² s
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-			
di_T/dt	Repetitive rate of rise of on-state current after triggering	$I_{TM} = 1.5\text{ A}; I_G = 0.2\text{ A}; di_G/dt = 0.2\text{ A}/\mu\text{s}$	-			
		T2+ G+	-	50		A/ μs
		T2+ G-	-	50		A/ μs
		T2- G-	-	50		A/ μs
		T2- G+	-	10		A/ μs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		$^\circ\text{C}$
T_j	Operating junction temperature		-	125		$^\circ\text{C}$

¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/ μs .

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point	full or half cycle	-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted; minimum footprint pcb mounted; pad area as in fig:14	-	156 70	-	K/W K/W

STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$ T2+ G+ T2+ G- T2- G- T2- G+	-	2.5 4.0 5.0 11	10 10 10 25	mA mA mA mA
I_L	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$ T2+ G+ T2+ G- T2- G- T2- G+	-	3.0 10 2.5 4.0	15 20 15 20	mA mA mA mA
I_H	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	2.2	15	mA
V_T	On-state voltage	$I_T = 2\text{ A}$	-	1.2	1.5	V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.7	1.5	V
I_D	Off-state leakage current	$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125\text{ °C}$ $V_D = V_{DRM(max)}; T_j = 125\text{ °C}$	0.25	0.4 0.1	- 0.5	V mA

DYNAMIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$ exponential waveform; gate open circuit	-	30	-	V/ μ s
t_{gt}	Gate controlled turn-on time	$I_{TM} = 1.5\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $di_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	μ s

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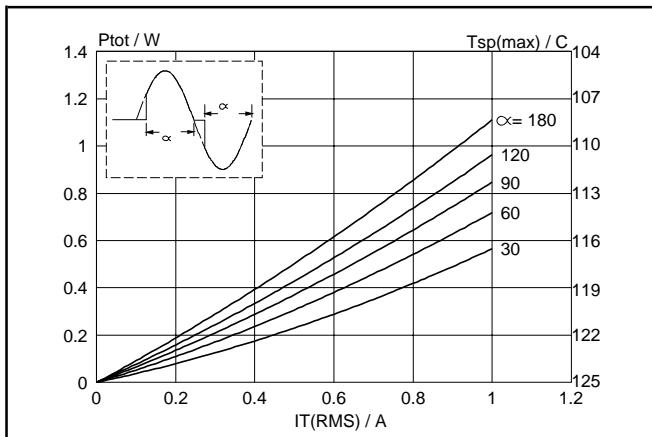


Fig.1. Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where $\alpha =$ conduction angle.

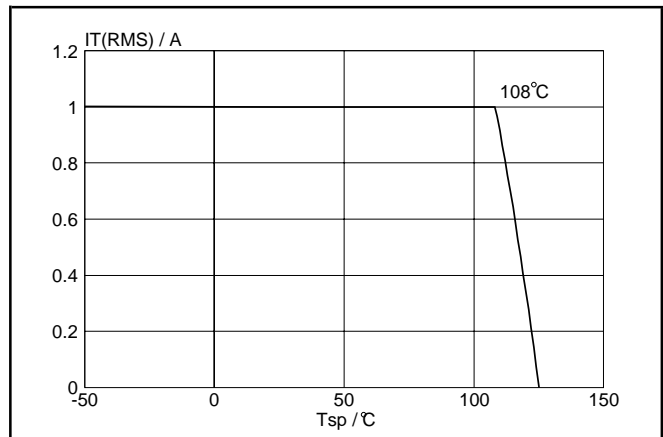


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus solder point temperature T_{sp} .

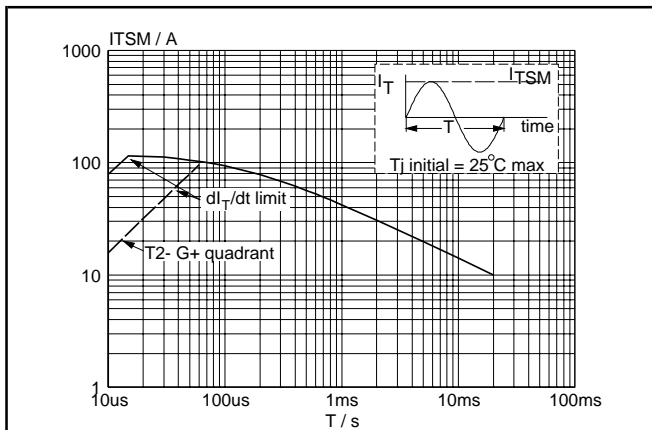


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \leq 20\text{ms}$.

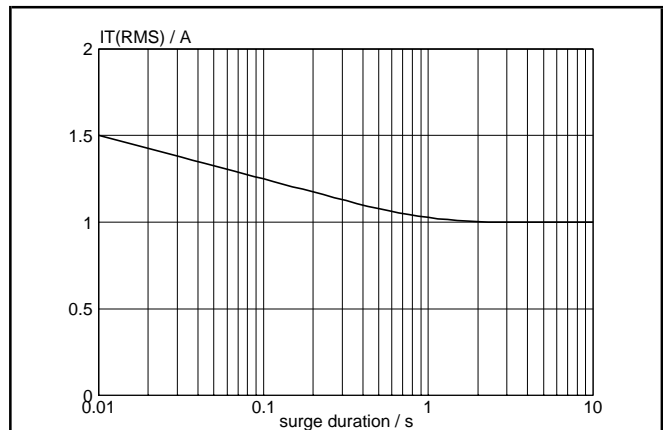


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f = 50\text{ Hz}$; $T_{sp} \leq 108^\circ\text{C}$.

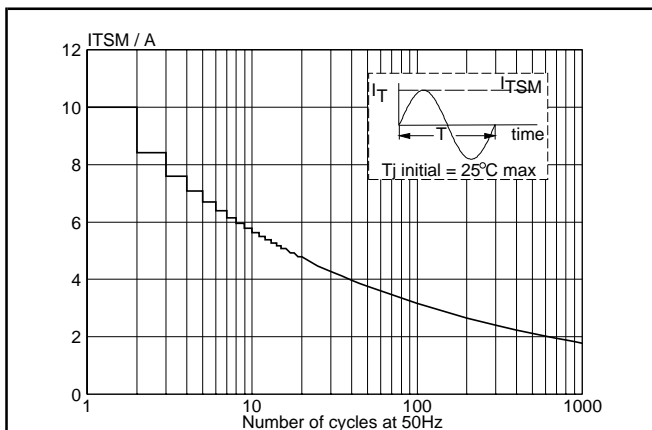


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f = 50\text{ Hz}$.

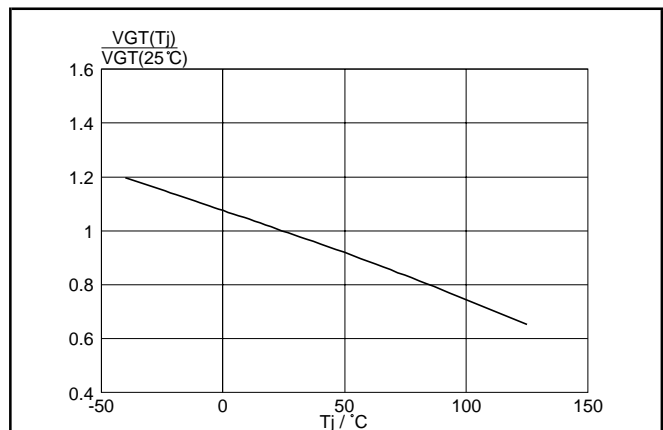
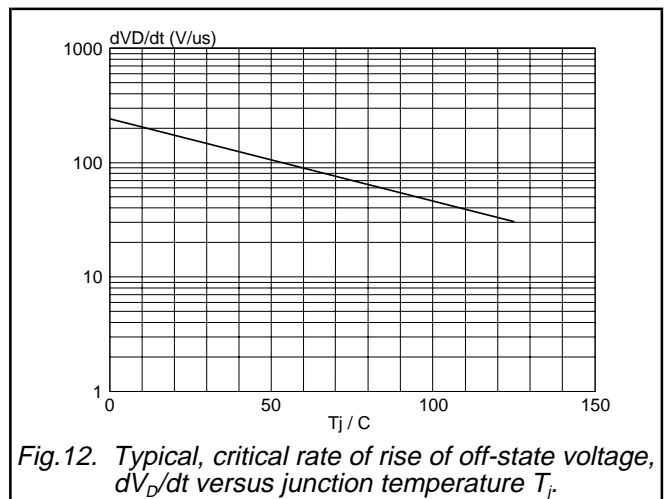
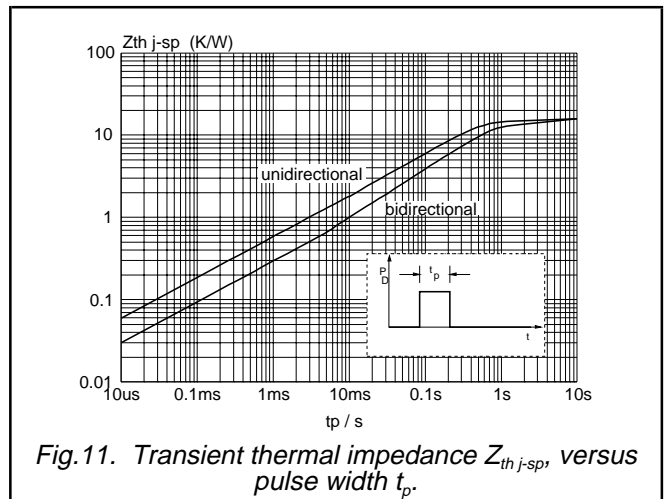
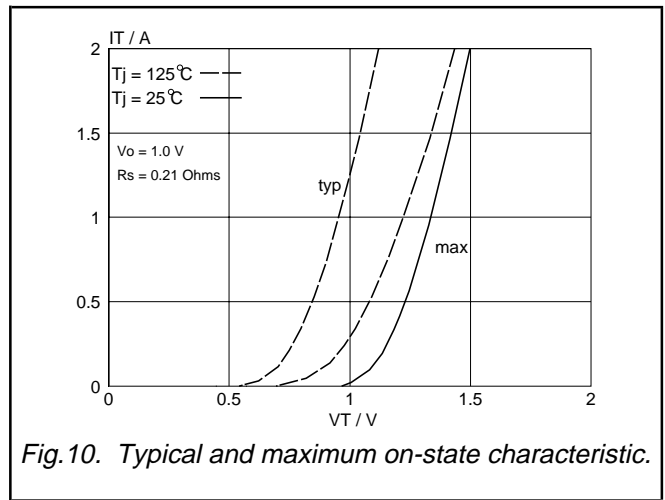
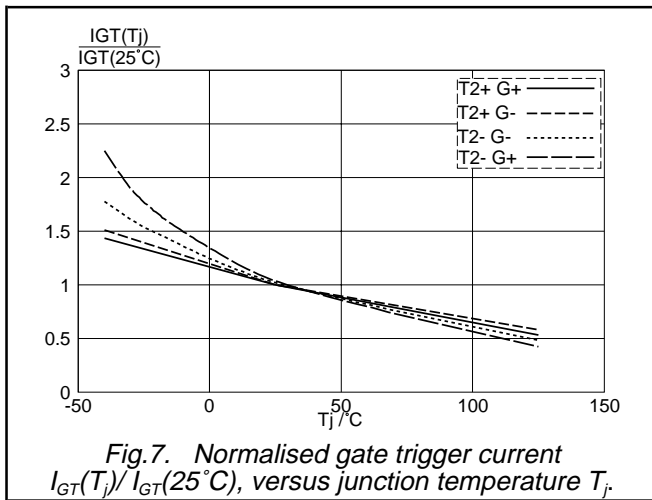


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

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MOUNTING INSTRUCTIONS

Dimensions in mm.

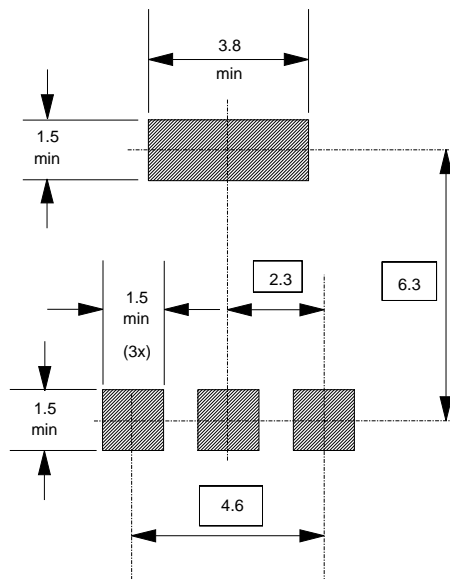
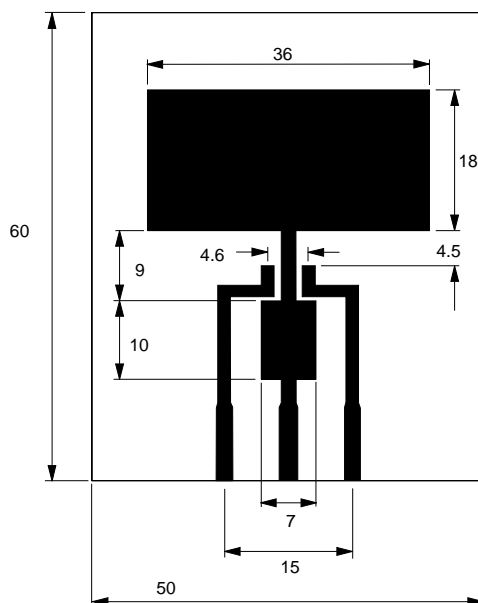


Fig.13. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

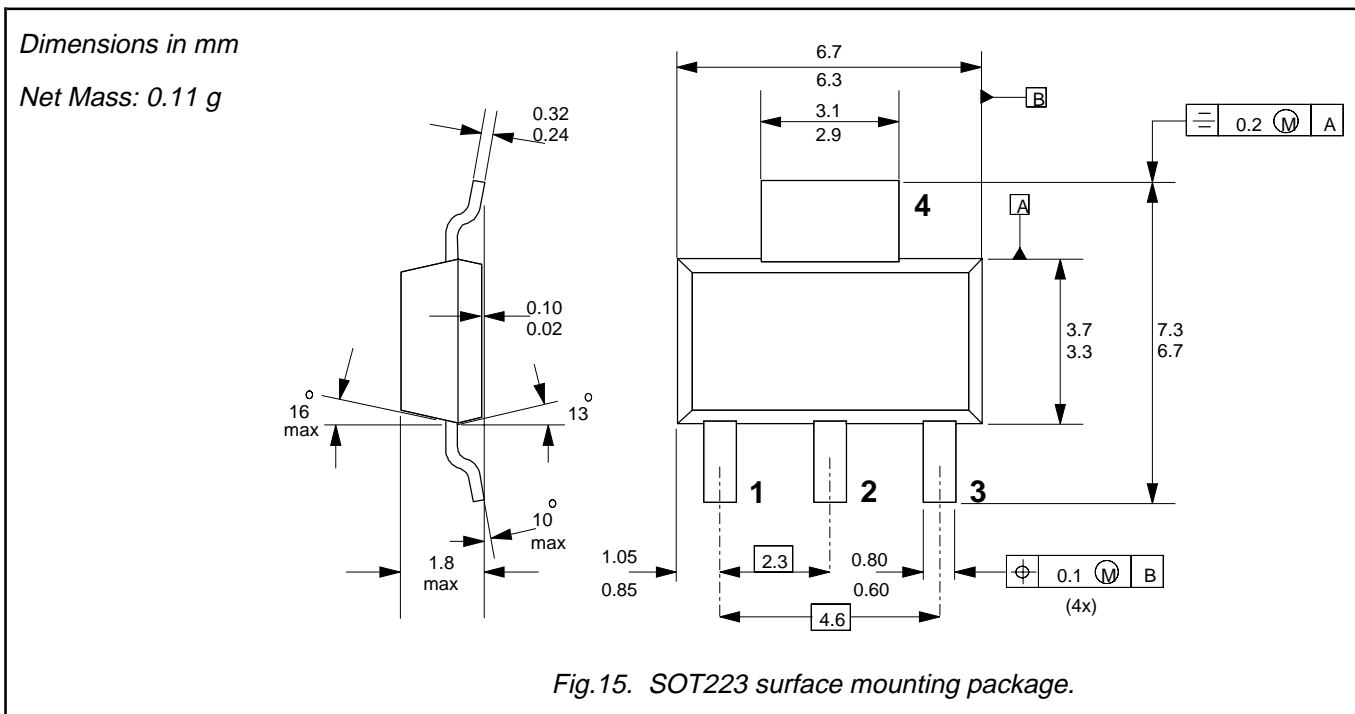


*Fig.14. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

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MECHANICAL DATA



Notes

1. For further information, refer to Philips publication SC18 " SMD Footprint Design and Soldering Guidelines".
Order code: 9397 750 00505.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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