

DATA SHEET

74ABT16952

74ABTH16952

16-bit registered transceiver (3-State)

Product specification
Supersedes data of 1995 Sep 28
IC23 Data Handbook

1998 Feb 25

16-bit registered transceiver (3-State)

74ABT16952
74ABTH16952

FEATURES

- Two 8-bit registered transceivers
- Live insertion/extraction permitted
- Power-up 3-State
- 74ABTH16952 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Independent registers for A and B buses
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs

DESCRIPTION

The 74ABT16952 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16952 is a dual octal registered transceiver. Two 8-bit registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock ($nCPXX$) provided that the Clock Enable ($nCEXX$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($nOEXX$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

Two options are available, 74ABT16952 which does not have the bus-hold feature and 74ABTH16952 which incorporates the bus-hold feature.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCPBA to nAx or nCPAB to nBx	$C_L = 50pF$; $V_{CC} = 5V$	2.8 2.3	ns
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	$V_O = 0V$ or V_{CC} ; 3-State	7	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5V$	500	μA
I_{CCL}		Outputs LOW; $V_{CC} = 5.5V$	8	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	$-40^{\circ}C$ to $+85^{\circ}C$	74ABT16952 DL	BT16952 DL	SOT371-1
56-Pin Plastic TSSOP Type II	$-40^{\circ}C$ to $+85^{\circ}C$	74ABT16952 DGG	BT16952 DGG	SOT364-1
56-Pin Plastic SSOP Type III	$-40^{\circ}C$ to $+85^{\circ}C$	74ABTH16952 DL	BH16952 DL	SOT371-1
56-Pin Plastic TSSOP Type II	$-40^{\circ}C$ to $+85^{\circ}C$	74ABTH16952 DGG	BH16952 DGG	SOT364-1

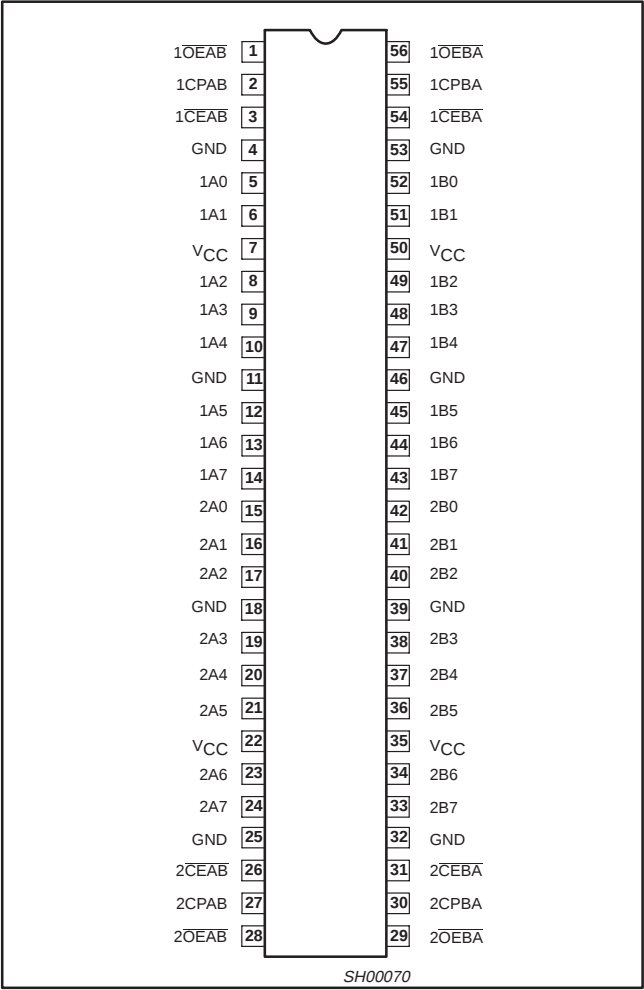
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55 18, 22	1CPAB / 1CPBA 2CPAB / 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1CEAB / 1CEBA 2CEAB / 2CEBA	Clock enable input A to B / Clock enable input B to A
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1A0 – 1A7 2A0 – 2A7	Data inputs/outputs (A side)
1, 56 8, 29	1B0 – 1B7 2B0 – 2B7	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 45, 53	1OEAB / 1OEBA 2OEAB / 2OEBA	Output enable inputs
4, 17, 30, 43	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

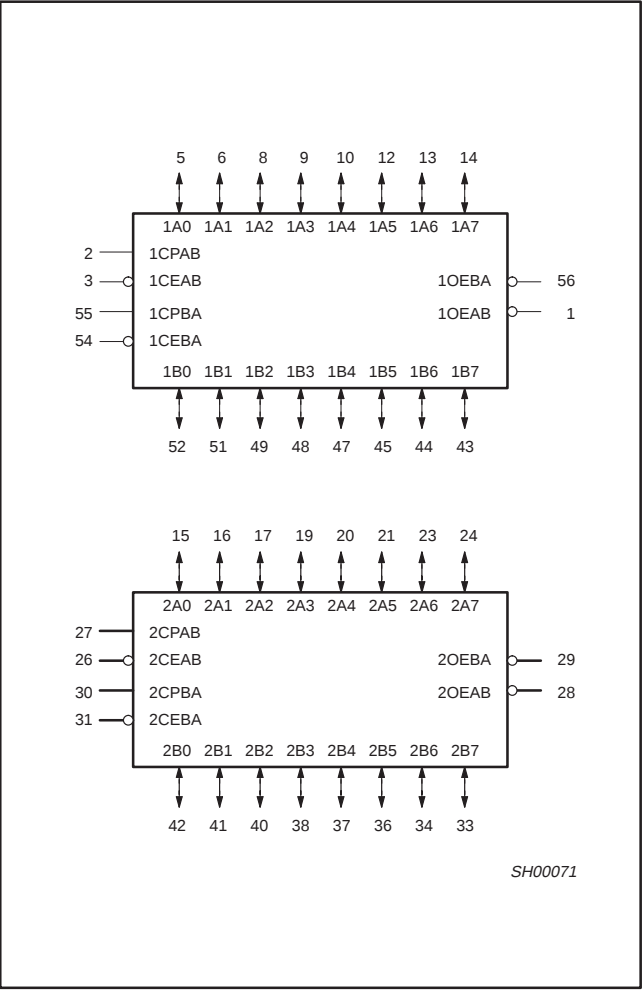
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PIN CONFIGURATION



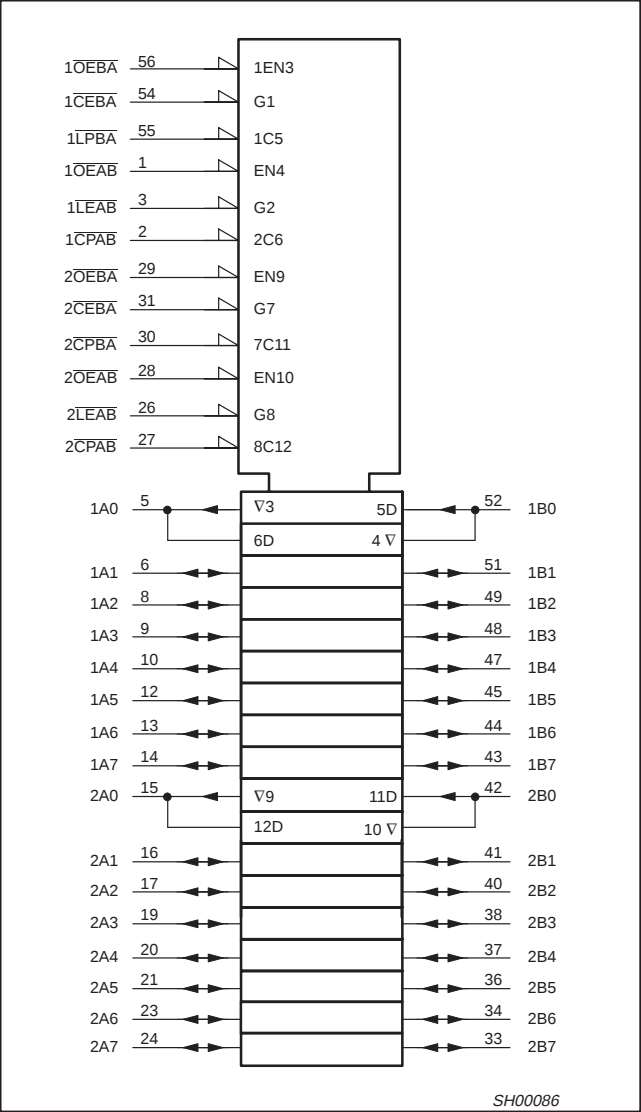
LOGIC SYMBOL



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LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL Q	OPERATING MODE
nAx or nBx	nCPXX	nCEXX		
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

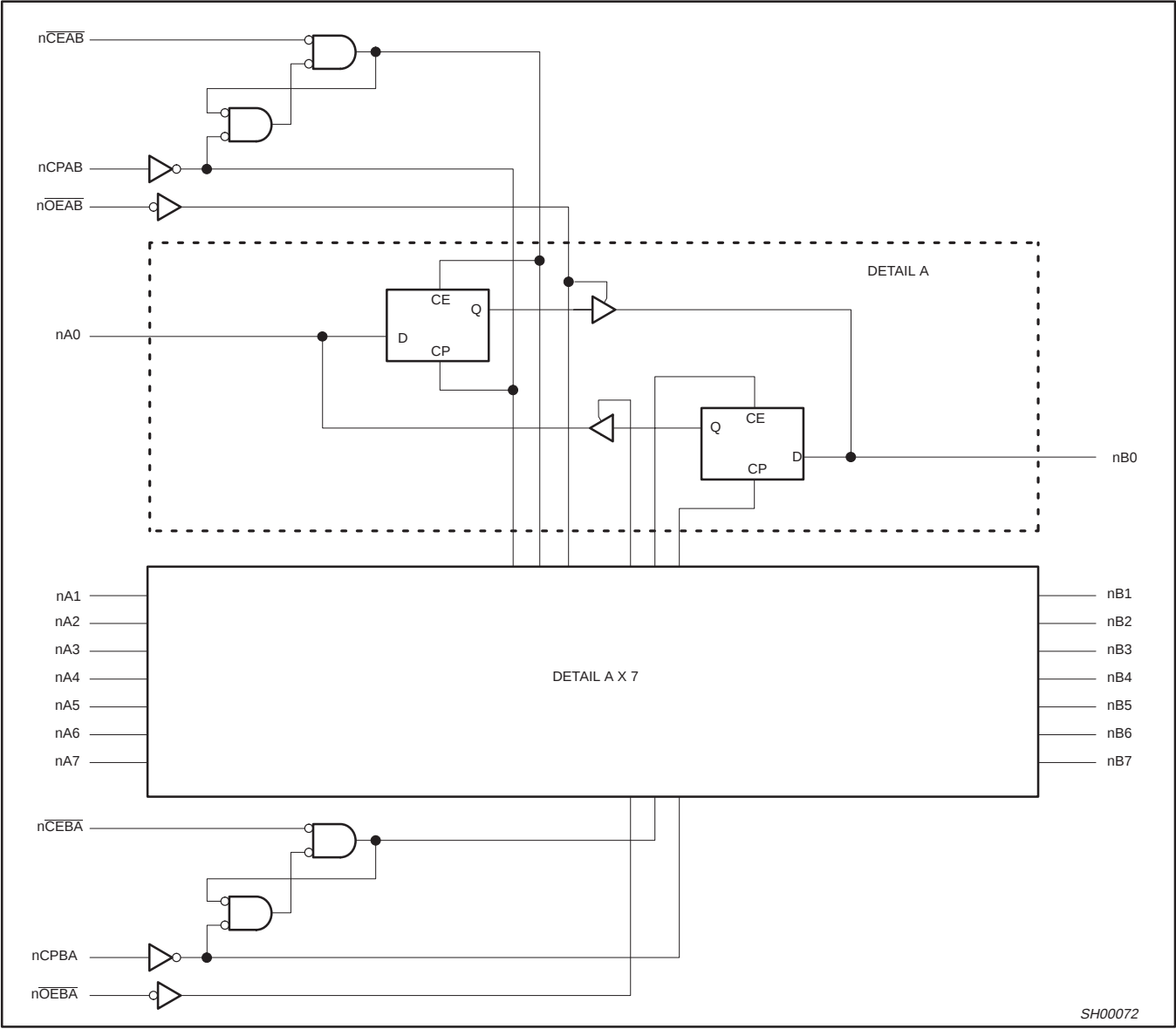
INPUTS		INTERNAL Q	nAx or nBx OUTPUTS	OPERATING MODE
nOEXX				
H	X	X	Z	Disable outputs
L L	L H	L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

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LOGIC DIAGRAM



16-bit registered transceiver (3-State)

74ABT16952
74ABTH16952ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	−18	mA
V_I	DC input voltage ³		−1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	−50	mA
V_{OUT}	DC output voltage ³	Output in Off or High state	−0.5 to +5.5	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	−64	
T_{stg}	Storage temperature range		−65 to 150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level Input voltage		0.8	V
I_{OH}	High-level output current		−32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	−40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T _{amb} = +25°C			T _{amb} = -40°C to +85°C		
				MIN	TYP	MAX	MIN	MAX	
V _{IK}	Input clamp voltage		V _{CC} = 4.5V; I _{IK} = -18mA		-0.9	-1.2		-1.2	V
V _{OH}	High-level output voltage		V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	2.5	2.9		2.5		V
			V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH}	3.0	3.4		3.0		V
			V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH}	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage		V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH}		0.42	0.55		0.55	V
V _{RST}	Power-up output low voltage ³		V _{CC} = 5.5V; I _{OL} = 1mA; V _I = GND or V _{CC}		0.13	0.55		0.55	V
I _I	Input leakage current	Control pins	V _{CC} = 5.5V; V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
I _{HOLD}	Bus Hold current A inputs ⁶ 74ABTH16952		V _{CC} = 4.5V, V _I = 0.8V	50			50		μA
			V _{CC} = 4.5V; V _I = 2.0V	-75			-75		
			V _{CC} = 5.5V; V _I = 0 to 5.5V	±500					
I _{OFF}	Power-off leakage current		V _{CC} = 0V; V _O or V _I ≤ 4.5V		±5.0	±100		±100	μA
I _{PU/PD}	Power-up/down 3-State output current ⁴		V _{CC} = 2.1V; V _O = 0.0V; V _I = GND or V _{CC} ; V _{OE} = Don't care		±5.0	±50		±50	μA
I _{IH} + I _{OZH}	3-State output High current		V _{CC} = 5.5V; V _O = 5.5V; V _I = V _{IL} or V _{IH}		5.0	50		50	μA
I _{IL} + I _{OZL}	3-State output Low current		V _{CC} = 5.5V; V _O = 0.0V; V _I = V _{IL} or V _{IH}		-5.0	-50		-50	μA
I _{CEX}	Output High leakage current		V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC}		5.0	50		50	μA
I _O	Output current ¹		V _{CC} = 5.5V; V _O = 2.5V	-50	-70	-180	-50	-180	mA
I _{CCH}	Quiescent supply current		V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC}		0.5	1.5		1.5	mA
I _{CCL}			V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC}		8	19		19	mA
I _{CCZ}			V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC}		0.5	1.5		1.5	mA
ΔI _{CC}	Additional supply current per input pin ² 74ABT16952		V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		5	100		100	μA
ΔI _{CC}	Additional supply current per input pin ² 74ABTH16952		V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND		100	500		500	μA

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.
- Unused pins at V_{CC} or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = −40°C to +85°C V _{CC} = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
f _{MAX}	Maximum clock frequency	1	150			150		MHz
t _{PLH} t _{PHL}	Propagation delay nCPBA to nAx, nCPAB to nBx	1	1.0 1.0	2.8 2.3	3.9 3.9	1.0 1.0	4.3 4.3	ns
t _{PZH} t _{PZL}	Output enable time nOEBA to nAx, nOEAB to nBx	3 4	1.0 1.0	2.5 2.2	3.8 3.8	1.0 1.0	4.6 4.6	ns
t _{PHZ} t _{PLZ}	Output disable time nOEBA to nAx, nOEAB to nBx	3 4	1.7 1.3	3.4 2.6	4.4 3.9	1.7 1.3	5.2 4.2	ns

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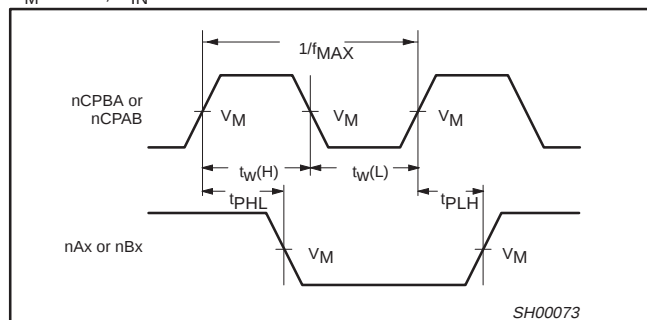
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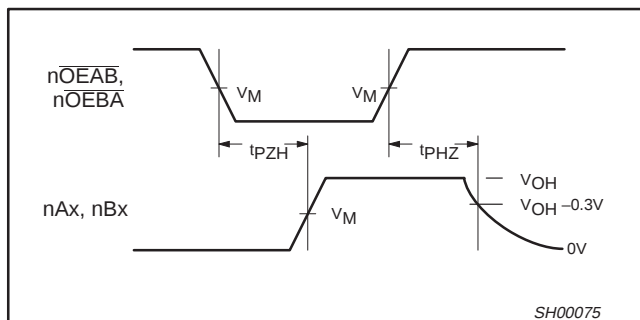
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time nAx to nCPAB or nBx to nCPBA	2	1.2 1.5	0.9 1.2	1.2 1.5	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time nAx to nCPAB or nBx to nCPBA	2	0.0 0.0	-1.2 -0.9	0.0 0.0	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time nCEAB to nCPAB, nCEBA to nCPBA	2	1.2 1.6	0.9 1.1	1.2 1.6	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time nCEAB to nCPAB, nCEBA to nCPBA	2	0.0 0.0	-1.1 -0.9	0.0 0.0	ns
$t_w(\text{H})$ $t_w(\text{L})$	nCPAB or nCPBA pulse width, High or Low	1	3.3 2.5	2.6 1.0	3.3 2.5	ns

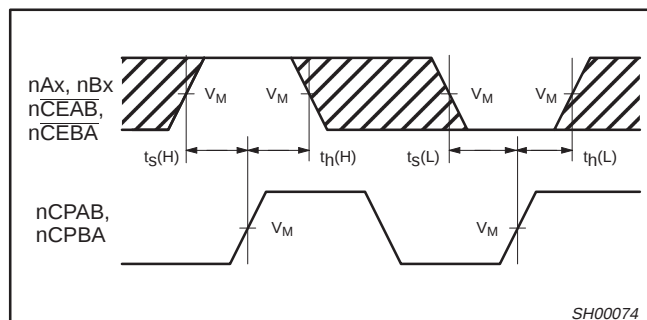
AC WAVEFORMS

 $V_M = 1.5\text{V}$, $V_{IN} = \text{GND to } 3.0\text{V}$ 

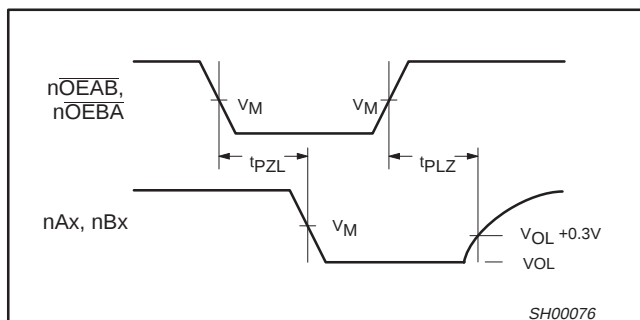
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Data Setup and Hold Times

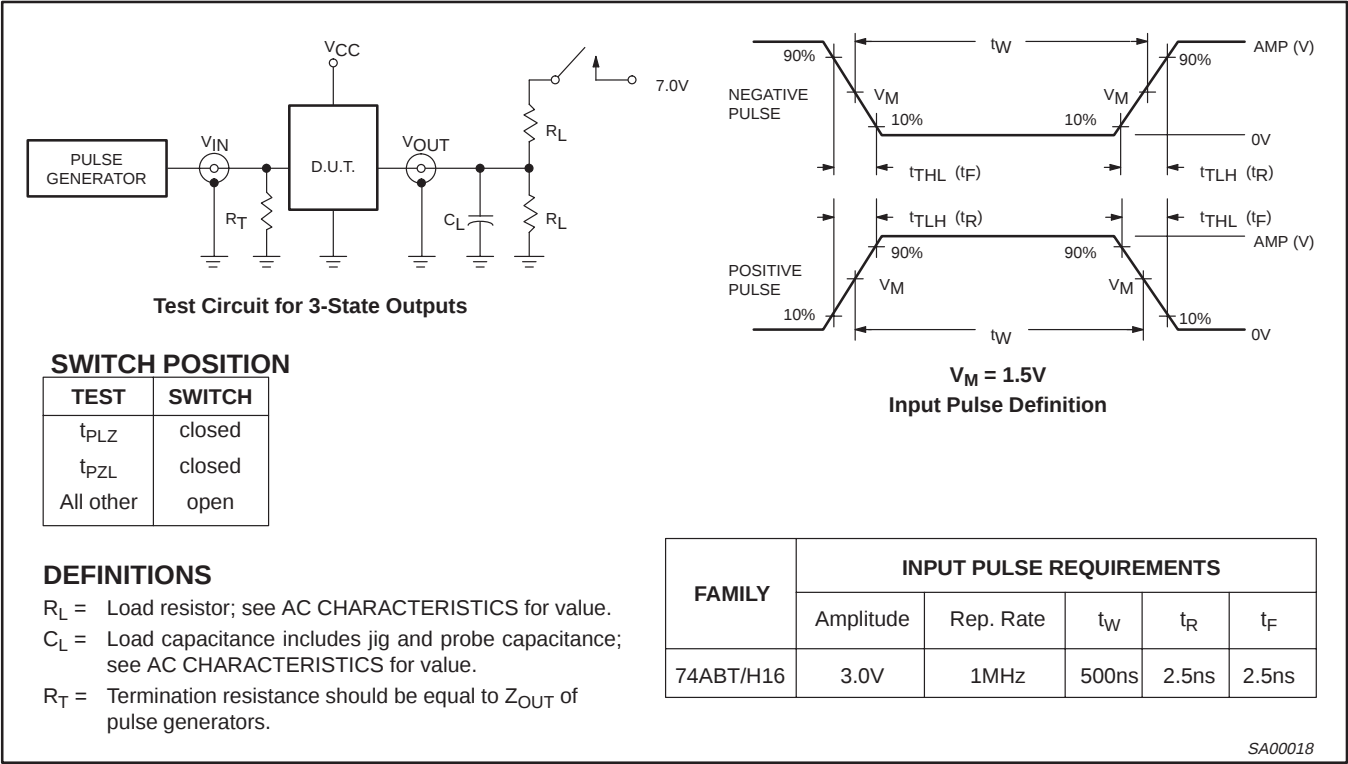


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORMS

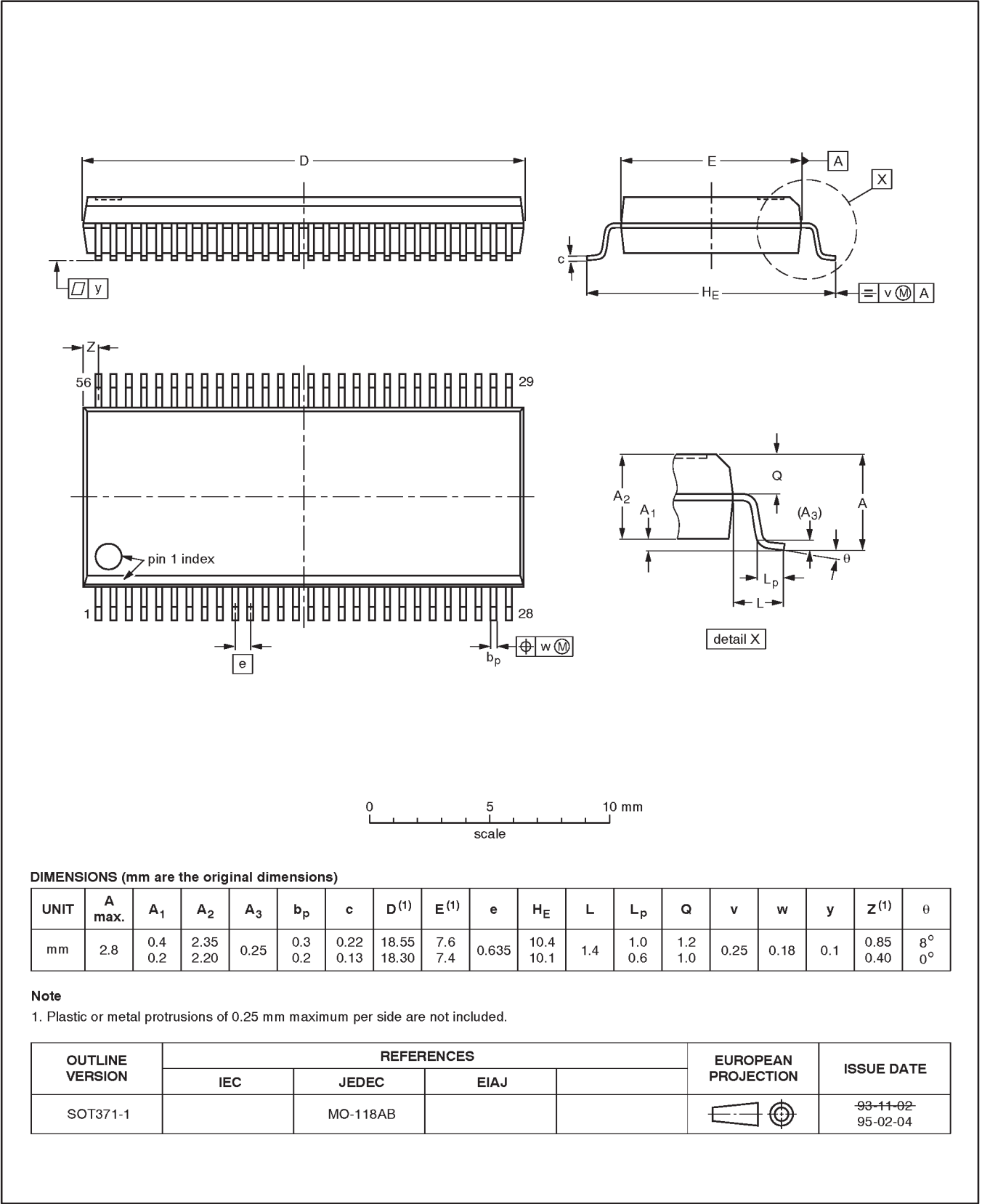


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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

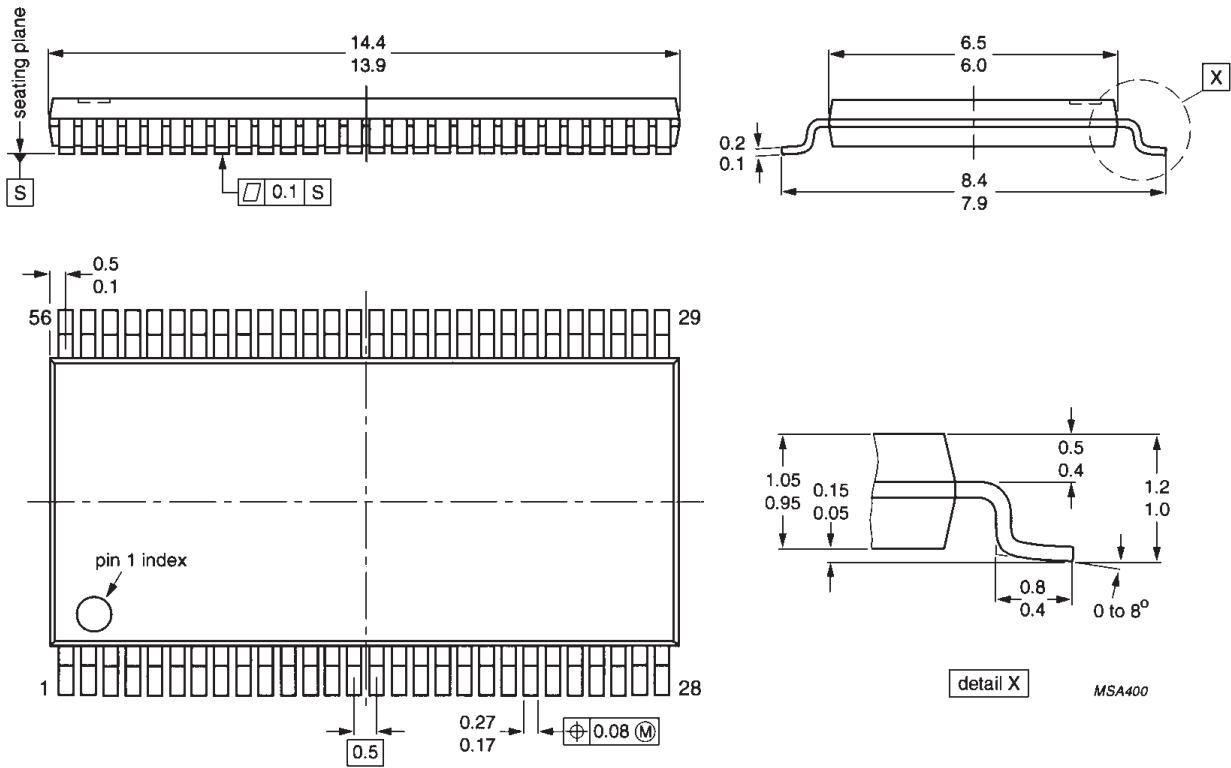


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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



Dimensions in mm.

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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