# DATA SHEET

# BUK107-50DL
PowerMOS transistor
Logic level TOPFET

Product specification
Supersedes data of September 1994
File under Discrete Semiconductors, SC13a

March 1997

Philips
Semiconductors

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# PowerMOS transistor
# Logic level TOPFET

# BUK107-50DL

## DESCRIPTION

Monolithic overload protected logic level power MOSFET in a surface mount plastic envelope, intended as a general purpose switch for automotive systems and other applications.

## APPLICATIONS

General controller for driving
- lamps
- small motors
- solenoids

## FEATURES

- Vertical power DMOS output stage
- Overload protected up to 85˚C ambient
- Overload protection by current limiting and overtemperature sensing
- Latched overload protection reset by input
- 5 V logic compatible input level
- Control of power MOSFET and supply of overload protection circuits derived from input
- Low operating input current permits direct drive by micro-controller
- ESD protection on all pins
- Overvoltage clamping for turn off of inductive loads

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MAX. | UNIT |
|---|---|---|---|
| $V_{DS}$ | Continuous drain source voltage | 50 | V |
| $I_D$ | Continuous drain current | 0.7 | A |
| $P_D$ | Total power dissipation | 1.8 | W |
| $T_j$ | Continuous junction temperature | 150 | ˚C |
| $R_{DS(ON)}$ | Drain-source on-state resistance | 200 | mΩ |

## FUNCTIONAL BLOCK DIAGRAM

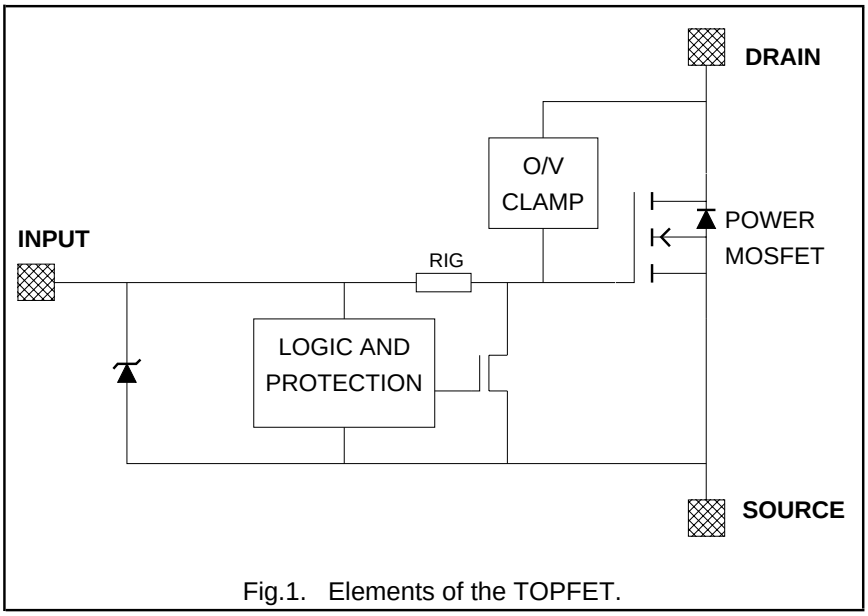
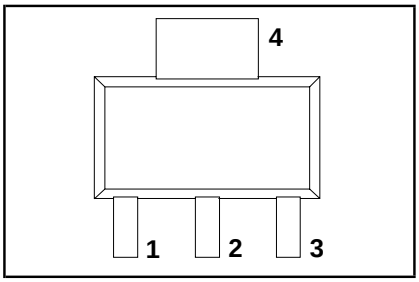



Fig.1. Elements of the TOPFET.

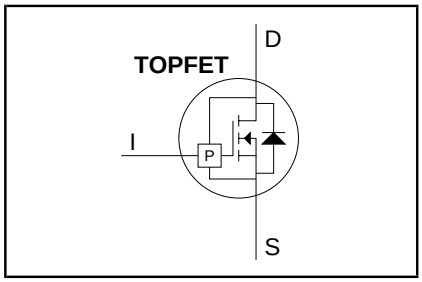
## PINNING - SOT223

| PIN | DESCRIPTION |
|---|---|
| 1 | input |
| 2 | drain |
| 3 | source |
| 4 | drain (tab) |

## PIN CONFIGURATION




## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DS}$ | Continuous drain source voltage[1] | - | - | 50 | V |
| $I_D$ | Continuous drain current[2] | - | - | self limiting | A |
| $I_I$ | Continuous input current | clamping | - | 3 | mA |
| $I_{IRM}$ | Non-repetitive peak input current | $t_p \leq 1$ ms | - | 10 | mA |
| $P_D$ | Total power dissipation | $T_{amb} = 25$ ˚C | - | 1.8 | W |
| $T_{stg}$ | Storage temperature | - | -55 | 150 | ˚C |
| $T_j$ | Continuous junction temperature | normal operation[3] | - | 150 | ˚C |

## ESD LIMITING VALUE

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_C$ | Electrostatic discharge capacitor voltage | Human body model; C = 250 pF; R = 1.5 kΩ | - | 2 | kV |

## OVERVOLTAGE CLAMPING LIMITING VALUES

At a drain source voltage above 50 V the power MOSFET is actively turned on to clamp overvoltage transients.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $E_{DSM}$ | Non-repetitive clamping energy | $T_b \leq 25$ ˚C; $I_{DM} < I_{D(lim)}$; inductive load | - | 100 | mJ |
| $E_{DRM}$ | Repetitive clamping energy | $T_b \leq 75$ ˚C; $I_{DM} = 50$ mA; f = 250 Hz | - | 4 | mJ |

## OVERLOAD PROTECTION LIMITING VALUES

With the protection supply provided via the input pin, TOPFET can protect itself from short circuit loads.
Overload protection operates by means of drain current limiting and activating the overtemperature protection.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DDP}$ | Protected drain source supply voltage | $V_{IS} = 5$ V | - | 35 | V |
| | | $V_{IS} = 4$ V | - | 16 | V |

## OVERLOAD PROTECTION CHARACTERISTICS

TOPFET switches off to protect itself when there is an overload fault condition.
It remains latched off until reset by the input.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| | **Overload protection** | | | | | |
| $I_{D(lim)}$ | Drain current limiting | $V_{IS} = 5$ V | 0.7 | 1.1 | 1.5 | A |
| | **Overtemperature protection** | only in drain current limiting | | | | |
| $T_{j(TO)}$ | Threshold junction temperature | $V_{IS} = 5$ V | 100 | 130 | 160 | ˚C |

**1** Prior to the onset of overvoltage clamping. For voltages above this value, safe operation is limited by the overvoltage clamping energy.

**2** Refer to OVERLOAD PROTECTION CHARACTERISTICS.

**3 Not** in an overload condition with drain current limiting.

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| | **Thermal resistance** | | | | | |
| $R_{th\ j\text{-}sp}$ | Junction to solder point | | - | 12 | 18 | K/W |
| $R_{th\ j\text{-}b}$ | Junction to board[1] | Mounted on any PCB | - | 40 | - | K/W |
| $R_{th\ j\text{-}a}$ | Junction to ambient | Mounted on PCB of fig. 19 | - | - | 70 | K/W |

## STATIC CHARACTERISTICS

$T_b$ = 25 ˚C unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{(CL)DSS}$ | Drain-source clamping voltage | $V_{IS}$ = 0 V; $I_D$ = 10 mA | 50 | 55 | - | V |
| $V_{(CL)DSS}$ | Drain-source clamping voltage | $V_{IS}$ = 0 V; $I_{DM}$ = 200 mA; $t_p \le 300\ \mu s$; $\delta \le 0.01$ | - | 56 | 70 | V |
| $I_{DSS}$ | Off-state drain current | $V_{DS}$ = 45 V; $V_{IS}$ = 0 V | - | 0.5 | 2 | µA |
| $I_{DSS}$ | Off-state drain current | $V_{DS}$ = 50 V; $V_{IS}$ = 0 V | - | 1 | 20 | µA |
| $I_{DSS}$ | Off-state drain current | $V_{DS}$ = 40 V; $V_{IS}$ = 0 V; $T_j$ = 100 ˚C | - | 10 | 100 | µA |
| $R_{DS(ON)}$ | Drain-source on-state resistance[2] | $V_{IS}$ = 5 V; $I_{DM}$ = 100 mA; $t_p \le 300\ \mu s$; $\delta \le 0.01$ | - | 150 | 200 | mΩ |

## INPUT CHARACTERISTICS

$T_b$ = 25 ˚C unless otherwise specified. The supply for the logic and overload protection is taken from the input.

| SYMBOL | PARAMETER | CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IS(TO)}$ | Input threshold voltage | $V_{DS}$ = 5 V; $I_D$ = 1 mA | | 1.7 | 2.2 | 2.7 | V |
| $I_{IS}$ | Input supply current | normal operation; | $V_{IS}$ = 5 V | - | 330 | 450 | µA |
| | | | $V_{IS}$ = 4 V | - | 170 | 270 | µA |
| $I_{ISL}$ | Input supply current | protection latched; | $V_{IS}$ = 5 V | - | 500 | 650 | µA |
| | | | $V_{IS}$ = 3.5 V | - | 250 | 400 | µA |
| $V_{ISR}$ | Protection latch reset voltage[3] | | | 1 | 2.2 | 3.5 | V |
| $V_{(CL)IS}$ | Input clamping voltage | $I_I$ = 1.5 mA | | 6 | 7.5 | - | V |
| $R_{IG}$ | Input series resistance | to gate of power MOSFET | | - | 33 | - | kΩ |

## SWITCHING CHARACTERISTICS

$T_{amb}$ = 25 ˚C; resistive load $R_L$ = 50 Ω; adjust $V_{DD}$ to obtain $I_D$ = 250 mA; refer to test circuit and waveforms

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $t_{d\ on}$ | Turn-on delay time | $V_{IS}$ = 0 V to $V_{IS}$ = 5 V | - | 8 | - | µs |
| $t_r$ | Rise time | | - | 30 | - | µs |
| $t_{d\ off}$ | Turn-off delay time | $V_{IS}$ = 5 V to $V_{IS}$ = 0 V | - | 3 | - | µs |
| $t_f$ | Fall time | | - | 6 | - | µs |

**1** Temperature measured 1.3 mm from tab.

**2** Continuous input voltage. The specified pulse width is for the drain current.

**3** The input voltage below which the overload protection circuits will be reset.

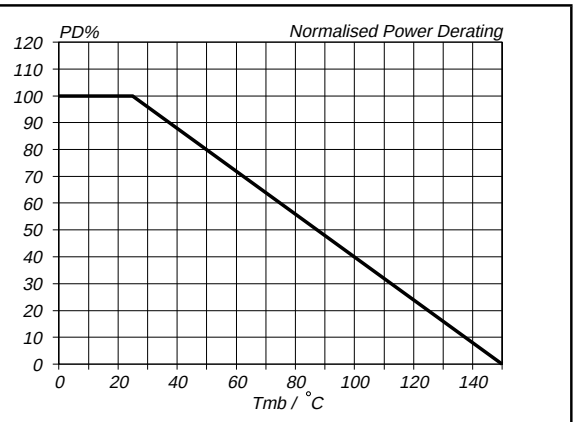



*Fig.2. Normalised limiting power dissipation. $P_D\% = 100 \cdot P_D/P_D(25\ ^\circ C) = f(T_{mb})$*

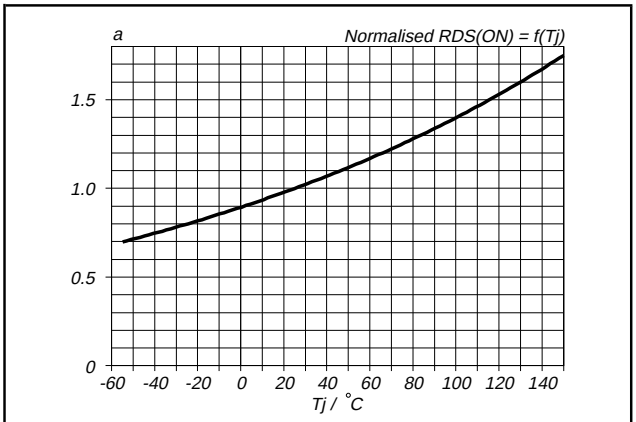



*Fig.5. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)}25\ ^\circ C = f(T_j)$; $I_D$ = 100 mA; $V_{IS}$ = 5 V*

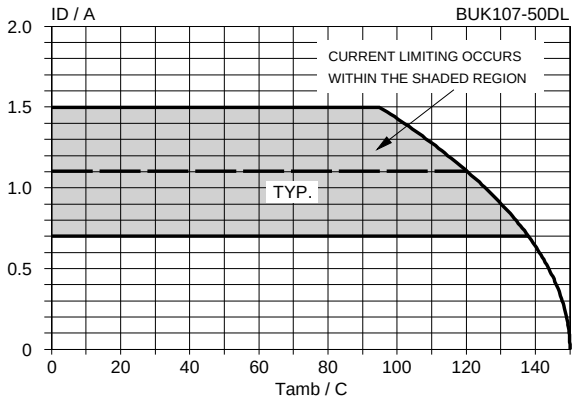



*Fig.3. Continuous drain current. $I_D = f(T_{amb})$; condition: $V_{IS}$ = 5 V*

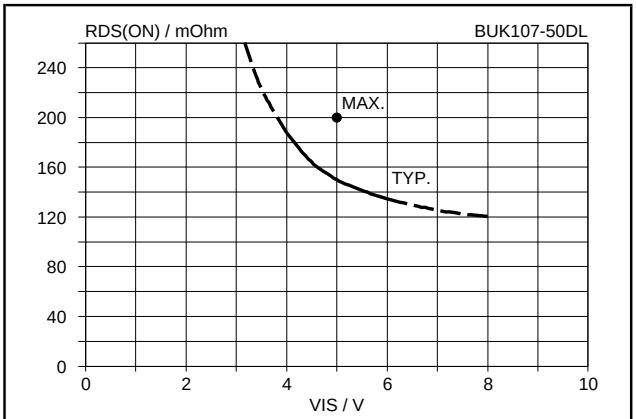



*Fig.6. Typical on-state resistance, $T_j$ = 25 ˚C. $R_{DS(ON)} = f(V_{IS})$; conditions: $I_D$ = 100 mA, $t_p$ = 300 µs*

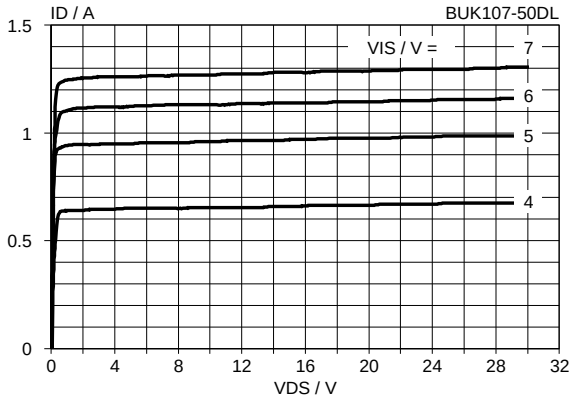



*Fig.4. Typical on-state characteristics, $T_j$ = 25 ˚C. $I_D = f(V_{DS})$; parameter $V_{IS}$; $t_p$ = 300 µs*

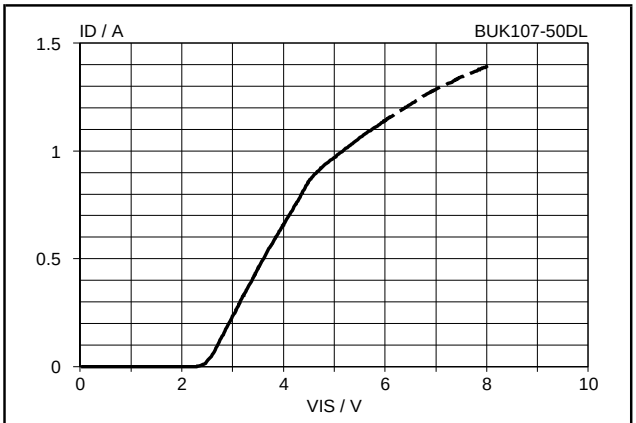



*Fig.7. Typical transfer characteristics, $T_j$ = 25 ˚C. $I_D = f(V_{IS})$; conditions: $V_{DS}$ = 10 V, $t_p$ = 300 µs*

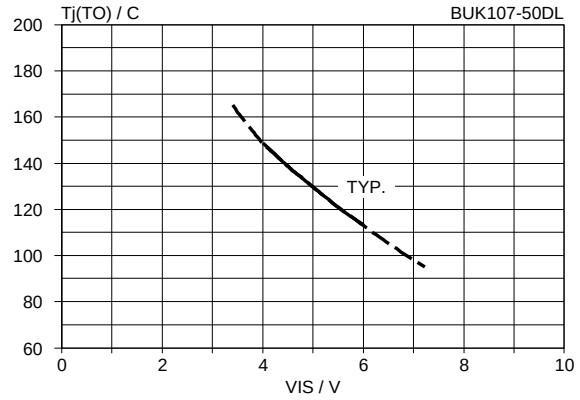



*Fig.8. Typical overtemperature protection threshold. $T_{j(TO)} = f(V_{IS})$; condition: $V_{DS}$ = 10 V*

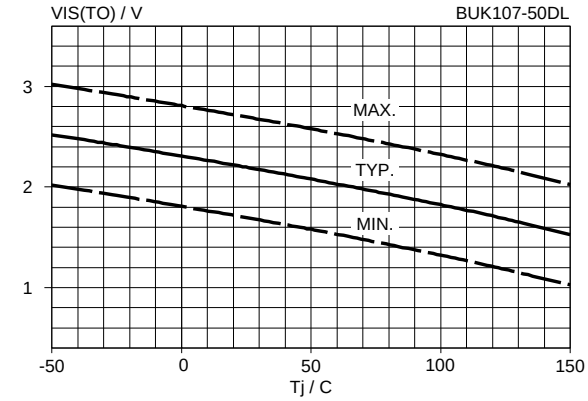



*Fig.11. Input threshold voltage. $V_{IS(TO)} = f(T_j)$; conditions: $I_D$ = 1 mA; $V_{DS}$ = 5 V*

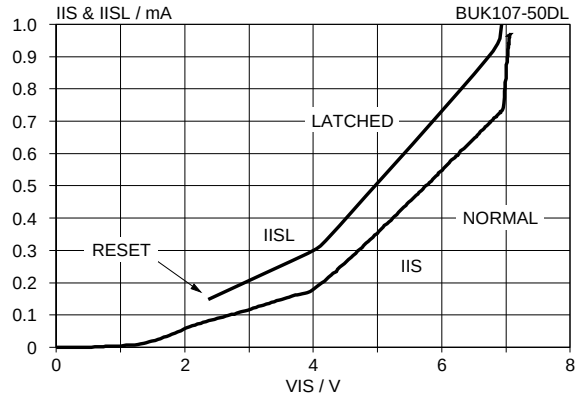



*Fig.9. Typical DC input characteristics, $T_j$ = 25 ˚C. $I_{IS}$ & $I_{ISL} = f(V_{IS})$; normal operation & protection latched*

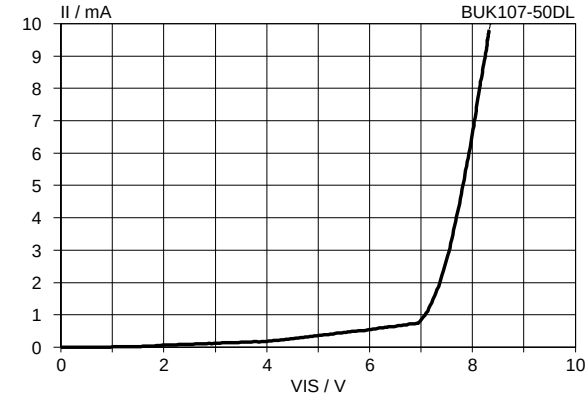



*Fig.12. Typical input clamping characteristic. $I_I = f(V_{IS})$; normal operation, $T_j$ = 25 ˚C.*

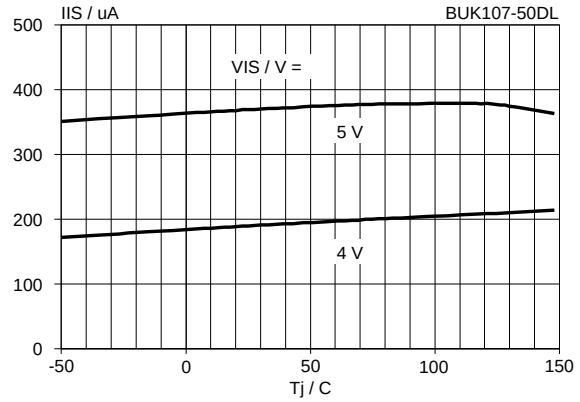



*Fig.10. Typical DC input current. $I_{IS} = f(T_j)$; parameter $V_{IS}$; normal operation*

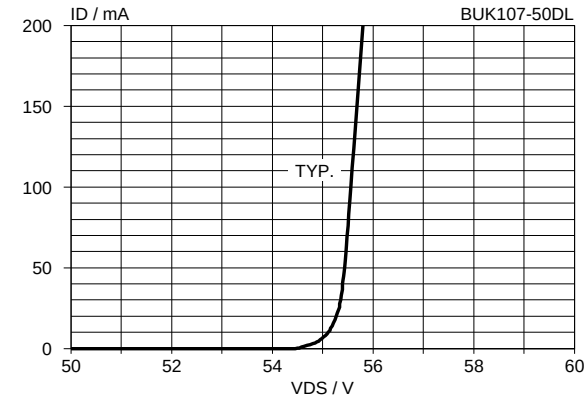



*Fig.13. Overvoltage clamping characteristic, 25 ˚C. $I_D = f(V_{DS})$; conditions: $V_{IS}$ = 0 V; $t_p \leq 300$ µs*

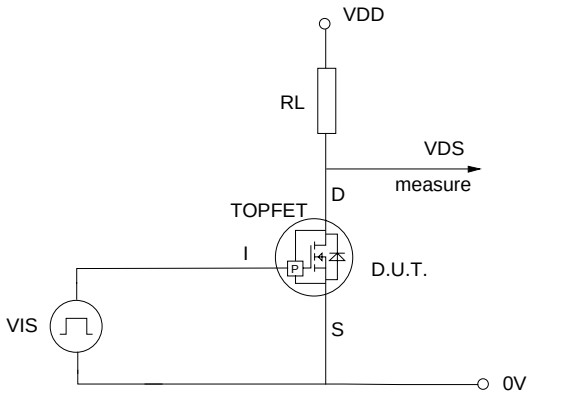



*Fig.14. Test circuit for resistive load switching times. $V_{IS}$ = 5 V*

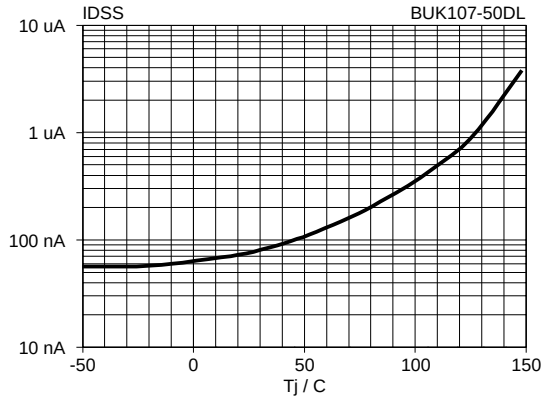



*Fig.16. Typical drain source leakage current $I_{DSS} = f(T_j)$; conditions: $V_{DS}$ = 40 V; $V_{IS}$ = 0 V.*

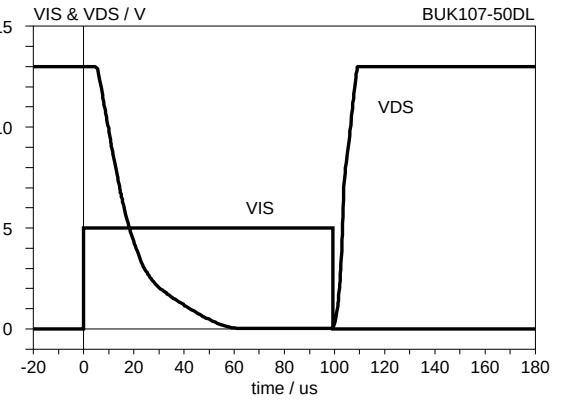



*Fig.15. Typical switching waveforms, resistive load . $R_L$ = 50 Ω; adjust $V_{DD}$ to obtain $I_D$ = 250 mA; $T_j$ = 25˚C*

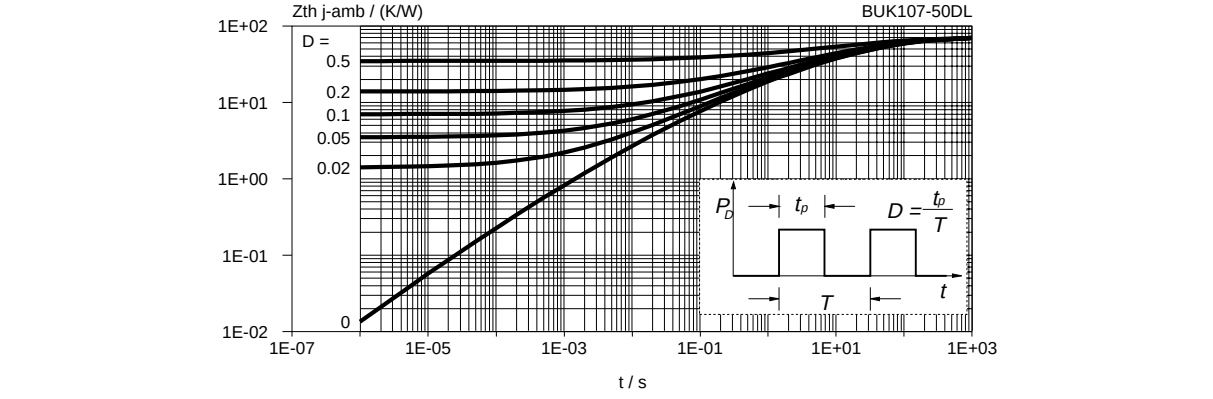



*Fig.17. Transient thermal impedance, TOPFET mounted on PCB of fig 19. $Z_{th\ j\text{-}amb} = f(t)$; parameter $D = t_p/T$*

## MOUNTING INSTRUCTIONS

*Dimensions in mm.*

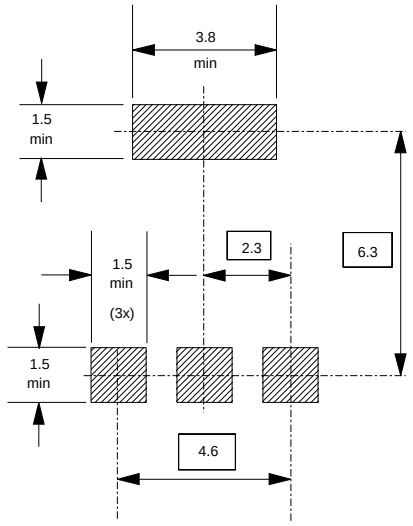



*Fig.18. Soldering pattern for surface mounting.*

## PRINTED CIRCUIT BOARD

*Dimensions in mm.*

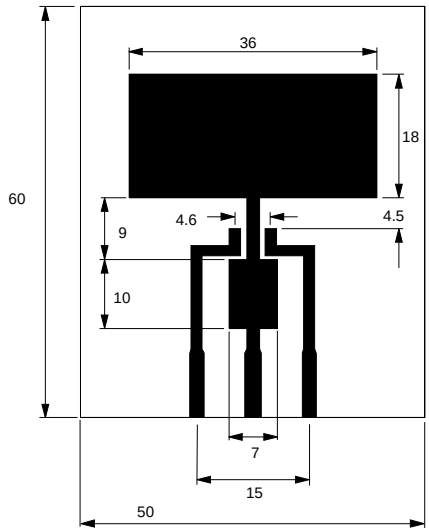



*Fig.19. PCB for thermal resistance and power rating. PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

## MECHANICAL DATA

*Dimensions in mm*

*Net Mass: 0.11 g*

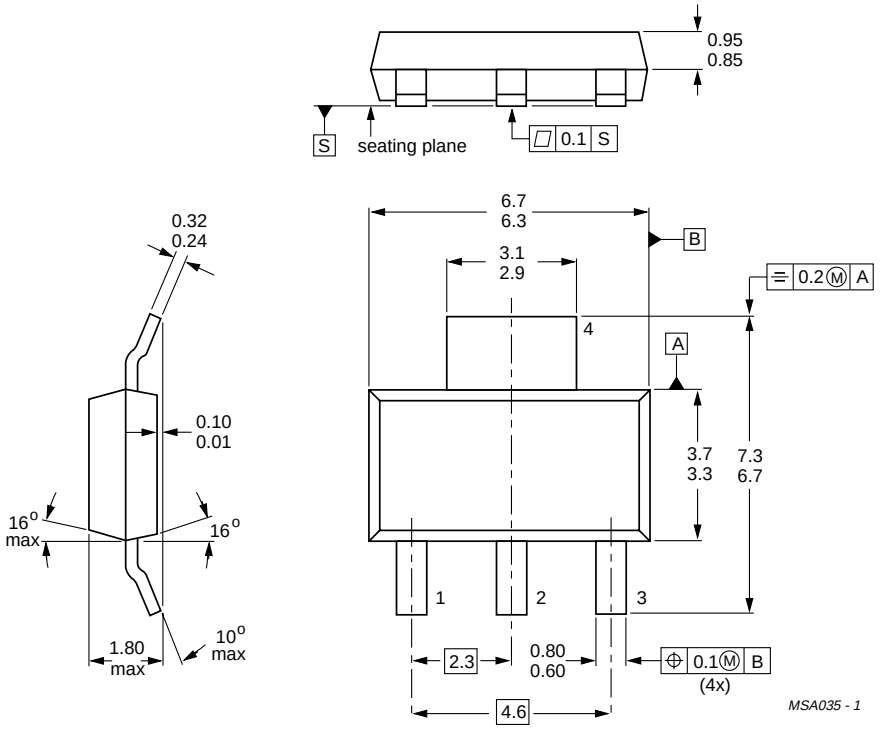



*Fig.20. SOT223 surface mounting package*[1].

**1** For further information, refer to surface mounting instructions for SOT223 envelope. Epoxy meets UL94 V0 at 1/8".

## DEFINITIONS

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |
|  | |
|  | |
|  | |

## LIFE SUPPORT APPLICATIONS

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