

PowerMOS transistor

BUK466-60A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

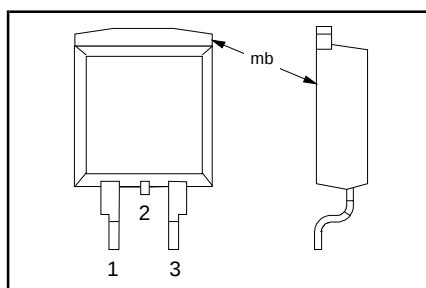
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	60	V
I_D	Drain current (DC)	52	A
P_{tot}	Total power dissipation	150	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance	0.028	Ω

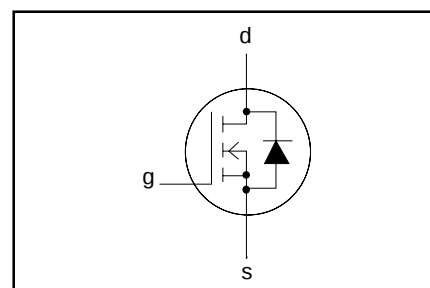
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	60	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	60	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	52	A
I_D	Drain current (DC)	$T_{mb} = 100 \text{ }^\circ\text{C}$	-	36	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	208	A
P_{tot}	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	150	W
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	-	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	1.0	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board (see Fig 18).	-	50	-	K/W

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STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA	60	-	-	V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA	2.1	3.0	4.0	V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	1	10	μA
I _{DSS}	Zero gate voltage drain current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 125 °C	-	0.1	1.0	mA
I _{GSS}	Gate source leakage current	V _{GS} = ±30 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 10 V; I _D = 29 A	-	0.024	0.028	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g _{fs}	Forward transconductance	V _{DS} = 25 V; I _D = 29 A	17	22	-	S
C _{iss}	Input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	1500	2000	pF
C _{oss}	Output capacitance		-	800	1000	pF
C _{rss}	Feedback capacitance		-	270	400	pF
t _{d on}	Turn-on delay time	V _{DD} = 30 V; I _D = 3 A; V _{GS} = 10 V; R _{GS} = 50 Ω; R _{gen} = 50 Ω	-	20	30	ns
t _r	Turn-on rise time		-	70	100	ns
t _{d off}	Turn-off delay time		-	170	220	ns
t _f	Turn-off fall time		-	120	160	ns
L _d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L _s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

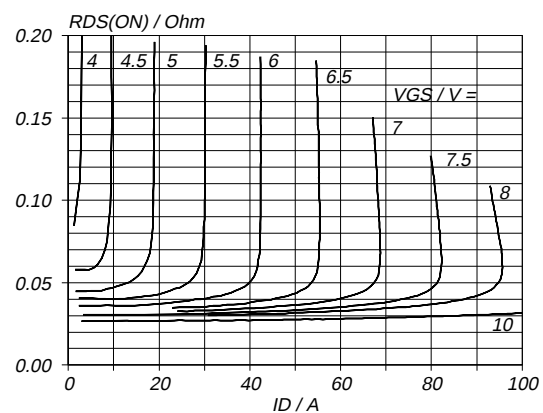
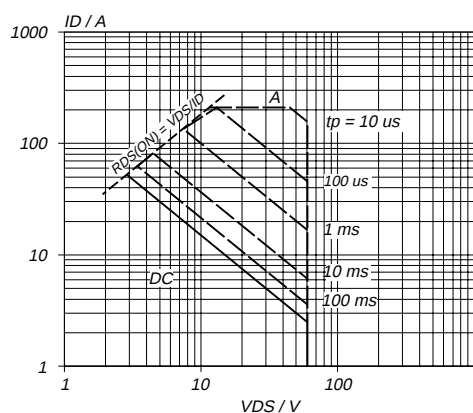
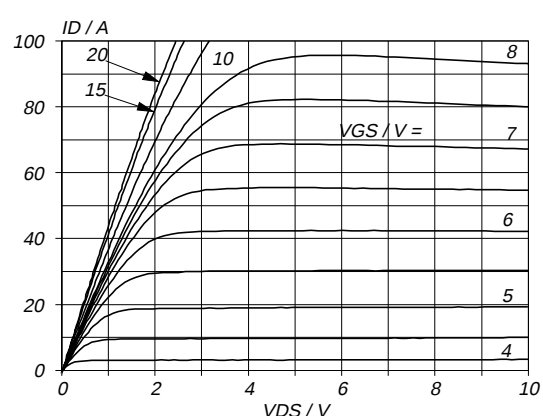
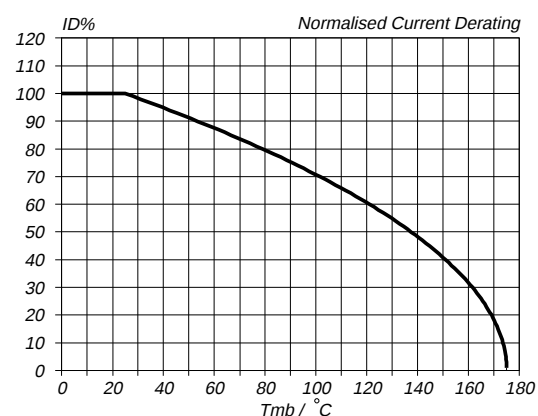
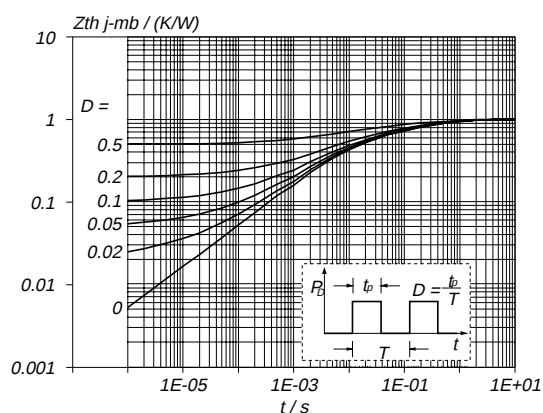
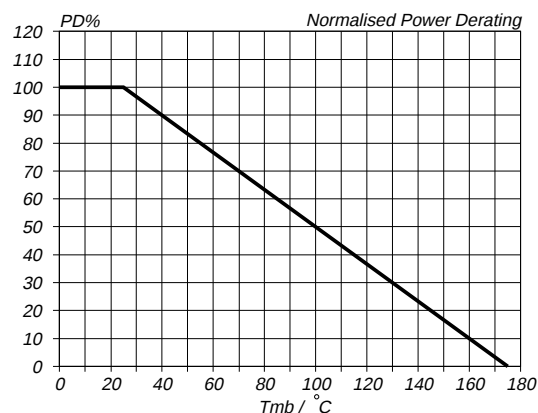
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{DR}	Continuous reverse drain current	-	-	-	52	A
I _{DRM}	Pulsed reverse drain current	-	-	-	208	A
V _{SD}	Diode forward voltage	I _F = 52 A; V _{GS} = 0 V	-	1.8	2.5	V
t _{rr}	Reverse recovery time	I _F = 52 A; -di _F /dt = 100 A/μs;	-	80	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = 0 V; V _R = 30 V	-	0.4	-	μC

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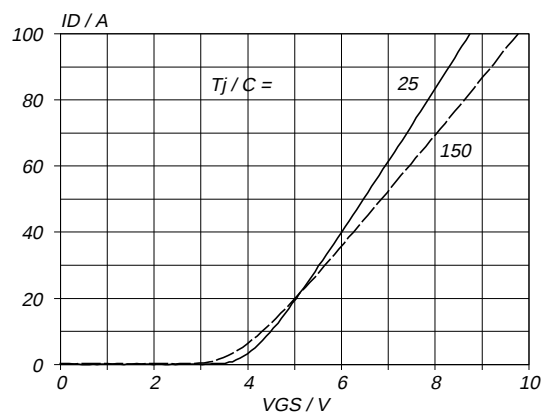


Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

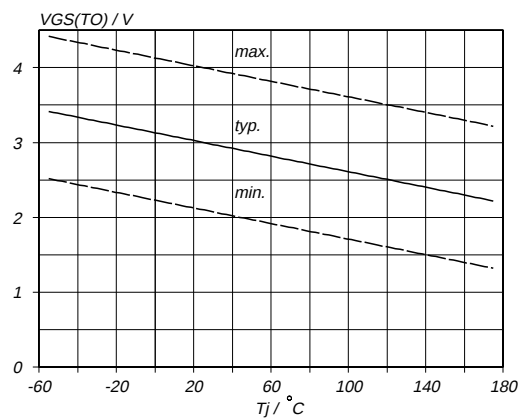


Fig.10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

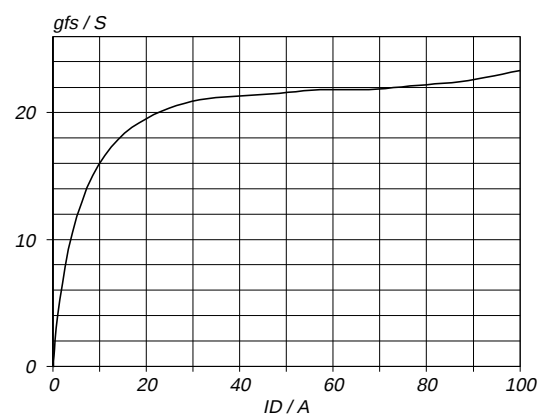


Fig.8. Typical transconductance, $T_j = 25\text{ °C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

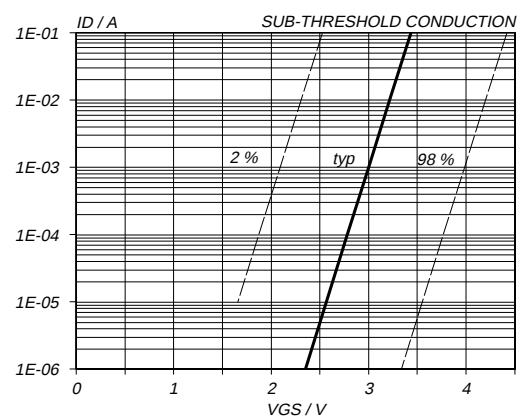


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25\text{ °C}$; $V_{DS} = V_{GS}$

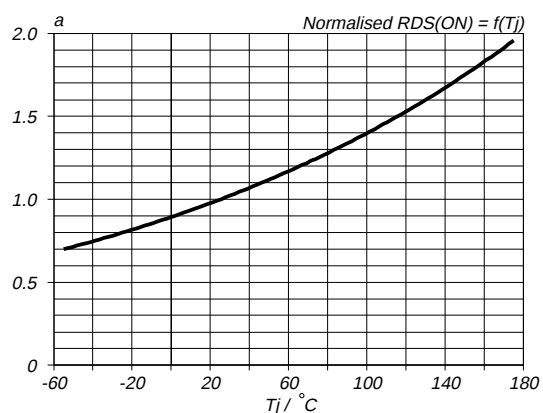


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ °C}} = f(T_j)$; $I_D = 29\text{ A}$; $V_{GS} = 10\text{ V}$

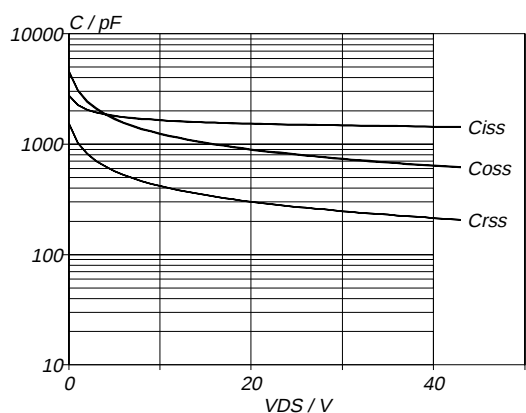
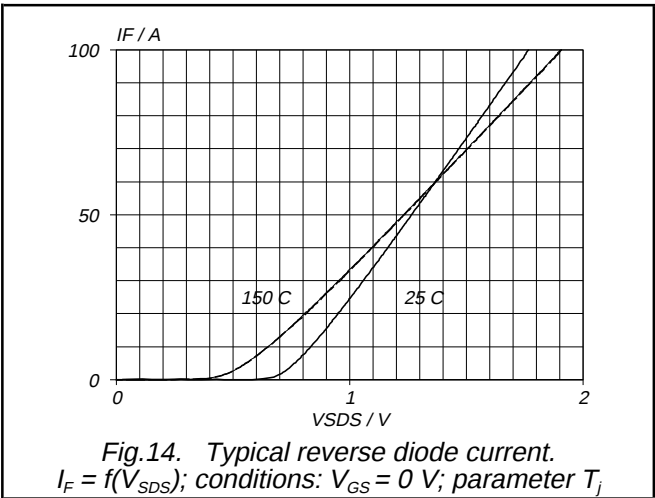
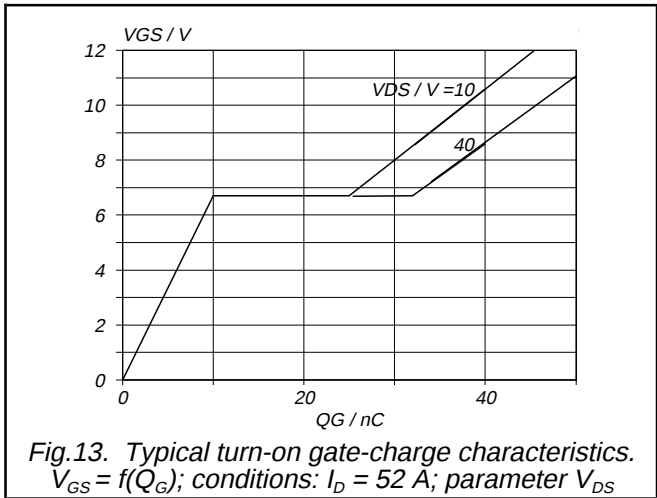


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

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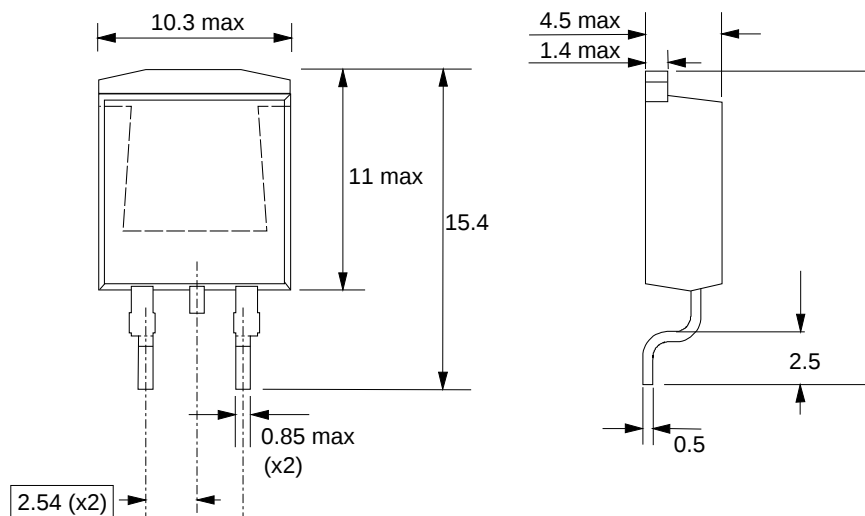
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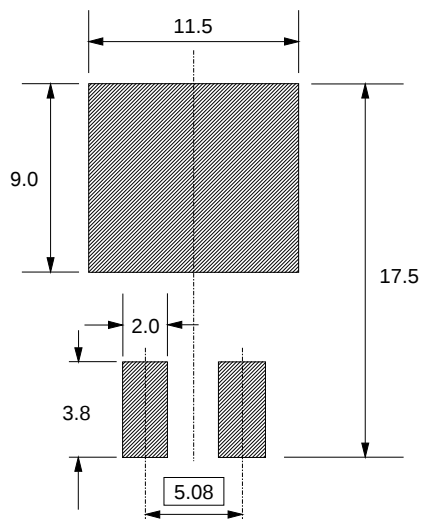
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MECHANICAL DATA

*Dimensions in mm**Net Mass: 1.4 g**Fig.15. SOT404 : centre pin connected to mounting base.*

MOUNTING INSTRUCTIONS

Dimensions in mm*Fig.16. SOT404 : soldering pattern for surface mounting.***Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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