

PowerMOS transistor

Logic level FET

BUK545-100A/B**GENERAL DESCRIPTION**

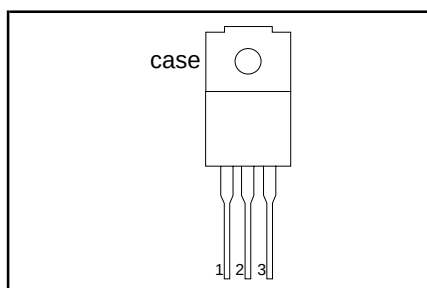
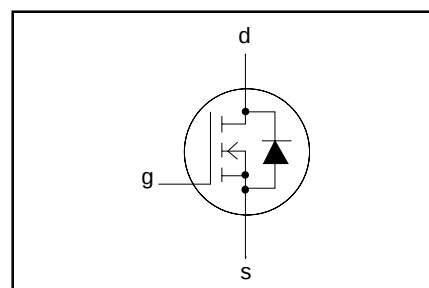
N-channel enhancement mode logic level field-effect power transistor in a plastic full-pack envelope.
The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in automotive and general purpose switching applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BUK545	-100A	-100B	
V_{DS}	Drain-source voltage	100	100	V
I_D	Drain current (DC)	13	12	A
P_{tot}	Total power dissipation	30	30	W
T_j	Junction temperature	150	150	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5\text{ V}$	0.085	0.11	Ω

PINNING - SOT186

PIN	DESCRIPTION
1	gate
2	drain
3	source
case	isolated

PIN CONFIGURATION**SYMBOL****LIMITING VALUES**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
$\pm V_{GSM}$	Non-repetitive gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$	-	20	V
I_D	Drain current (DC)	$T_{hs} = 25\text{ }^\circ\text{C}$	-	13	A
I_D	Drain current (DC)	$T_{hs} = 100\text{ }^\circ\text{C}$	-	8.2	A
I_{DM}	Drain current (pulse peak value)	$T_{hs} = 25\text{ }^\circ\text{C}$	-	52	A
P_{tot}	Total power dissipation	$T_{hs} = 25\text{ }^\circ\text{C}$	-	30	W
T_{stg}	Storage temperature	-	- 55	150	°C
T_j	Junction Temperature	-	-	150	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\text{ j-hs}}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	4.17	K/W
$R_{th\text{ j-a}}$	Thermal resistance junction to ambient		-	55	-	K/W

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STATIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA	100	-	-	V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA	1.0	1.5	2.0	V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	1	10	μA
I _{DSS}	Zero gate voltage drain current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 125 °C	-	0.1	1.0	mA
I _{GSS}	Gate source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 5 V; I _D = 13 A	-	0.075	0.085	Ω
		BUK545-100A	-	0.09	0.11	Ω
		BUK545-100B	-			

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g _{fs}	Forward transconductance	V _{DS} = 25 V; I _D = 13 A	10	13.5	-	S
C _{iss}	Input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	1450	1750	pF
C _{oss}	Output capacitance		-	280	350	pF
C _{rss}	Feedback capacitance		-	100	150	pF
t _{d on}	Turn-on delay time	V _{DD} = 30 V; I _D = 3 A;	-	25	40	ns
t _r	Turn-on rise time	V _{GS} = 5 V; R _{GS} = 50 Ω;	-	65	85	ns
t _{d off}	Turn-off delay time	R _{gen} = 50 Ω	-	135	180	ns
t _f	Turn-off fall time		-	80	110	ns
L _d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L _s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H. ≤ 65% ; clean and dustfree	-		1500	V
C _{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	12	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{DR}	Continuous reverse drain current	-	-	-	13	A
I _{DRM}	Pulsed reverse drain current	-	-	-	52	A
V _{SD}	Diode forward voltage	I _F = 13 A ; V _{GS} = 0 V	-	1.3	1.7	V
t _{rr}	Reverse recovery time	I _F = 13 A; -di _F /dt = 100 A/μs;	-	90	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = 0 V; V _R = 30 V	-	0.70	-	μC

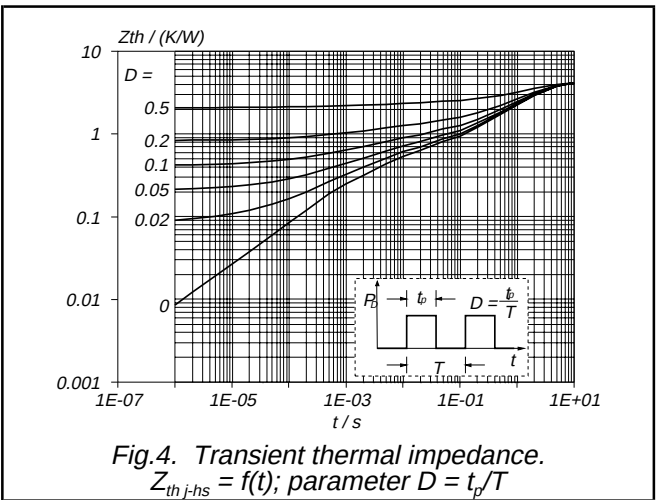
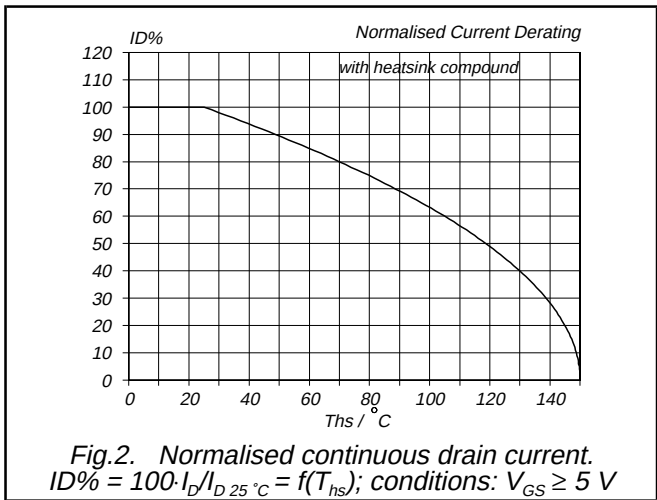
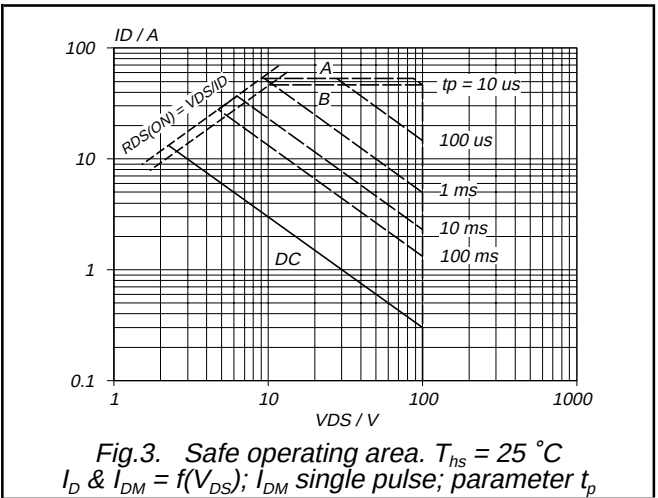
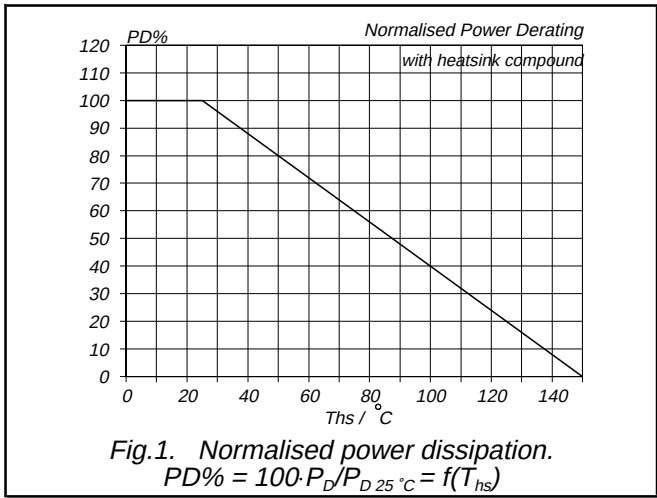
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AVALANCHE LIMITING VALUE

T_{hs} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W _{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I _D = 25 A ; V _{DD} ≤ 50 V ; V _{GS} = 5 V ; R _{GS} = 50 Ω	-	-	140	mJ



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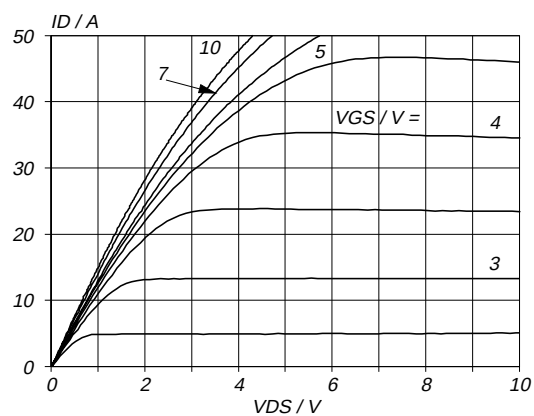
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Fig.5. Typical output characteristics, $T_j = 25\text{ }^{\circ}\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

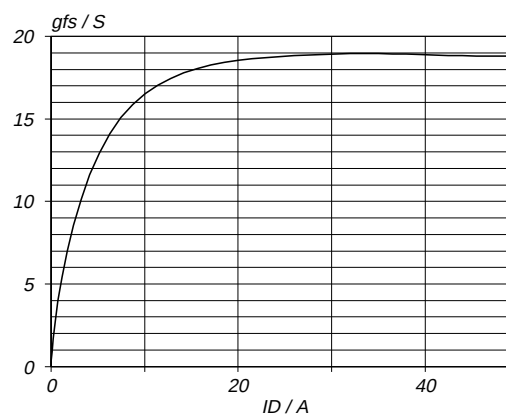


Fig.8. Typical transconductance, $T_j = 25\text{ }^{\circ}\text{C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

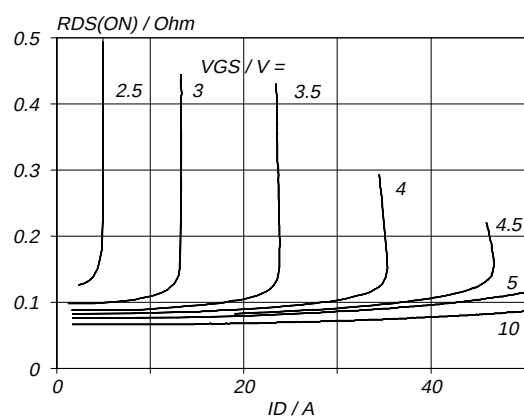


Fig.6. Typical on-state resistance, $T_j = 25\text{ }^{\circ}\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

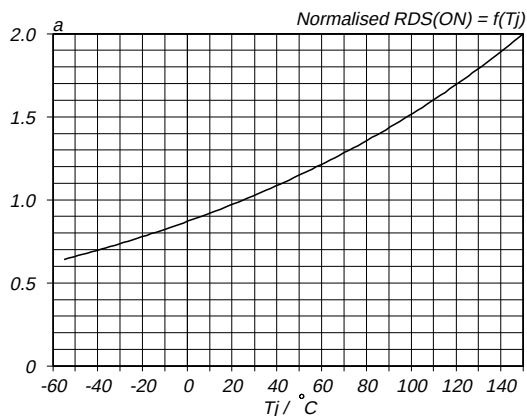


Fig.9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ }^{\circ}\text{C}} = f(T_j)$; $I_D = 13\text{ A}$; $V_{GS} = 5\text{ V}$

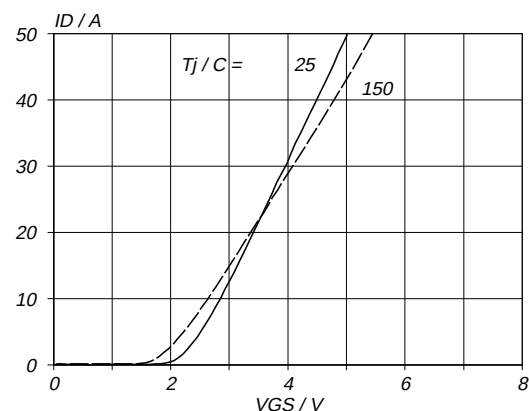


Fig.7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

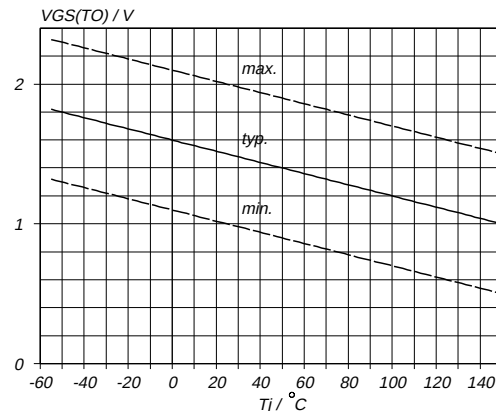


Fig.10. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

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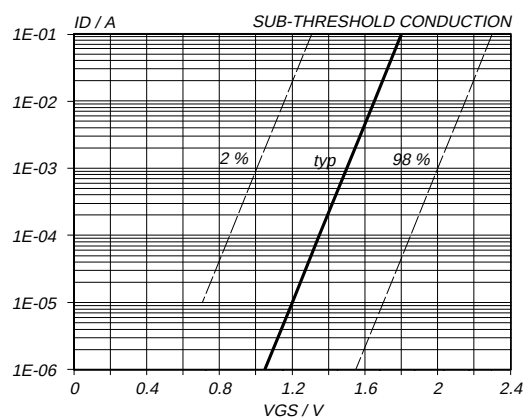


Fig.11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25^\circ\text{C}$; $V_{DS} = V_{GS}$

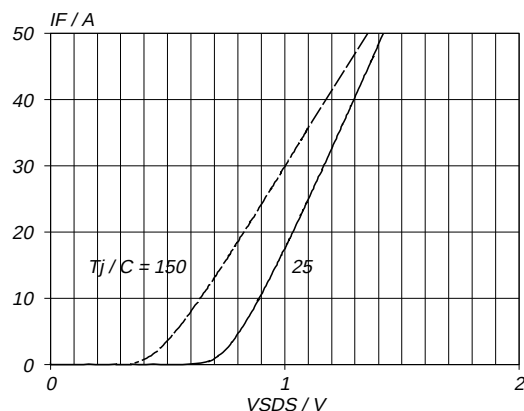


Fig.14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j

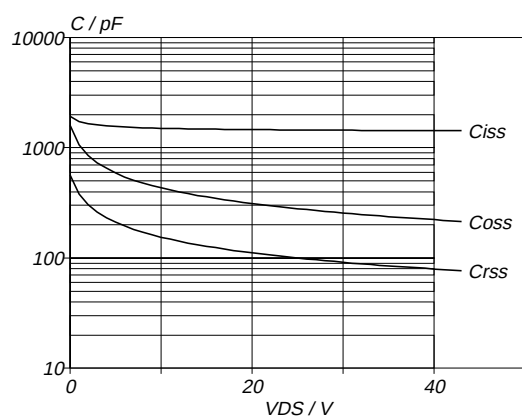


Fig.12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

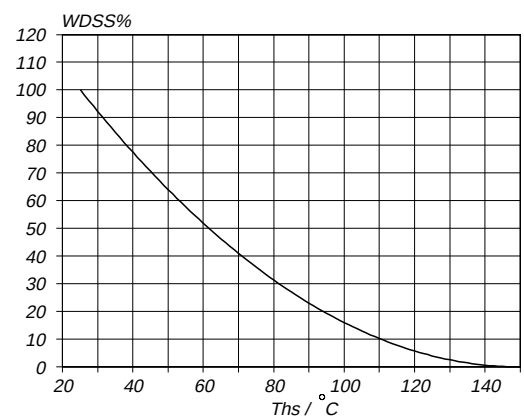


Fig.15. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{hs})$; conditions: $I_D = 25\text{ A}$

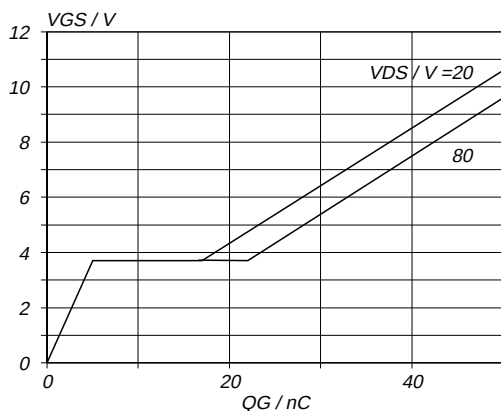


Fig.13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 25\text{ A}$; parameter V_{DS}

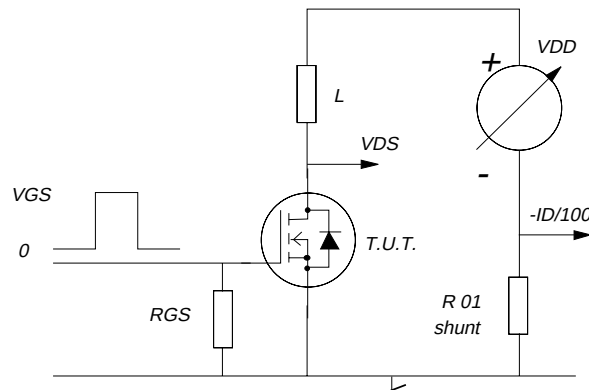


Fig.16. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS} / (BV_{DSS} - V_{DD})$

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MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

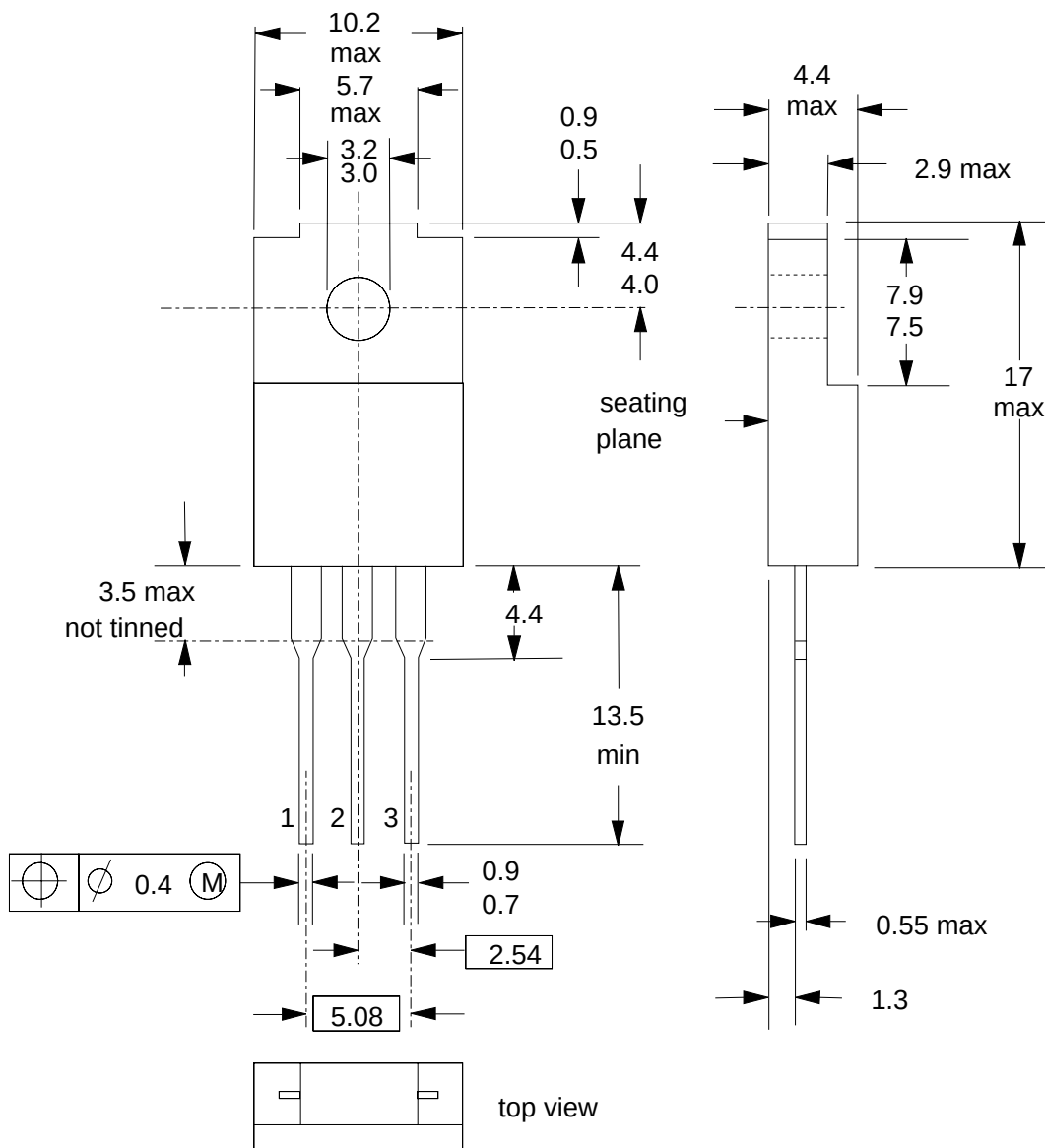


Fig.17. SOT186; The seating plane is electrically isolated from all terminals.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for F-pack envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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