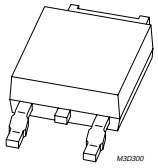


# BUK9214-30A

TrenchMOS™ logic level FET

**Rev. 01 — 20 March 2002** **Product data**

## 1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™[1] technology, featuring very low on-state resistance.

Product availability:

BUK9214-30A in SOT428 (D-PAK).

## 2. Features

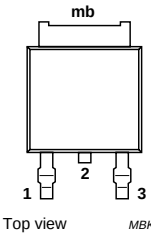
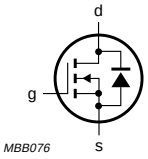
- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

## 3. Applications

- Automotive and general purpose power switching:
  - 12 V loads
  - Motors, lamps and solenoids.

## 4. Pinning information

**Table 1: Pinning - SOT428, simplified outline and symbol**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1 | gate (g) |  |  |
| 2 | drain (d) | | |
| 3 | source (s) | | |
| mb | mounting base; connected to drain (d) | | |



**SOT428 (D-PAK)**

1. TrenchMOS is a trademark of Koninklijke Philips Electronics.

PHILIPS

## 5. Quick reference data

**Table 2: Quick reference data**

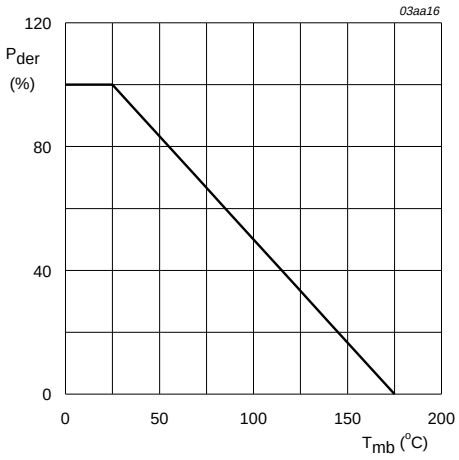
| Symbol | Parameter | Conditions | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | | - | 30 | V |
| $I_D$ | drain current (DC) | $T_{mb}$ = 25 °C; $V_{GS}$ = 5 V | - | 63 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C | - | 107 | W |
| $T_j$ | junction temperature | | - | 175 | °C |
| $R_{DSon}$ | drain-source on-state resistance | $T_j$ = 25 °C; $V_{GS}$ = 5 V; $I_D$ = 25 A | 11 | 14 | mΩ |
| | | $T_j$ = 25 °C; $V_{GS}$ = 4.5 V; $I_D$ = 25 A | - | 15.5 | mΩ |
| | | $T_j$ = 25 °C; $V_{GS}$ = 10 V; $I_D$ = 25 A | 9 | 12 | mΩ |

## 6. Limiting values

**Table 3: Limiting values**

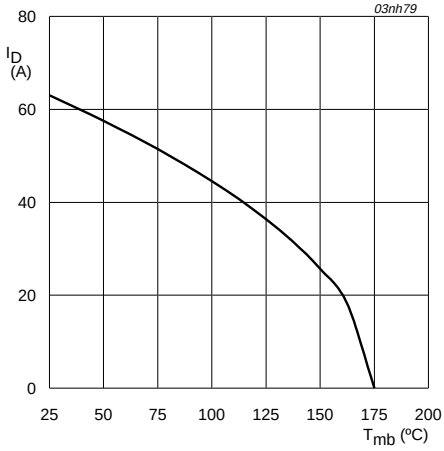
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage (DC) | | - | 30 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | $R_{GS}$ = 20 kΩ | - | 30 | V |
| $V_{GS}$ | gate-source voltage (DC) | | - | ±15 | V |
| $I_D$ | drain current (DC) | $T_{mb}$ = 25 °C; $V_{GS}$ = 5 V; Figure 2 and 3 | - | 63 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 5 V; Figure 2 | - | 45 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3 | - | 253 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Figure 1 | - | 107 | W |
| $T_{stg}$ | storage temperature | | –55 | +175 | °C |
| $T_j$ | operating junction temperature | | –55 | +175 | °C |
| **Source-drain diode** | | | | | |
| $I_{DR}$ | reverse drain current (DC) | $T_{mb}$ = 25 °C | - | 63 | A |
| $I_{DRM}$ | pulsed reverse drain current | $T_{mb}$ = 25 °C; pulsed; $t_p \leq 10$ µs | - | 253 | A |
| **Avalanche ruggedness** | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | unclamped inductive load; $I_D$ = 63 A; $V_{DS} \leq 30$ V; $V_{GS}$ = 5 V; $R_{GS}$ = 50 Ω; starting $T_j$ = 25 °C | - | 230 | mJ |



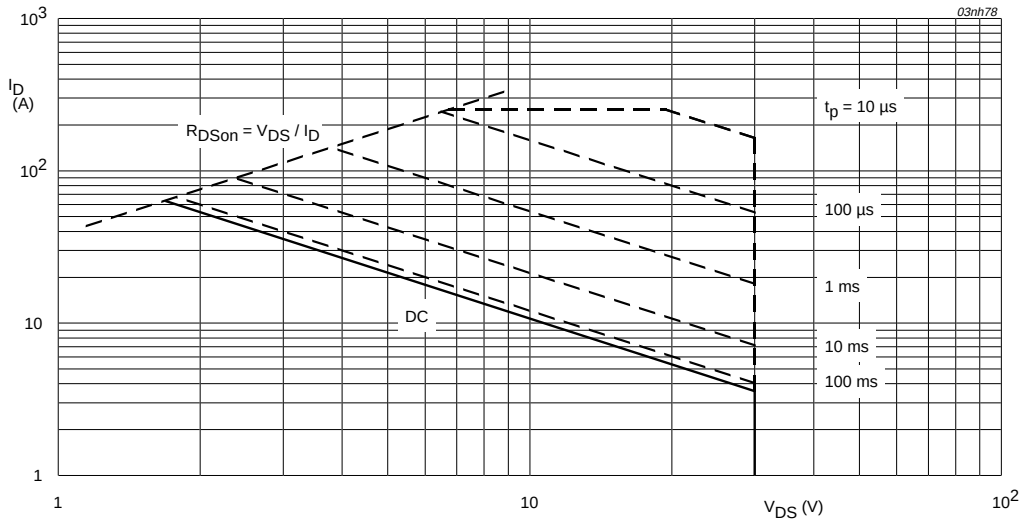

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**




$V_{GS} \geq 4.5$ V

**Fig 2. Continuous drain current as a function of mounting base temperature.**




$T_{mb}$ = 25 °C; $I_{DM}$ is single pulse.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

# 7. Thermal characteristics

**Table 4: Thermal characteristics**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Figure 4 | 1.4 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | | 71.4 | K/W |

## 7.1 Transient thermal impedance

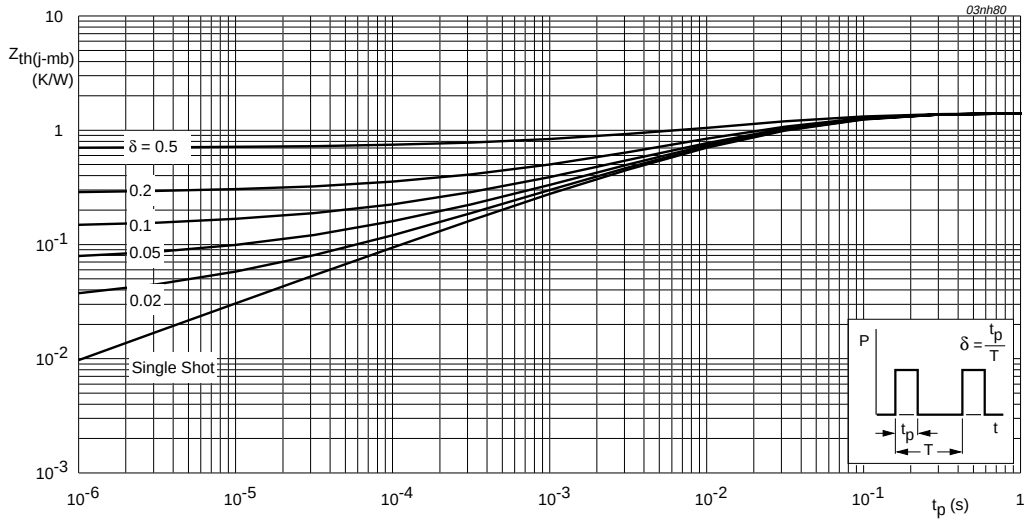



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.**

# 8. Characteristics

**Table 5: Characteristics**

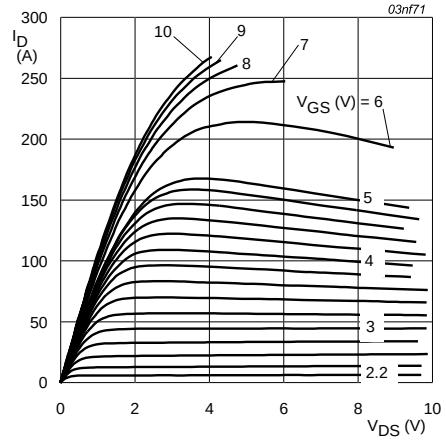
*$T_j$ = 25 °C unless otherwise specified*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 0.25 mA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | 30 | - | - | V |
| | | $T_j$ = –55 °C | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; Figure 9 | | | | |
| | | $T_j$ = 25 °C | 1 | 1.5 | 2 | V |
| | | $T_j$ = 175 °C | 0.5 | - | - | V |
| | | $T_j$ = –55 °C | - | - | 2.3 | V |
| $I_{DSS}$ | drain-source leakage current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | 0.05 | 10 | µA |
| | | $T_j$ = 175 °C | - | - | 500 | µA |
| $I_{GSS}$ | gate-source leakage current | $V_{GS}$ = ±10 V; $V_{DS}$ = 0 V | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 25 A; Figure 7 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 11 | 14 | mΩ |
| | | $T_j$ = 175 °C | - | - | 26.6 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; | - | - | 15.5 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; | - | 9 | 12 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{g(tot)}$ | total gate charge | $V_{GS}$ = 5 V; $V_{DD}$ = 24 V; $I_D$ = 25 A; Figure 14 | - | 31 | - | nC |
| $Q_{gs}$ | gate-to-source charge | | - | 5.3 | - | nC |
| $Q_{gd}$ | gate-to-drain (Miller) charge | | - | 12.2 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; Figure 12 | - | 1730 | 2317 | pF |
| $C_{oss}$ | output capacitance | | - | 400 | 481 | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 260 | 365 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DD}$ = 30 V; $R_L$ = 1.2 Ω; $V_{GS}$ = 5 V; $R_G$ = 10 Ω; | - | 10 | - | ns |
| $t_r$ | rise time | | - | 85 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 94 | - | ns |
| $t_f$ | fall time | | - | 108 | - | ns |
| $L_d$ | internal drain inductance | from drain to centre of die | - | 2.5 | - | nH |
| $L_s$ | internal source inductance | from source lead to source bond pad | - | 7.5 | - | nH |

**Table 5: Characteristics**...*continued*

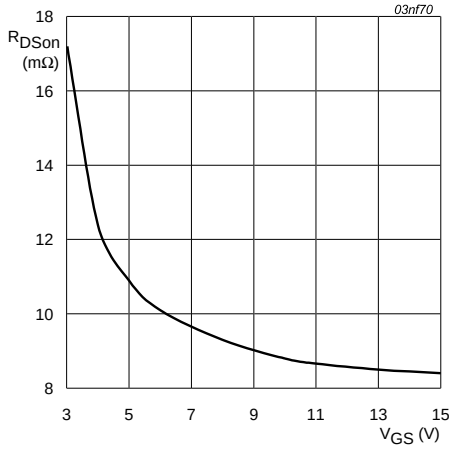
*$T_j$ = 25 °C unless otherwise specified*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain (diode forward) voltage | $I_S$ = 20 A; $V_{GS}$ = 0 V; Figure 15 | - | 0.85 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = −100 A/µs $V_{GS}$ = −10 V; $V_{DS}$ = 30 V | - | 83 | - | ns |
| $Q_r$ | recovered charge | | - | 119 | - | nC |



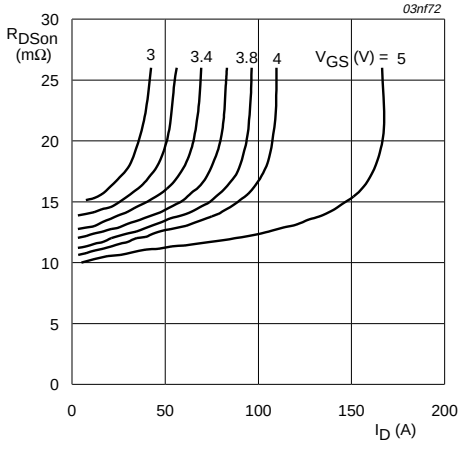

$T_j$ = 25 °C; $t_p$ = 300 µs

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



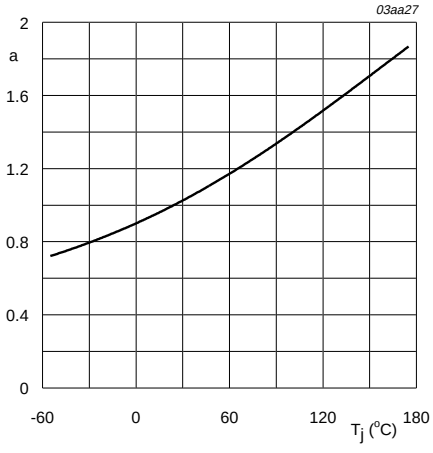

$T_j$ = 25 °C; $I_D$ = 25 A

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.**



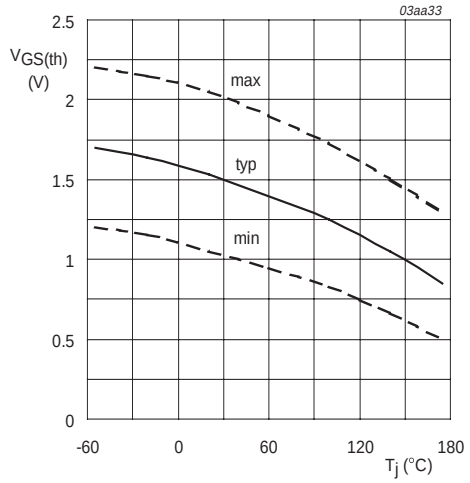

$T_j$ = 25 °C

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



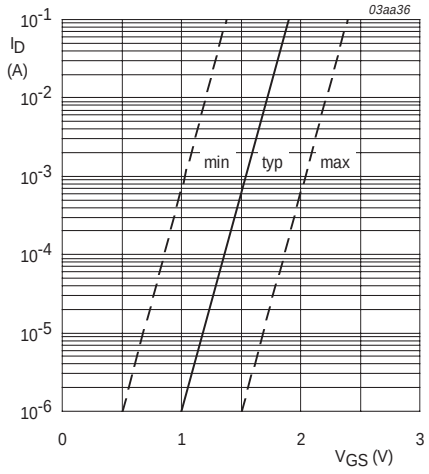

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



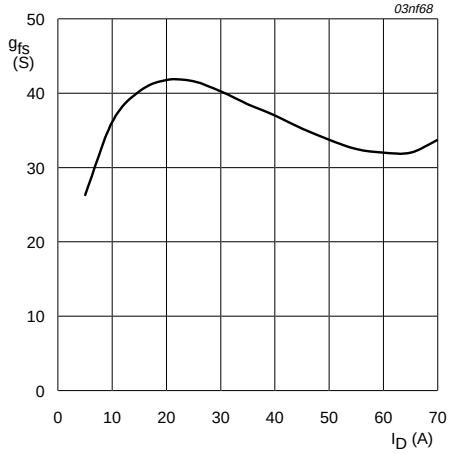

$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



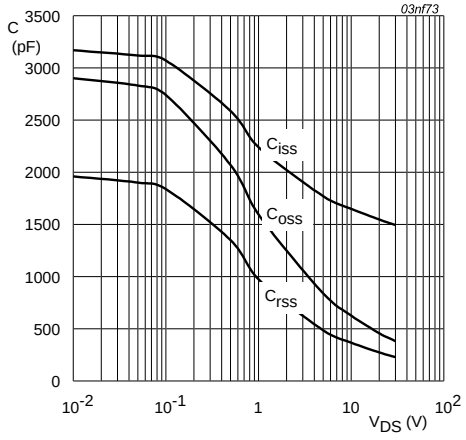

$T_j$ = 25 °C; $V_{DS}$ = $V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



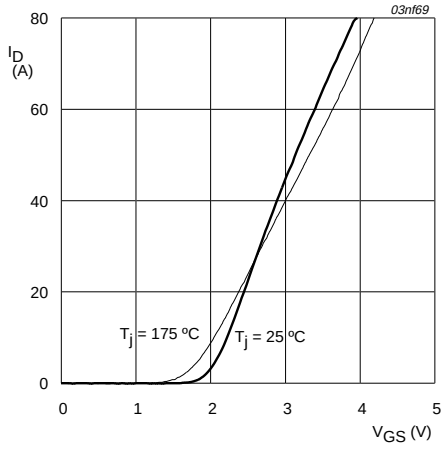

$T_j$ = 25 °C; $V_{DS}$ = 25 V

**Fig 11. Forward transconductance as a function of drain current; typical values.**



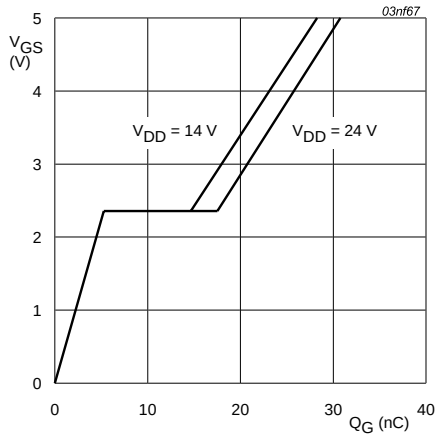

$V_{GS}$ = 0 V; f = 1 MHz

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



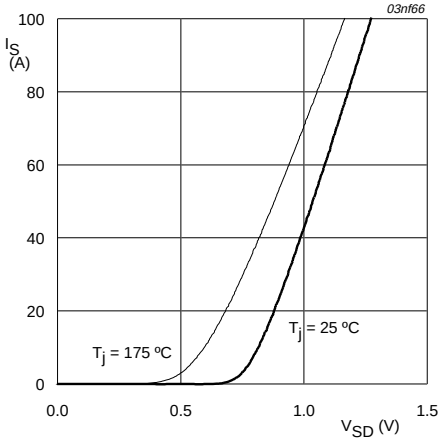

$V_{DS}$ = 25 V

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**




$T_j$ = 25 °C; $I_D$ = 25 A

**Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.**



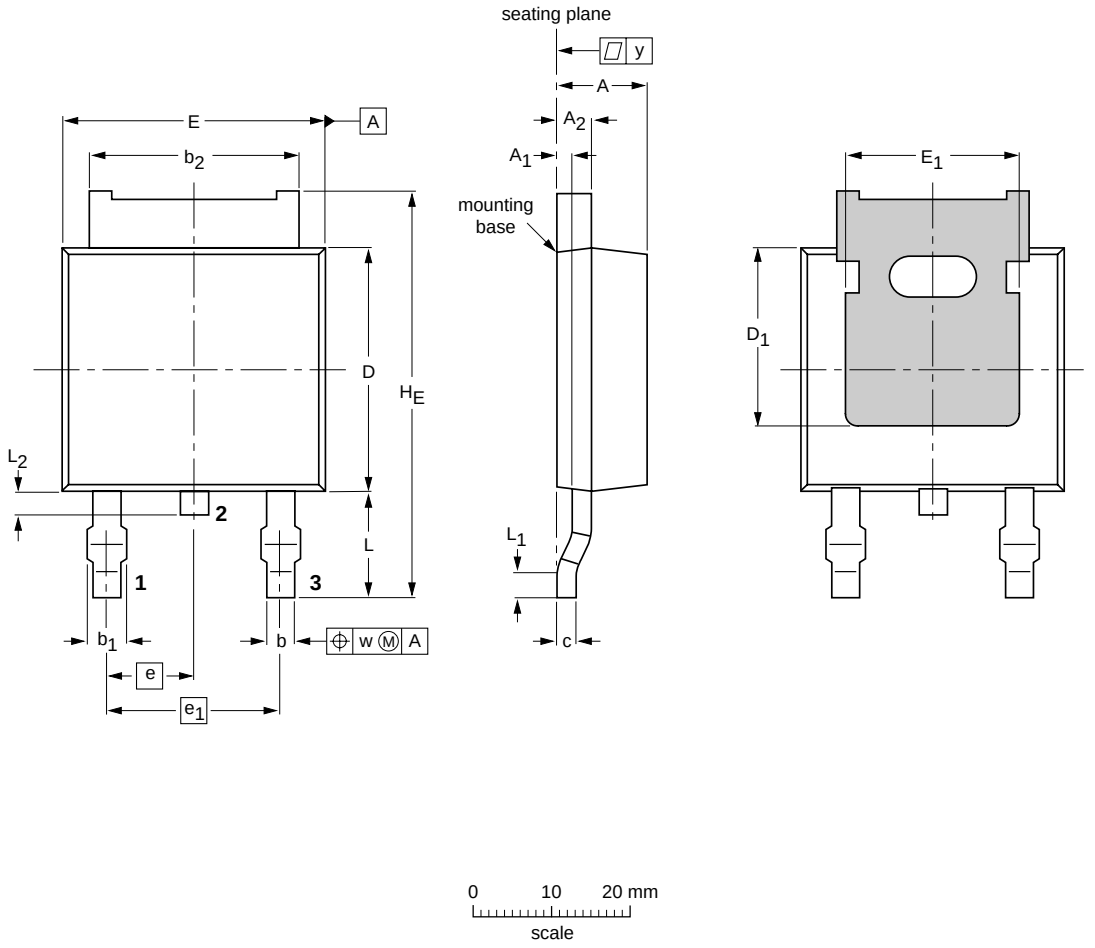

$V_{GS}$ = 0 V

**Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.**

# 9. Package outline

**Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)**

**SOT428**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ (1) | $A_2$ | b | $b_1$ | $b_2$ | c | D | $D_1$ min. | E | $E_1$ | e | $e_1$ | $H_E$ | L | $L_1$ min. | $L_2$ | w | y max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.38<br>2.22 | 0.65<br>0.45 | 0.93<br>0.73 | 0.89<br>0.71 | 1.1<br>0.9 | 5.46<br>5.26 | 0.4<br>0.2 | 6.22<br>5.98 | 4.0 | 6.73<br>6.47 | 4.81<br>4.45 | 2.285 | 4.57 | 10.4<br>9.6 | 2.95<br>2.55 | 0.5 | 0.9<br>0.5 | 0.2 | 0.2 |

**Note**

1. Measured from heatsink back to lead.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT428 | | TO-252 | SC-63 | | | ~~99-09-13~~<br>01-12-11 |

**Fig 16. SOT428 (D-PAK).**

## 10. Revision history

Table 6: Revision history

| Rev | Date | CPCN | Description |
|---|---|---|---|
| 01 | 20020320 | - | Product specification, initial version. |

## 11. Data sheet status

| Data sheet status[1] | Product status[2] | Definition |
|---|---|---|
| Objective data | Development | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice. |
| Preliminary data | Qualification | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product. |
| Product data | Production | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A. |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

## 12. Definitions

**Short-form specification —** The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition —** Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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# Contents





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