



BUK9560-100A; BUK9660-100A

TrenchMOS™ logic level FET

Rev. 01 — 22 January 2001

Product specification

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance.

Product availability:

BUK9560-100A in SOT78 (TO-220AB)

BUK9660-100A in SOT404 (D²-PAK).

2. Features

- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

3. Applications

- Automotive and general purpose power switching:
 - ◆ 12 V, 24 V and 42 V loads
 - ◆ Motors, lamps and solenoids.

4. Pinning information

Table 1: Pinning - SOT78 and SOT404, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
mb	mounting base; connected to drain (d)		
		SOT78 (TO-220AB)	SOT404 (D²-PAK)



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5. Quick reference data

Table 2: Quick reference data

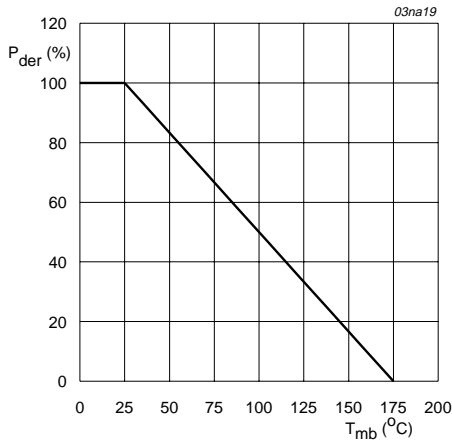
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)		–	100	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}$	–	26	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$	–	106	W
T_j	junction temperature		–	175	°C
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C}$	51	60	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C}$	–	67	mΩ

6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		–	100	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	–	100	V
V_{GS}	gate-source voltage (DC)		–	±10	V
V_{GSM}	non-repetitive gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$	–	±15	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2 and 3	–	26	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2	–	19	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	–	106	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	–	106	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	–	26	A
I_{DRM}	pulsed reverse drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	–	106	A
Avalanche ruggedness					
W_{DSS}	non-repetitive avalanche energy	unclamped inductive load; $I_D = 20\text{ A};$ $V_{DS} \leq 100\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_{mb} = 25\text{ °C}$	–	30	mJ



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

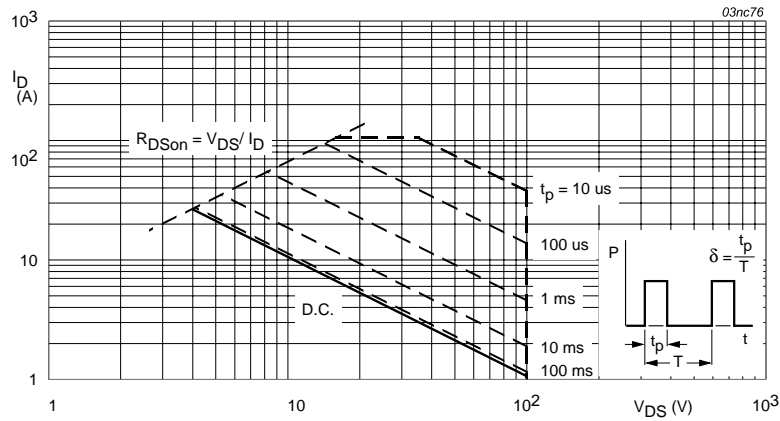
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$V_{GS} \geq 4.5 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT78 package	60	K/W
		mounted on printed circuit board; minimum footprint; SOT404 package	50	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	1.4	K/W

7.1 Transient thermal impedance

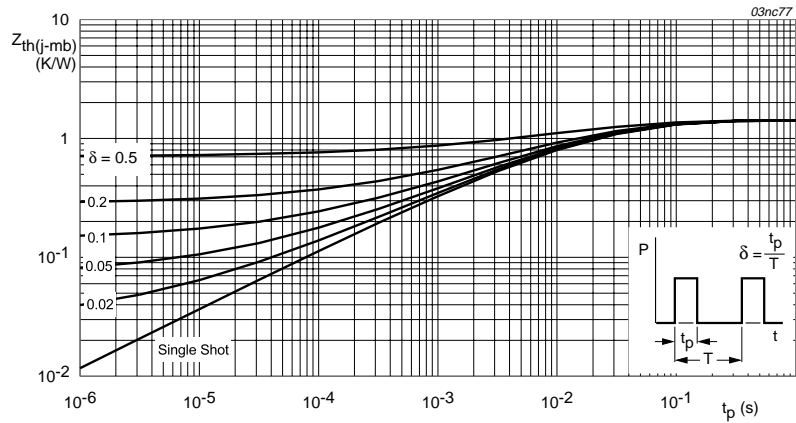


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

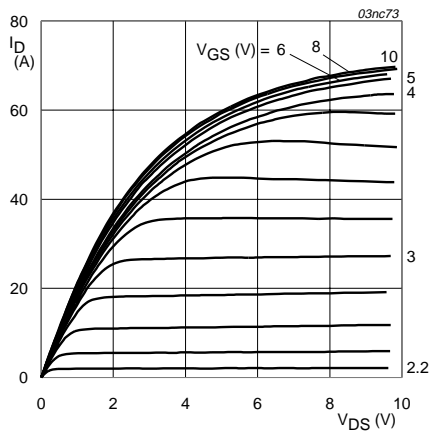
$T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	100	–	–	V
		$T_j = -55\text{ °C}$	89	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ Figure 9				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 175\text{ °C}$	0.5	–	–	V
		$T_j = -55\text{ °C}$	–	–	2.3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 100\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	–	0.05	10	μA
		$T_j = 175\text{ °C}$	–	–	500	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$	–	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 15\text{ A};$ Figure 7 and 8				
		$T_j = 25\text{ °C}$	–	51	60	m Ω
		$T_j = 175\text{ °C}$	–	–	150	m Ω
		$V_{GS} = 4.5\text{ V}; I_D = 15\text{ A}$	–	–	67	m Ω
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A}$	–	49	58	m Ω
Dynamic characteristics						
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$ $f = 1\text{ MHz};$ Figure 12	–	1440	1924	pF
C_{oss}	output capacitance		–	155	186	pF
C_{rss}	reverse transfer capacitance		–	100	138	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 30\text{ V}; R_L = 1.2\ \Omega;$	–	20	–	ns
t_r	rise time	$V_{GS} = 5\text{ V}; R_G = 10\ \Omega$	–	124	–	ns
$t_{d(off)}$	turn-off delay time		–	68	–	ns
t_f	fall time		–	67	–	ns
L_d	internal drain inductance	from drain lead 6 mm from package to centre of die	–	4.5	–	nH
		from contact screw on mounting base to centre of die SOT78	–	3.5	–	nH
		from upper edge of drain mounting base to centre of die SOT404	–	2.5	–	nH
L_s	internal source inductance	from source lead to source bond pad	–	7.5	–	nH

Table 5: Characteristics...continued

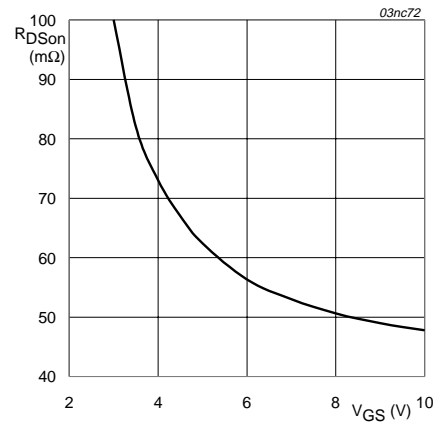
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 15	–	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$	–	61	–	ns
Q_r	recovered charge	$V_{GS} = -10\text{ V}$; $V_{DS} = 30\text{ V}$	–	200	–	nC



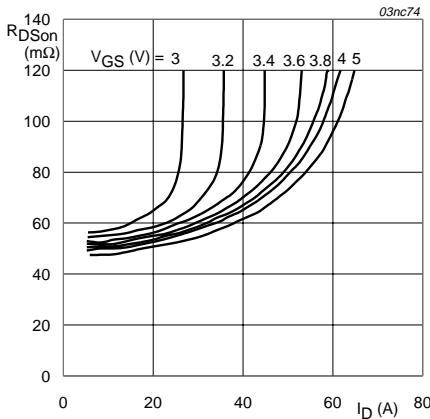
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



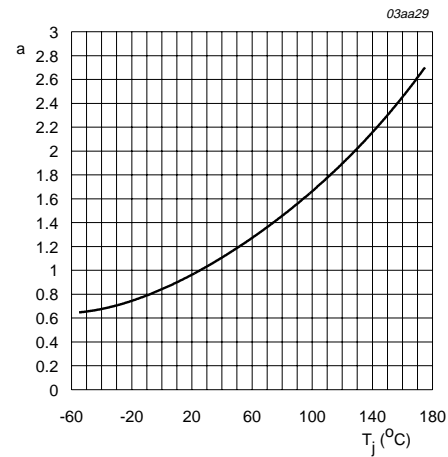
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 15\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{Dson}}{R_{Dson(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



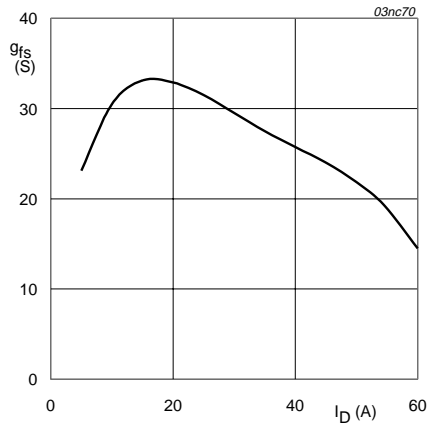
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



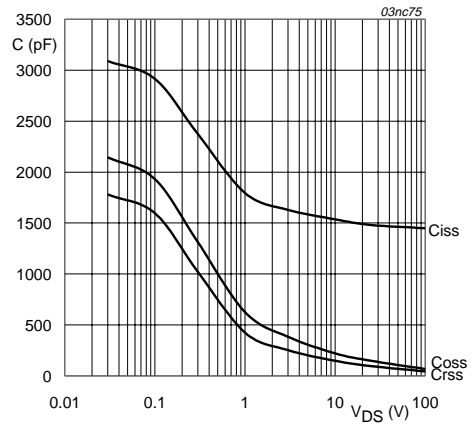
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



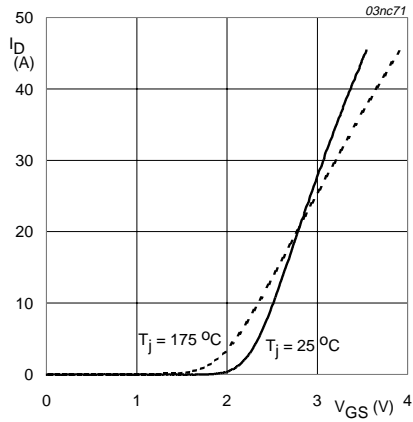
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



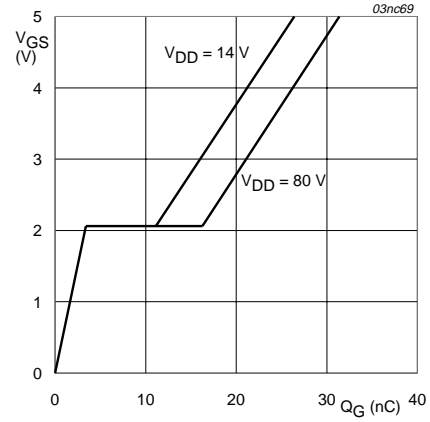
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



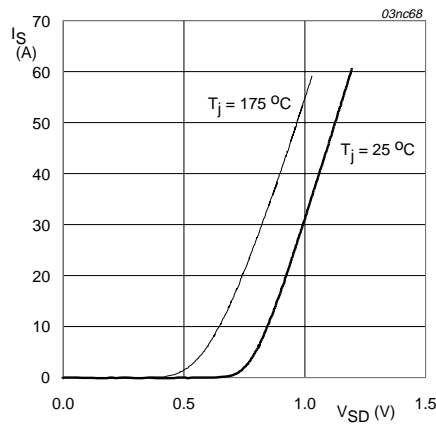
$V_{DS} = 25\text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}; I_D = 15\text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



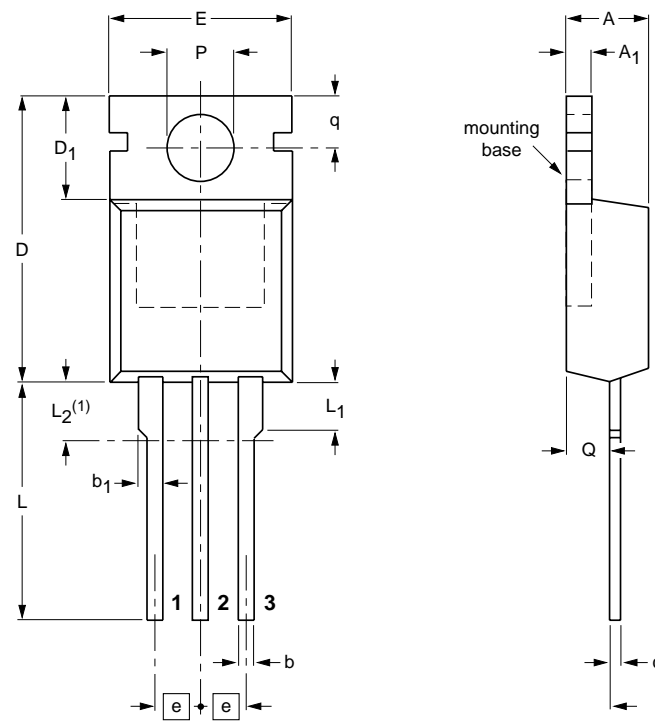
$V_{GS} = 0\text{ V}$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁	c	D	D ₁	E	e	L	L ₁	L ₂ ⁽¹⁾ max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

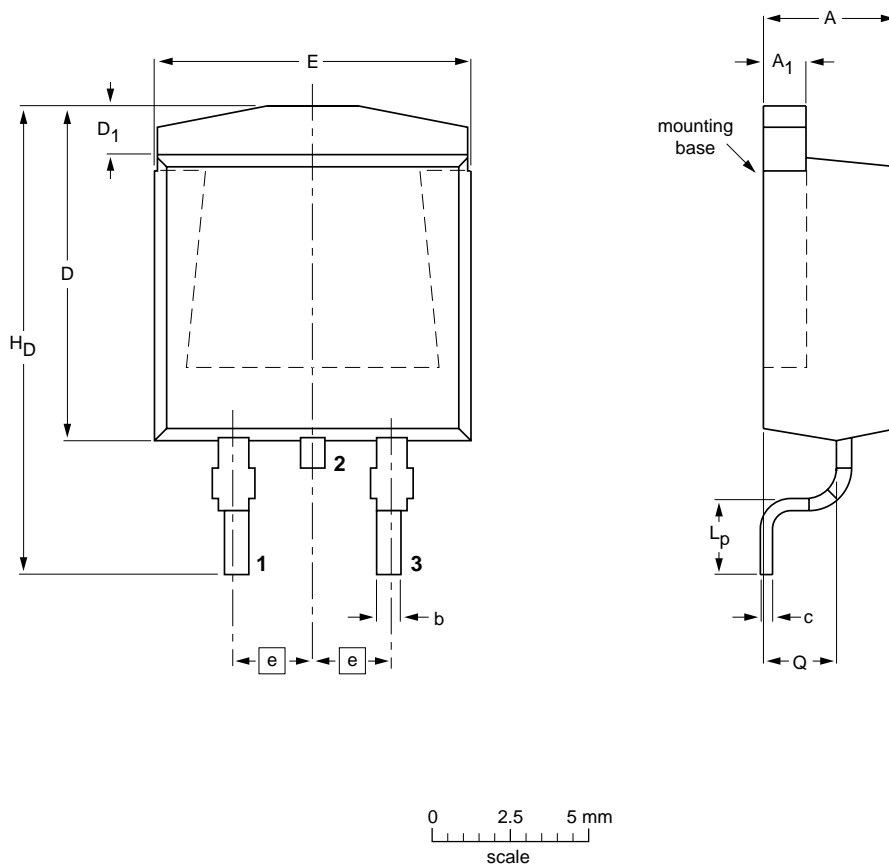
1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			99-09-13 00-09-07

Fig 16. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads
(one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D max.	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.40 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						98-12-14 99-06-25

Fig 17. SOT404 (D²-PAK).

10. Soldering



11. Revision history

Table 6: Revision history

Rev	Date	GPCN	Description
01	20010122	-	Product Specification; initial version

12. Data sheet status

Datasheet status	Product status	Definition ^[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Australia: Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

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Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Tel. +359 268 9211, Fax. +359 268 9102

Canada: Tel. +1 800 234 7381

China/Hong Kong: Tel. +852 2 319 7888, Fax. +852 2 319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Tel. +45 3 288 2636, Fax. +45 3 157 0044

Finland: Tel. +358 961 5800, Fax. +358 96 158 0920

France: Tel. +33 14 099 6161, Fax. +33 14 099 6427

Germany: Tel. +49 40 23 5360, Fax. +49 402 353 6300

Hungary: Tel. +36 1 382 1700, Fax. +36 1 382 1800

India: Tel. +91 22 493 8541, Fax. +91 22 493 8722

Indonesia: see Singapore

Ireland: Tel. +353 17 64 0000, Fax. +353 17 64 0200

Israel: Tel. +972 36 45 0444, Fax. +972 36 49 1007

Italy: Tel. +39 039 203 6838, Fax. +39 039 203 6800

Japan: Tel. +81 33 740 5130, Fax. +81 3 3740 5057

Korea: Tel. +82 27 09 1412, Fax. +82 27 09 1415

Malaysia: Tel. +60 37 50 5214, Fax. +60 37 57 4880

Mexico: Tel. +9-5 800 234 7381

Middle East: see Italy

For all other countries apply to: Philips Semiconductors,
Marketing Communications,
Building BE, P.O. Box 218, 5600 MD EINDHOVEN,
The Netherlands, Fax. +31 40 272 4825

Netherlands: Tel. +31 40 278 2785, Fax. +31 40 278 8399

New Zealand: Tel. +64 98 49 4160, Fax. +64 98 49 7811

Norway: Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Tel. +63 28 16 6380, Fax. +63 28 17 3474

Poland: Tel. +48 22 5710 000, Fax. +48 22 5710 001

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Romania: see Italy

Russia: Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Tel. +34 33 01 6312, Fax. +34 33 01 4107

Sweden: Tel. +46 86 32 2000, Fax. +46 86 32 2745

Switzerland: Tel. +41 14 88 2686, Fax. +41 14 81 7730

Taiwan: Tel. +886 22 134 2451, Fax. +886 22 134 2874

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Turkey: Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: Tel. +1 800 234 7381

Uruguay: see South America

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