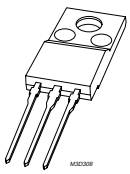


BUK9775-55A

N-channel TrenchMOS™ logic level FET

Rev. 02 — 10 June 2004 **Product data**

1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™[1] technology, featuring very low on-state resistance.

Product availability:

BUK9775-55A in SOT186A (TO-220F).

2. Features

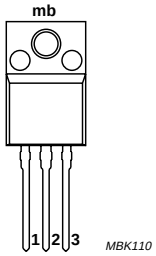
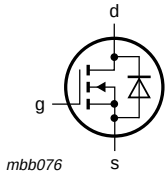
- TrenchMOS™ technology
- Q101 compliant
- 150 °C rated
- Logic level compatible.

3. Applications

- Automotive and general purpose power switching:
  - 12 V and 24 V loads
  - Motors, lamps and solenoids.

4. Pinning information

Table 1: Pinning - SOT186A, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d)		
3	source (s)		
mb	mounting base; isolated		

SOT186A (TO-220F)

1. TrenchMOS is a trademark of Koninklijke Philips Electronics N.V.

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5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)		-	55	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V	-	11	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	-	18	W
T_j	junction temperature		-	150	°C
R_{DSon}	drain-source on-state resistance	T_j = 25 °C; V_{GS} = 5 V; I_D = 10 A	63	75	mΩ
		T_j = 25 °C; V_{GS} = 4.5 V; I_D = 10 A	-	84	mΩ

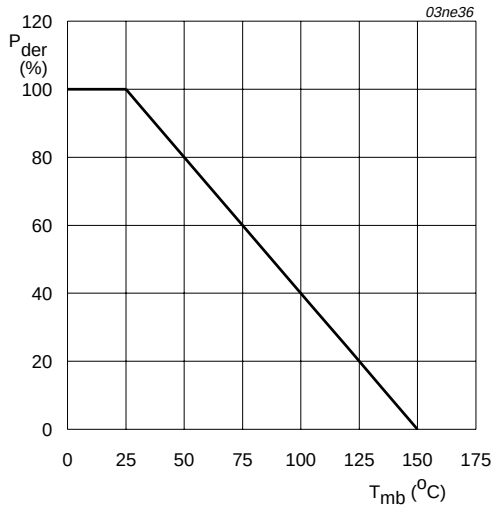
6. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

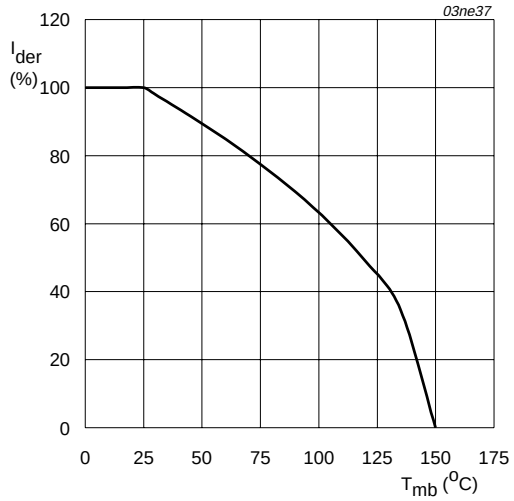
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage (DC)			-	55	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		-	55	V
V_{GS}	gate-source voltage (DC)			-	±10	V
V_{GSM}	non-repetitive gate-source voltage	$t_p \leq 50$ µs		-	±15	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3		-	11	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2		-	8	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3	[1]	-	46	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1		-	18	W
T_{stg}	storage temperature			–55	+150	°C
T_j	operating junction temperature			–55	+150	°C
Source-drain diode						
I_{DR}	reverse drain current (DC)	T_{mb} = 25 °C		-	11	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs		-	46	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive avalanche energy	unclamped inductive load; I_D = 11 A; $V_{DS} \leq 55$ V; V_{GS} = 5 V; R_{GS} = 50 Ω; starting T_j = 25 °C		-	50	mJ

[1] I_{DM} is limited by chip, not package.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

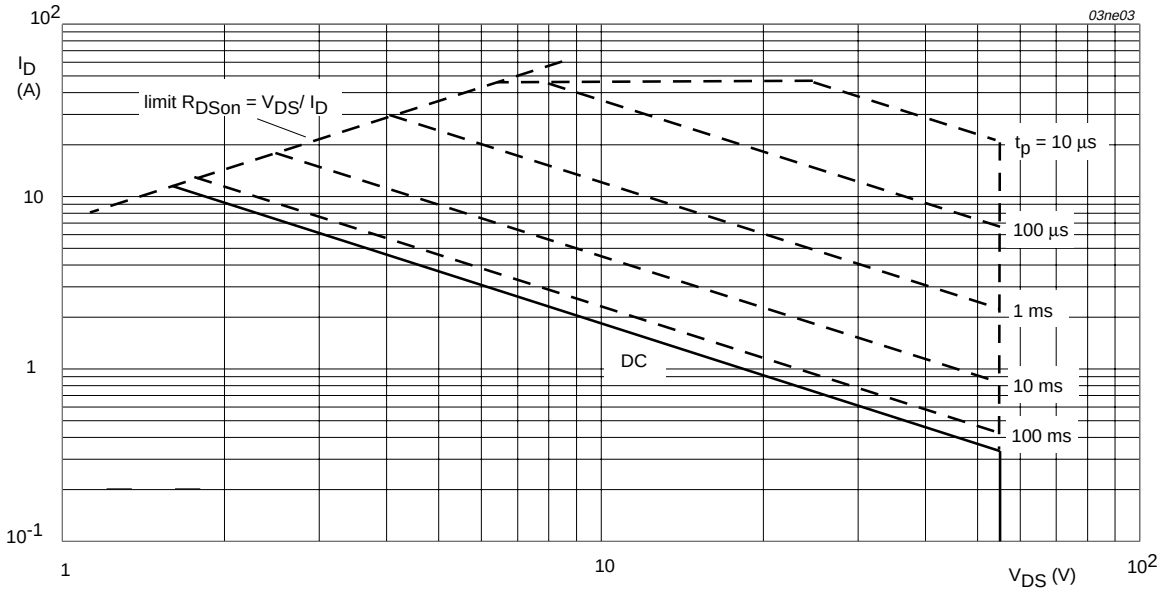
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 5$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{amb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	6.8	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	55	-	K/W

7.1 Transient thermal impedance

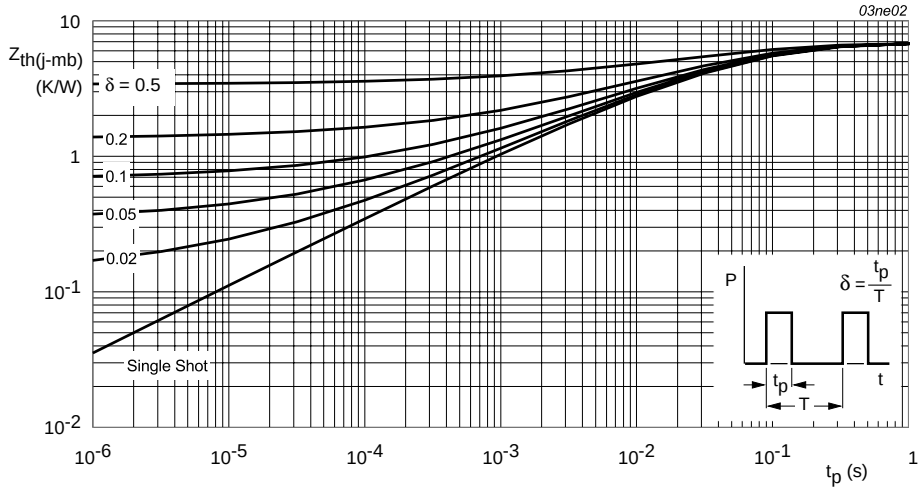


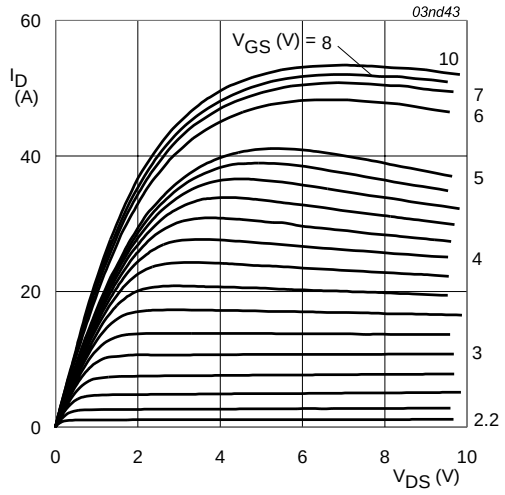
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

Table 5: Characteristics

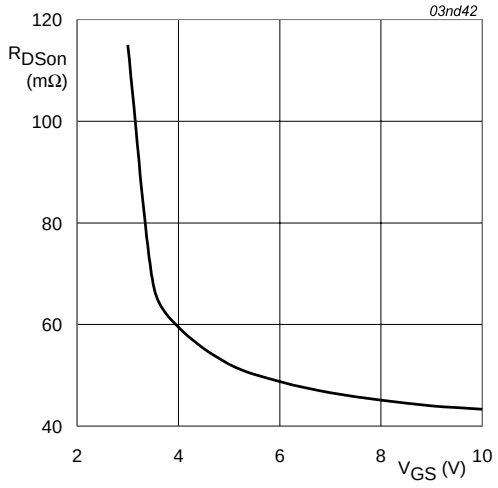
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	55	-	-	V
		T_j = –55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	1	1.5	2	V
		T_j = 150 °C	0.6	-	-	V
		T_j = –55 °C	-	-	2.3	V
I_{DSS}	drain-source leakage current	V_{DS} = 55 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	10	µA
		T_j = 150 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 10 A; Figure 7 and 8				
		T_j = 25 °C	-	63	75	mΩ
		T_j = 150 °C	-	-	138	mΩ
		V_{GS} = 4.5 V; I_D = 10 A	-	-	84	mΩ
		V_{GS} = 10 V; I_D = 10 A	-	57	68	mΩ
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	V_{GS} = 5 V; V_{DD} = 44 V; I_D = 10 A; Figure 14	-	10.5	-	nC
Q_{gs}	gate-to-source charge		-	1.6	-	nC
Q_{gd}	gate-to-drain (Miller) charge		-	4.6	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	-	440	630	pF
C_{oss}	output capacitance		-	90	110	pF
C_{rss}	reverse transfer capacitance		-	60	94	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; R_G = 10 Ω	-	10	-	ns
t_r	rise time		-	47	-	ns
$t_{d(off)}$	turn-off delay time		-	28	-	ns
t_f	fall time		-	33	-	ns
L_d	internal drain inductance	from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	internal source inductance	from source lead 6 mm from package to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 10 A; V_{GS} = 0 V; Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs V_{GS} = –10 V; V_{DS} = 30 V	-	33	-	ns
Q_r	recovered charge		-	60	-	nC



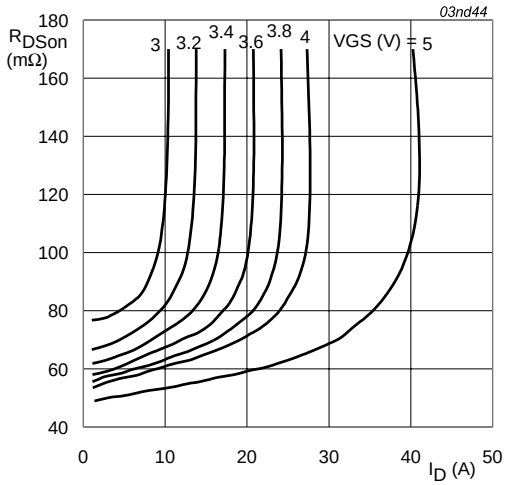
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



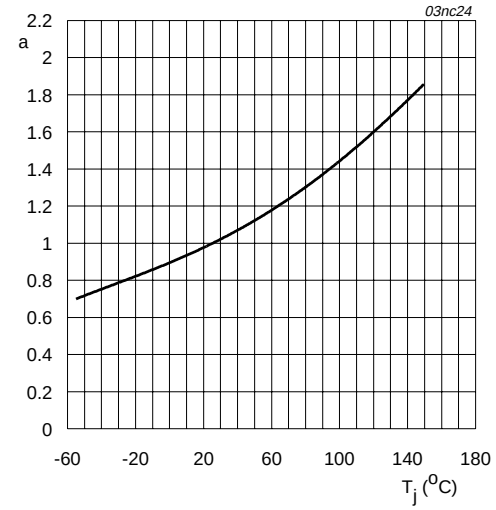
T_j = 25 °C; I_D = 10 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



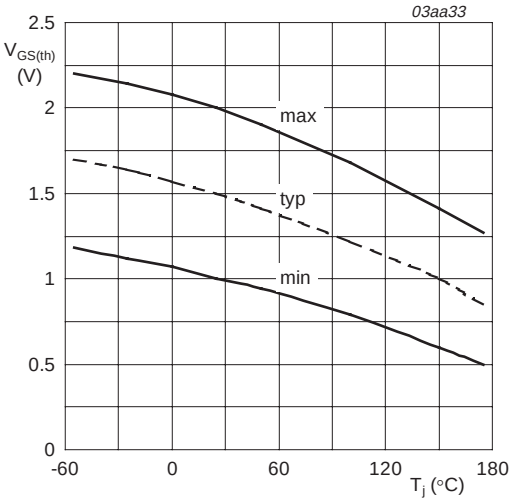
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



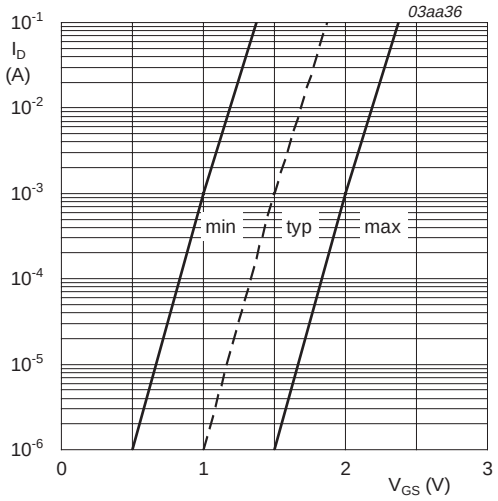
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



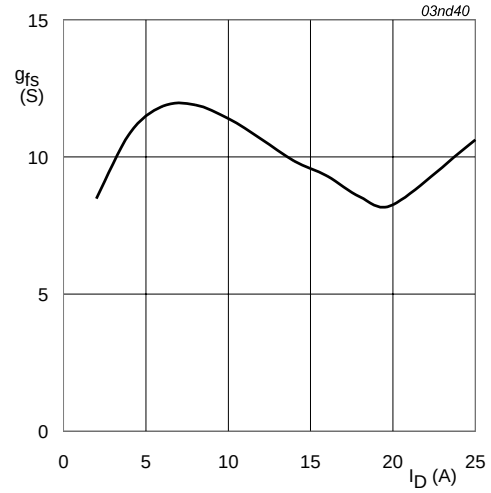
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



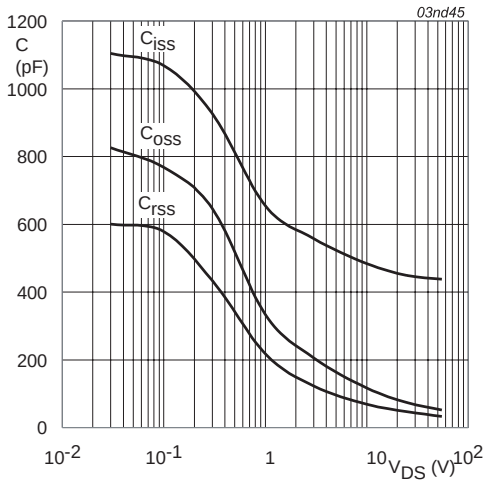
T_j = 25 °C; V_{DS} = V_{GS}

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



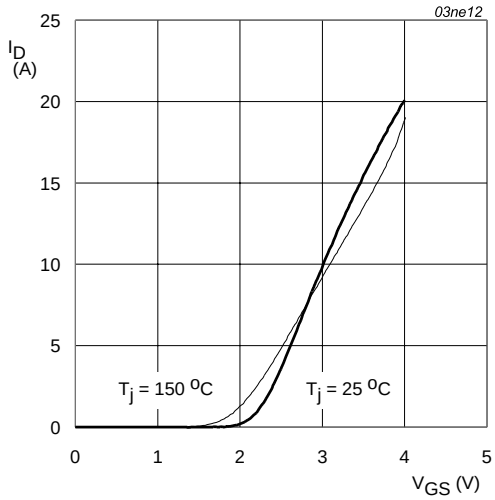
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values.



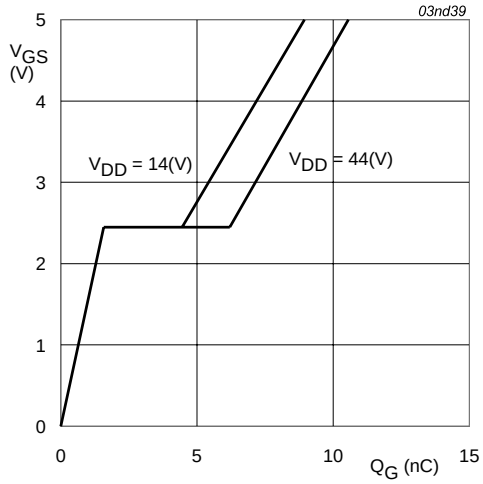
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



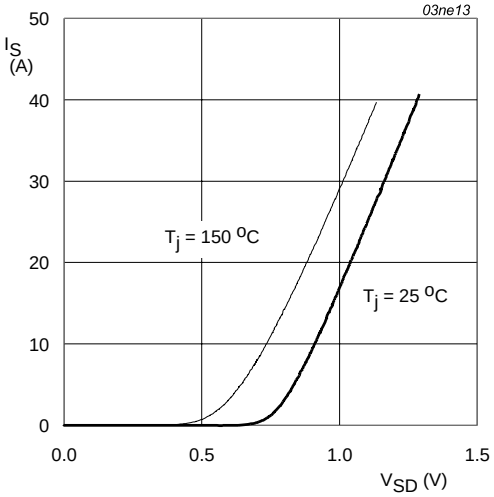
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



T_j = 25 °C; I_D = 10 A

Fig 14. Gate-source voltage as a function of gate charge; typical values.

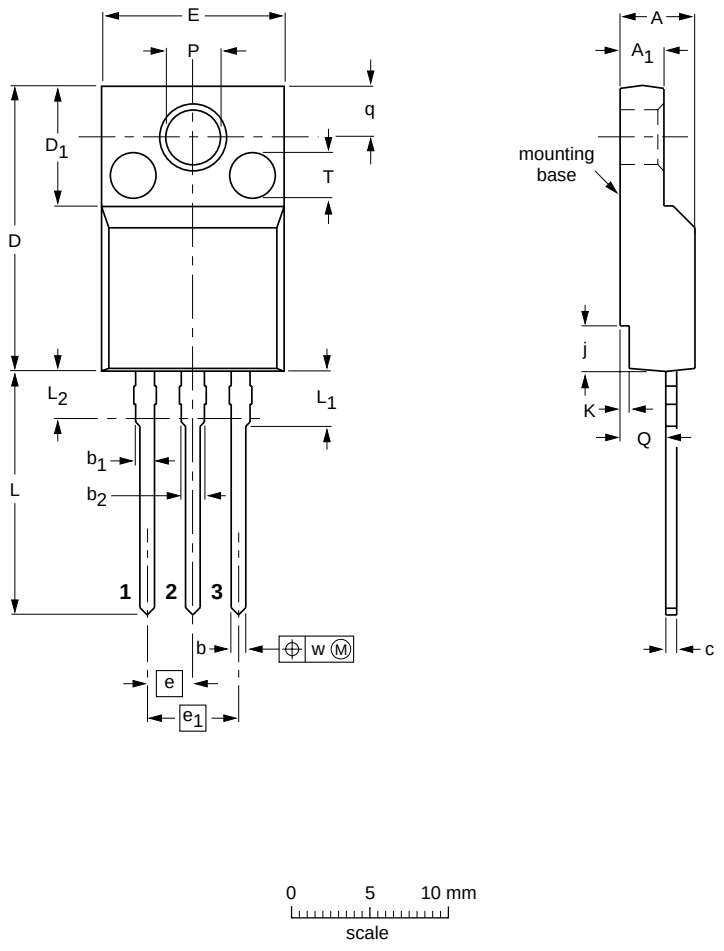


V_{GS} = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

9. Package outline

**Plastic single-ended package; isolated heatsink mounted;
1 mounting hole; 3 lead TO-220 'full pack'** **SOT186A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T(2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-03-12~~ 02-04-09

Fig 16. SOT186A.

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20040610	-	**Product data (9397 750 13328)** **Modifications:** • Latest version of package outline imported into data sheet.
01	20010215	-	**Product specification (9397 750 07997)**

11. Data sheet status

Level	Data sheet status[1]	Product status[2][3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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9397 750 13328

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Date of release: 10 June 2004 **Document order number: 9397 750 13328**

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