

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4066B

gates

Quadruple bilateral switches

Product specification
File under Integrated Circuits, IC04

January 1995

Quadruple bilateral switches

HEF4066B gates

DESCRIPTION

The HEF4066B has four independent bilateral analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). When E is connected to V_{DD} a low impedance bidirectional path between Y and Z is established (ON condition). When E is connected to V_{SS} the switch is

disabled and a high impedance between Y and Z is established (OFF condition).

The HEF4066B is pin compatible with the HEF4016B but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.

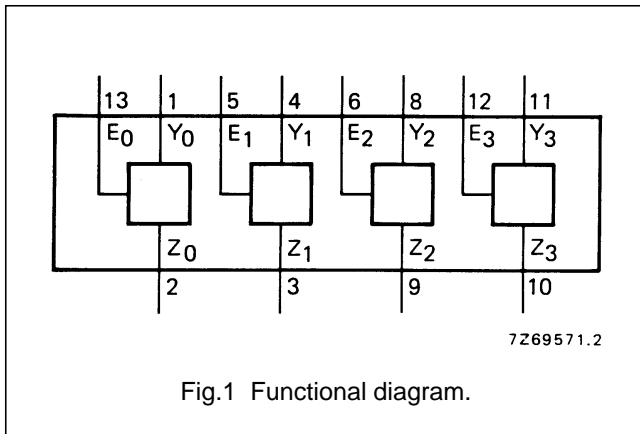


Fig.1 Functional diagram.

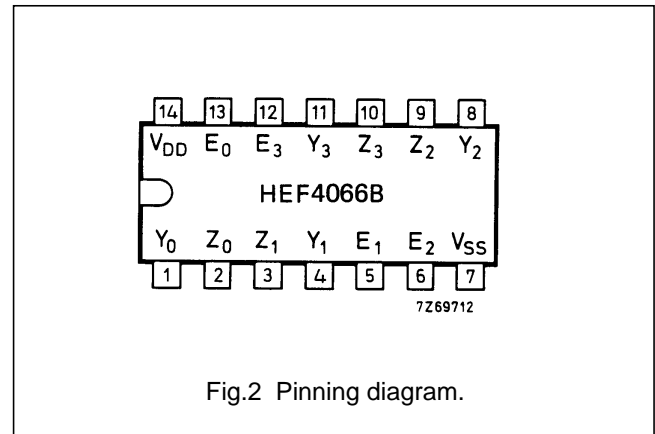


Fig.2 Pinning diagram.

- HEF4066BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4066BD(F): 14-lead DIL; ceramic (cerdip (SOT73))
- HEF4066BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America

PINNING

- E_0 to E_3 enable inputs
- Y_0 to Y_3 input/output terminals
- Z_0 to Z_3 input/output terminals

APPLICATION INFORMATION

An example of application for the HEF4066B is:

- Analogue and digital switching

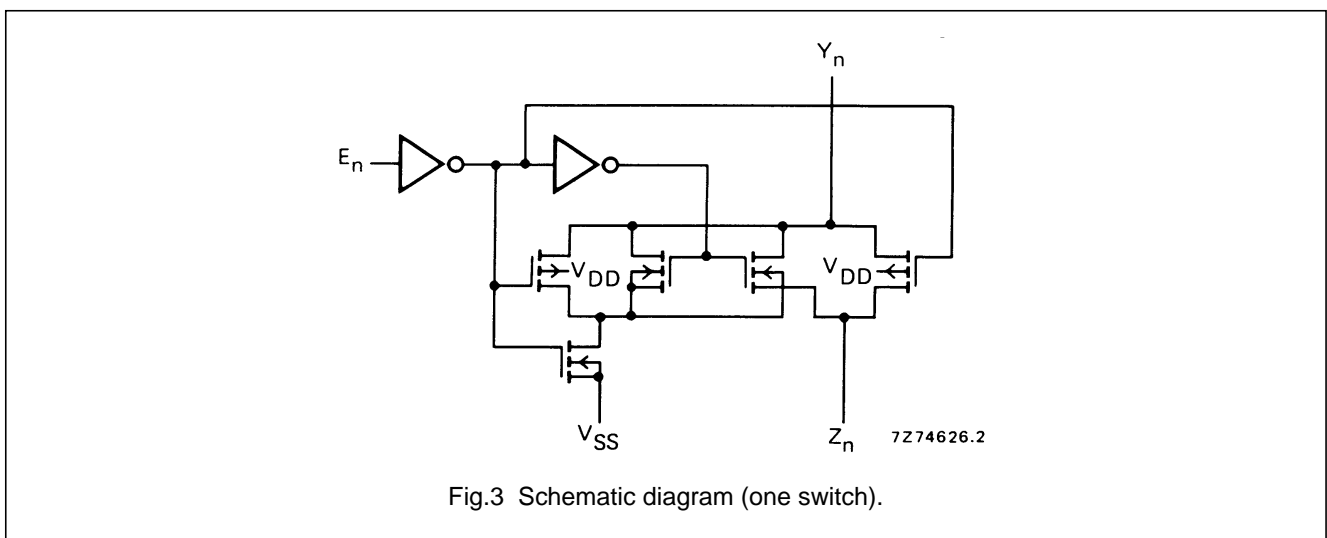


Fig.3 Schematic diagram (one switch).

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Power dissipation per switch

P max. 100 mW

For other RATINGS see Family Specifications

DC CHARACTERISTICS

T_{amb} = 25 °C

	V _{DD} V	SYMBOL	MIN. TYP. MAX.			CONDITIONS
ON resistance	5	R _{ON}	–	350	2500	E _n at V _{DD} V _{is} = V _{SS} to V _{DD} see Fig.4
	10		–	80	245	
	15		–	60	175	
ON resistance	5	R _{ON}	–	115	340	E _n at V _{DD} V _{is} = V _{SS} see Fig.4
	10		–	50	160	
	15		–	40	115	
ON resistance	5	R _{ON}	–	120	365	E _n at V _{DD} V _{is} = V _{DD} see Fig.4
	10		–	65	200	
	15		–	50	155	
'Δ' ON resistance between any two channels	5	ΔR _{ON}	–	25	–	E _n at V _{DD} V _{is} = V _{SS} to V _{DD} see Fig.4
	10		–	10	–	
	15		–	5	–	
OFF state leakage current, any channel OFF	5	I _{OZ}	–	–	–	E _n at V _{SS}
	10		–	–	–	
	15		–	–	200	
E _n input voltage LOW	5	V _{IL}	–	2,25	1	I _{is} = 10 μA see Fig.9
	10		–	4,50	2	
	15		–	6,75	2	

	V _{DD} V	SYMBOL	T _{amb} (°C)			CONDITIONS
			–40	+25	+85	
			MAX.	MAX.	MAX.	
Quiescent device current	5	I _{DD}	1,0	1,0	7,5	V _{SS} = 0; all valid input combinations; V _I = V _{SS} or V _{DD}
	10		2,0	2,0	15,0	
	15		4,0	4,0	30,0	
Input leakage current at E _n	15	± I _{IN}	–	300	1000	E _n at V _{SS} or V _{DD}

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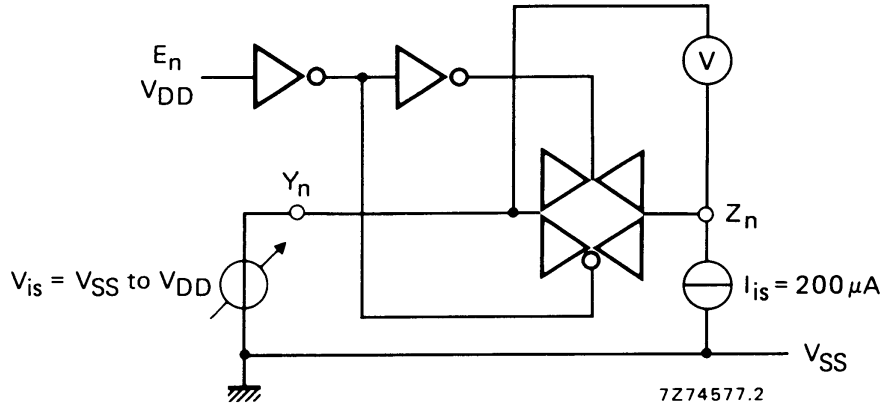
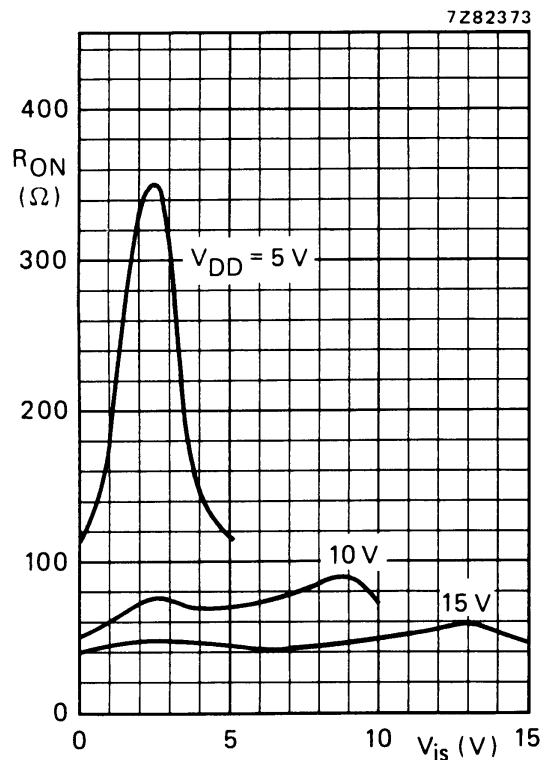


Fig.4 Test set-up for measuring R_{ON} .



E_n at V_{DD}
 $I_{is} = 200 \mu A$
 $V_{SS} = 0 V$

Fig.5 Typical R_{ON} as a function of input voltage.

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y, in this case there is no limit for the voltage drop across the switch, but the voltages at Y and Z may not exceed V_{DD} or V_{SS} .

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AC CHARACTERISTICS ^{(1), (2)}

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	TYP.	MAX.			
Propagation delays $V_{is} \rightarrow V_{os}$ HIGH to LOW	5	t_{PHL}	10	20	ns	note 3	
	10		5	10	ns		
	15		5	10	ns		
	LOW to HIGH	5	t_{PLH}	10	20	ns	note 3
		10		5	10	ns	
		15		5	10	ns	
Output disable times $E_n \rightarrow V_{os}$ HIGH	5	t_{PHZ}	80	160	ns	note 4	
	10		65	130	ns		
	15		60	120	ns		
	LOW	5	t_{PLZ}	80	160	ns	note 4
		10		70	140	ns	
		15		70	140	ns	
Output enable times $E_n \rightarrow V_{os}$ HIGH	5	t_{PZH}	40	80	ns	note 4	
	10		20	40	ns		
	15		15	30	ns		
	LOW	5	t_{PZL}	45	90	ns	note 4
		10		20	40	ns	
		15		15	30	ns	
Distortion, sine-wave response	5		0,25		%	note 5	
	10		0,04		%		
	15		0,04		%		
Crosstalk between any two channels	5		–		MHz	note 6	
	10		1		MHz		
	15		–		MHz		
Crosstalk; enable input to output	5		–		mV	note 7	
	10		50		mV		
	15		–		mV		
OFF-state feed-through	5		–		MHz	note 8	
	10		1		MHz		
	15		–		MHz		
ON-state frequency response	5		–		MHz	note 9	
	10		90		MHz		
	15		–		MHz		

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	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	800 f _i + ∑ (f _o C _L) × V _{DD} ² 3 500 f _i + ∑ (f _o C _L) × V _{DD} ² 10 100 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

Notes

- V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
- V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.
- R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; E_n = V_{DD}; V_{is} = V_{DD} (square-wave); see Figs 6 and 10.
- R_L = 10 kΩ; C_L = 50 pF to V_{SS}; E_n = V_{DD} (square-wave);
V_{is} = V_{DD} and R_L to V_{SS} for t_{PHZ} and t_{PZH};
V_{is} = V_{SS} and R_L to V_{DD} for t_{PLZ} and t_{PZL}; see Figs 6 and 11.
- R_L = 10 kΩ; C_L = 15 pF; E_n = V_{DD}; V_{is} = 1/2 V_{DD(p-p)} (sine-wave, symmetrical about 1/2 V_{DD}); f_{is} = 1 kHz; see Fig.7.
- R_L = 1 kΩ; V_{is} = 1/2 V_{DD(p-p)} (sine-wave, symmetrical about 1/2 V_{DD});

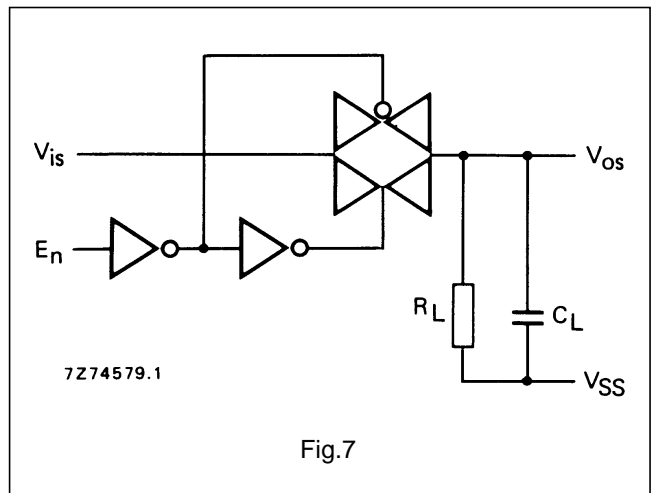
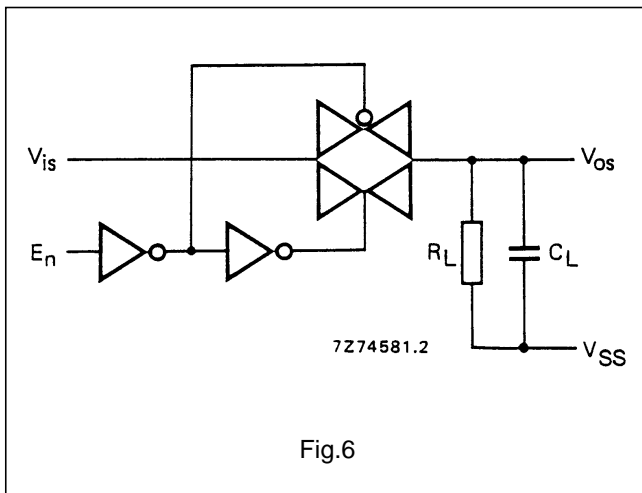
$$20 \log \frac{V_{os}(B)}{V_{is}(A)} = -50 \text{ dB}; E_n(A) = V_{SS}; E_n(B) = V_{DD}; \text{ see Fig. 8.}$$

- R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; E_n = V_{DD} (square-wave); crosstalk is |V_{os}| (peak value); see Fig.6.
- R_L = 1 kΩ; C_L = 5 pF; E_n = V_{SS}; V_{is} = 1/2 V_{DD(p-p)} (sine-wave, symmetrical about 1/2 V_{DD});

$$20 \log \frac{V_{os}}{V_{is}} = -50 \text{ dB}; \text{ see Fig. 7.}$$

- R_L = 1 kΩ; C_L = 5 pF; E_n = V_{DD}; V_{is} = 1/2 V_{DD(p-p)} (sine-wave, symmetrical about 1/2 V_{DD});

$$20 \log \frac{V_{os}}{V_{is}} = -3 \text{ dB}; \text{ see Fig. 7.}$$



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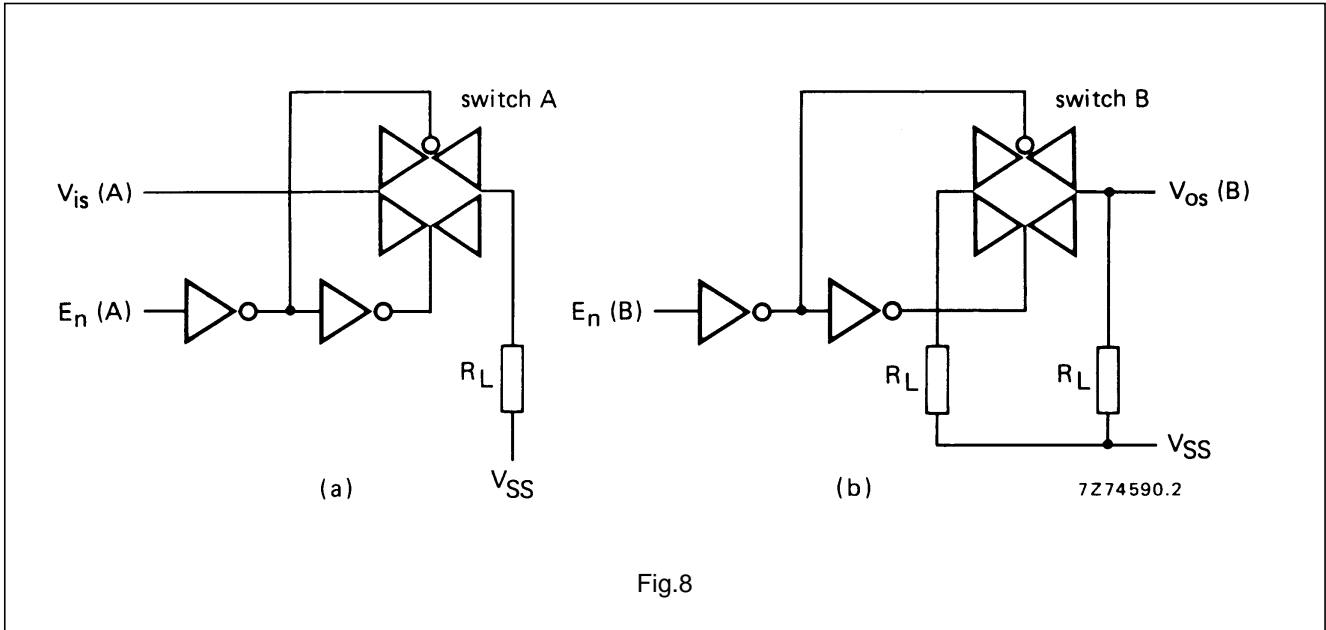


Fig.8

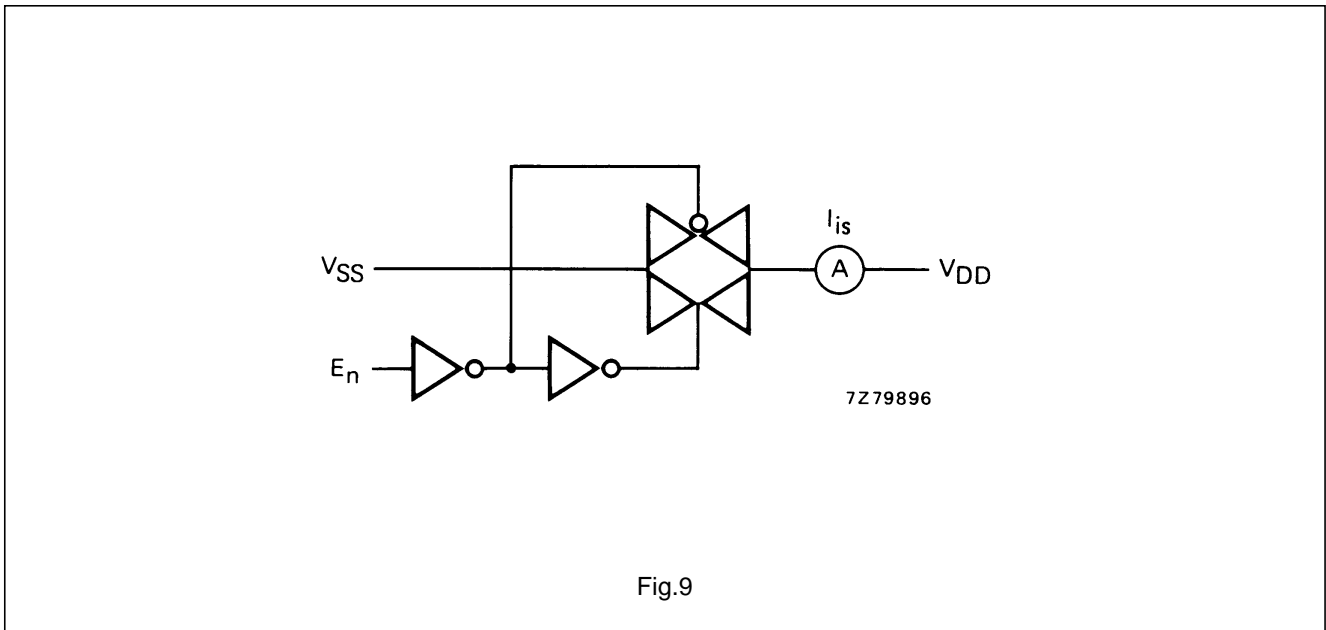


Fig.9

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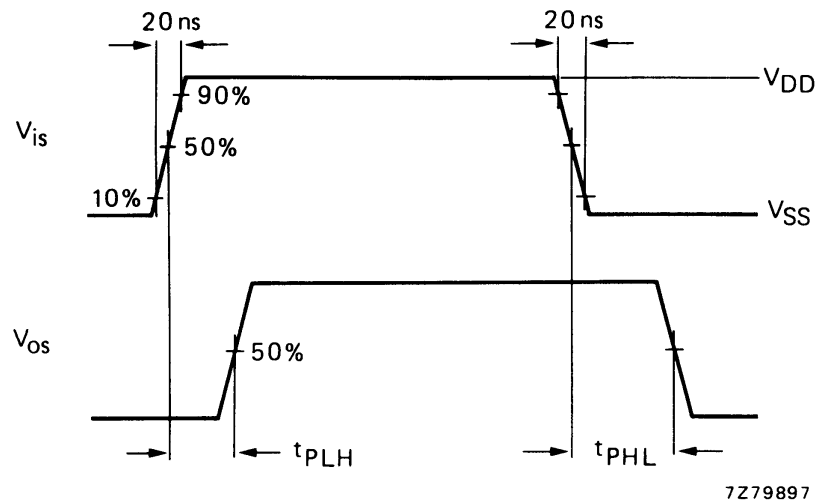
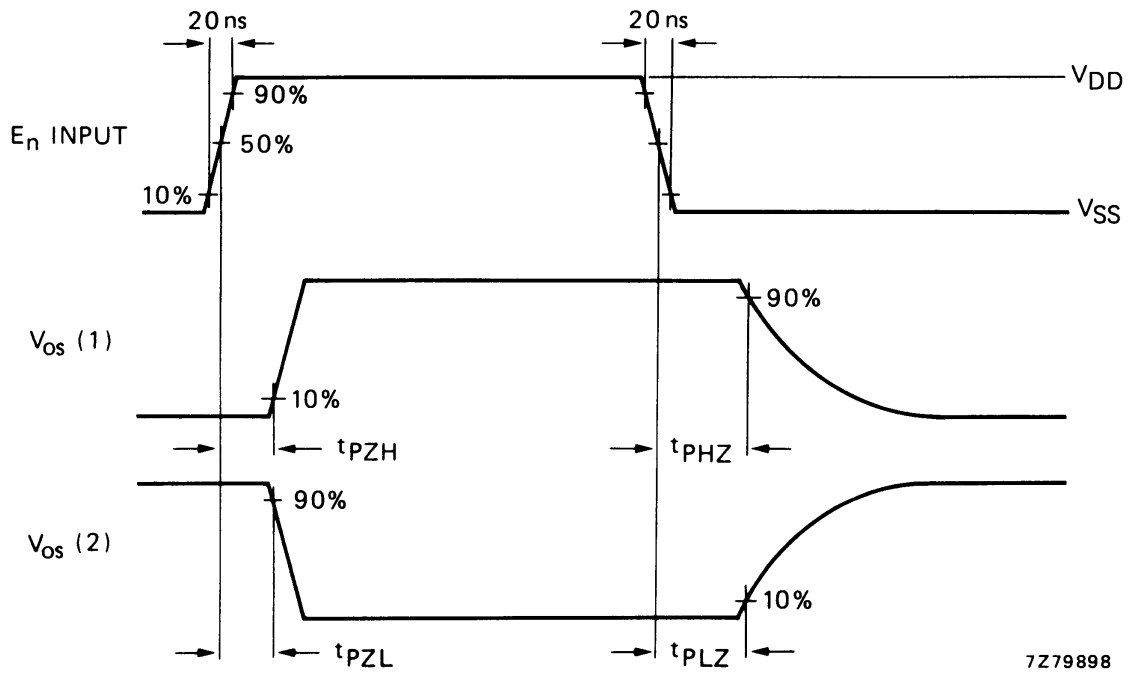


Fig.10 Waveforms showing propagation delays from V_{is} to V_{os} .



- (1) V_{is} at V_{DD}
- (2) V_{is} at V_{SS}

Fig.11 Waveforms showing output disable and enable times.