

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4516B

MSI

Binary up/down counter

Product specification
File under Integrated Circuits, IC04

January 1995

Binary up/down counter

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DESCRIPTION

The HEF4516B is an edge-triggered synchronous up/down 4-bit binary counter with a clock input (CP), an up/down count control input (UP/DN), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR which must be LOW. When PL and $\overline{CE}$ are LOW, the counter changes on the LOW to HIGH transition of CP. Input UP/DN determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, $\overline{TC}$ is LOW when O_0 and O_3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when O_0 to O_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (O_0 to $O_3 = \text{LOW}$) independent of all other input conditions.

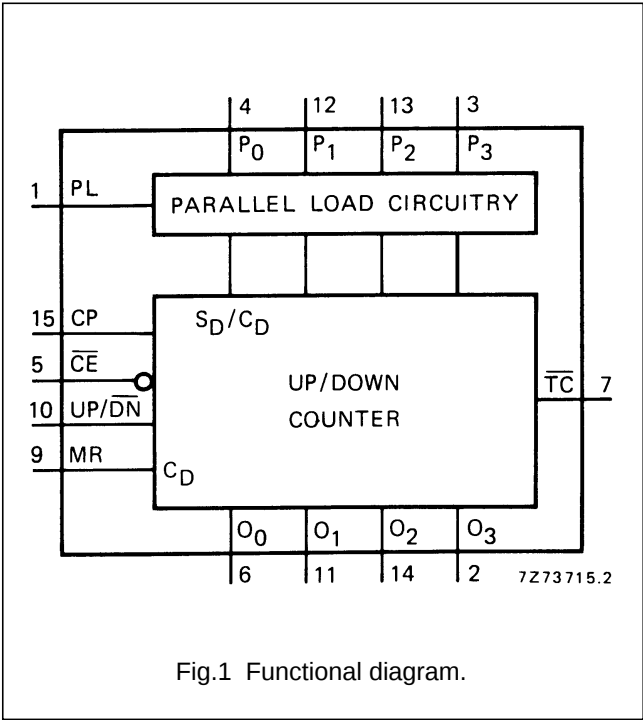


Fig.1 Functional diagram.

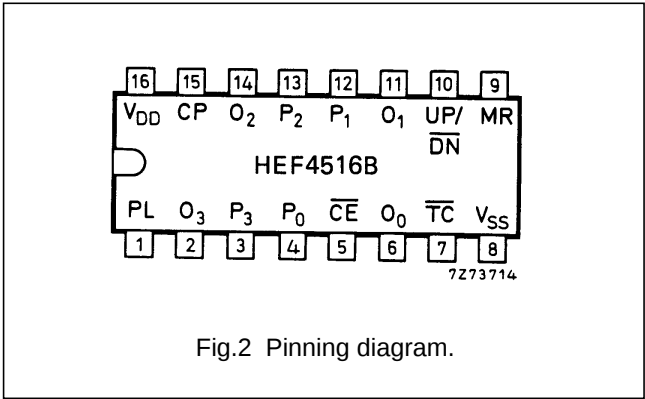


Fig.2 Pinning diagram.

PINNING

- PL parallel load input (active HIGH)
- P_0 to P_3 parallel inputs
- $\overline{CE}$ count enable input (active LOW)
- CP clock pulse input (LOW to HIGH, edge triggered)
- UP/DN up/down count control input
- MR master reset input
- $\overline{TC}$ terminal count output (active LOW)
- O_0 to O_3 parallel outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

- HEF4516BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4516BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4516BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

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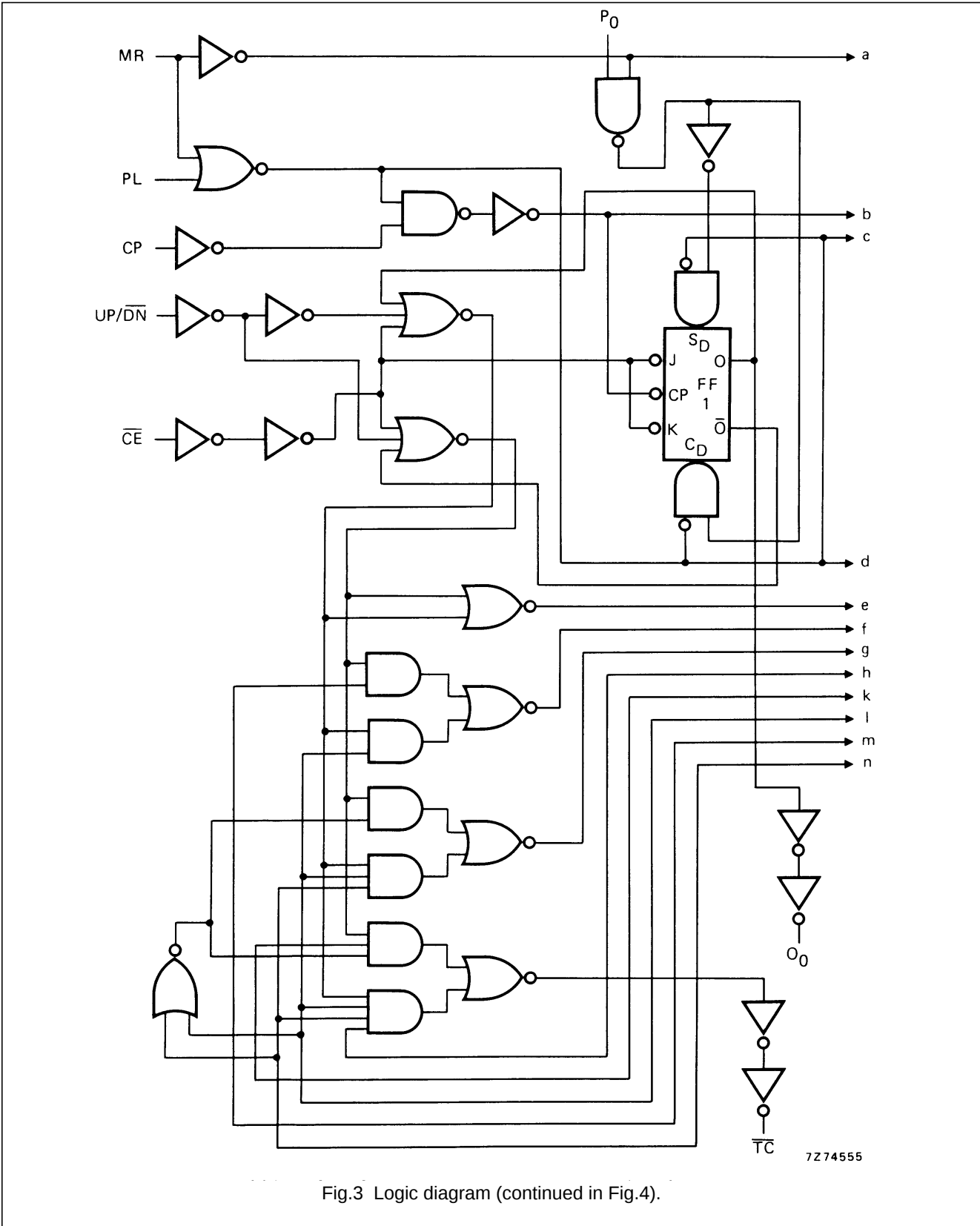
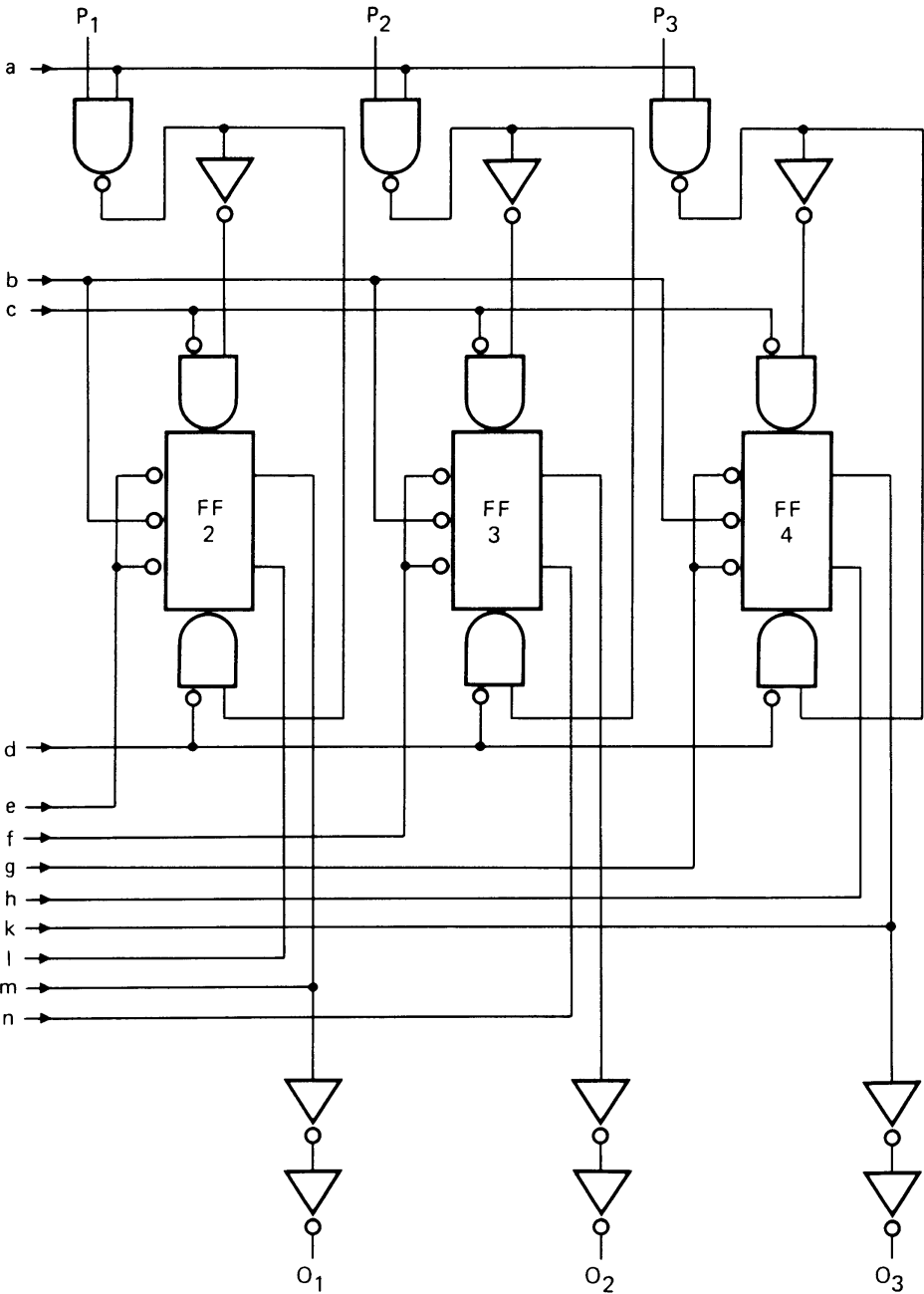


Fig.3 Logic diagram (continued in Fig.4).

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Fig.4 Logic diagram (continued from Fig.3).

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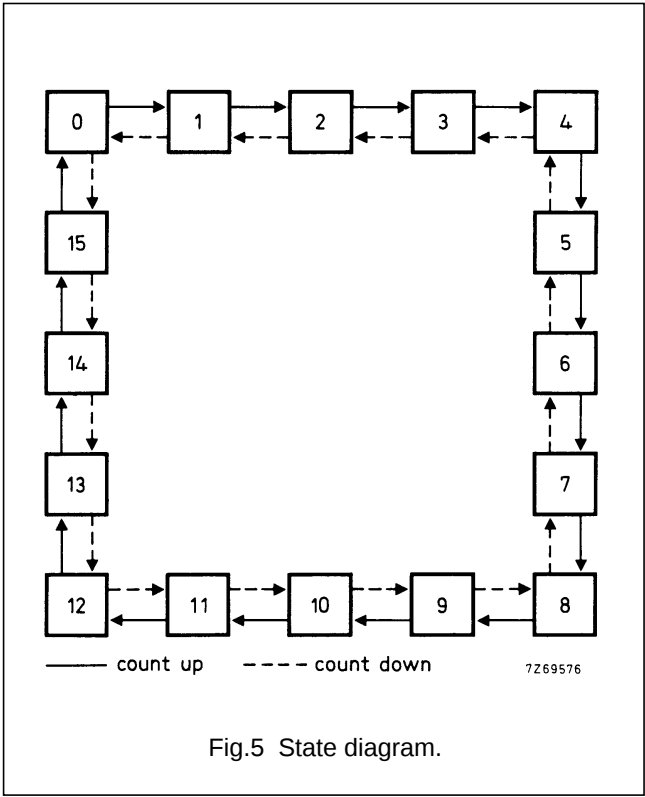
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FUNCTION TABLE

MR	PL	UP/DN	CE	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L		count down
L	L	H	L		count up
H	X	X	X	X	reset

Notes

1.
- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
 = positive-going transition



Logic equation for terminal count:

$$\overline{TC} = \overline{CE} \cdot \{ (UP/DN) \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3 + (\overline{UP/DN}) \cdot \overline{O_0} \cdot \overline{O_1} \cdot \overline{O_2} \cdot \overline{O_3} \}$$

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	1000 f _i + ∑ (f _o C _L) × V _{DD} ² 4500 f _i + ∑ (f _o C _L) × V _{DD} ² 11 200 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

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AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
CP $\rightarrow$ O _n	5			145	290 ns	118 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C _L
	15			45	90 ns	37 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		155	310 ns	128 ns + (0,55 ns/pF) C _L
	10			65	130 ns	54 ns + (0,23 ns/pF) C _L
	15			45	90 ns	37 ns + (0,16 ns/pF) C _L
CP $\rightarrow$ $\overline{TC}$	5			260	525 ns	233 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		105	210 ns	94 ns + (0,23 ns/pF) C _L
	15			75	150 ns	67 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		180	360 ns	153 ns + (0,55 ns/pF) C _L
	10			75	150 ns	64 ns + (0,23 ns/pF) C _L
	15			55	115 ns	47 ns + (0,16 ns/pF) C _L
PL $\rightarrow$ O _n	5			125	255 ns	98 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C _L
	15			40	85 ns	32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		170	340 ns	143 ns + (0,55 ns/pF) C _L
	10			70	140 ns	59 ns + (0,23 ns/pF) C _L
	15			50	105 ns	42 ns + (0,16 ns/pF) C _L
PL $\rightarrow$ $\overline{TC}$	5			250	500 ns	223 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		110	220 ns	99 ns + (0,23 ns/pF) C _L
	15			80	160 ns	72 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		250	500 ns	223 ns + (0,55 ns/pF) C _L
	10			110	220 ns	99 ns + (0,23 ns/pF) C _L
	15			80	160 ns	72 ns + (0,16 ns/pF) C _L
$\overline{CE} \rightarrow \overline{TC}$	5			165	330 ns	138 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		65	135 ns	54 ns + (0,23 ns/pF) C _L
	15			50	100 ns	42 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}		145	290 ns	118 ns + (0,55 ns/pF) C _L
	10			60	125 ns	49 ns + (0,23 ns/pF) C _L
	15			45	95 ns	37 ns + (0,16 ns/pF) C _L
MR $\rightarrow$ O _n , $\overline{TC}$	5			205	405 ns	178 ns + (0,55 ns/pF) C _L
HIGH to LOW	10	t _{PHL}		65	130 ns	54 ns + (0,23 ns/pF) C _L
	15			45	85 ns	37 ns + (0,16 ns/pF) C _L
MR $\rightarrow$ $\overline{TC}$	5			225	450 ns	198 ns + (0,55 ns/pF) C _L
LOW to HIGH	10	t _{PLH}		75	150 ns	64 ns + (0,23 ns/pF) C _L
	15			50	100 ns	42 ns + (0,16 ns/pF) C _L

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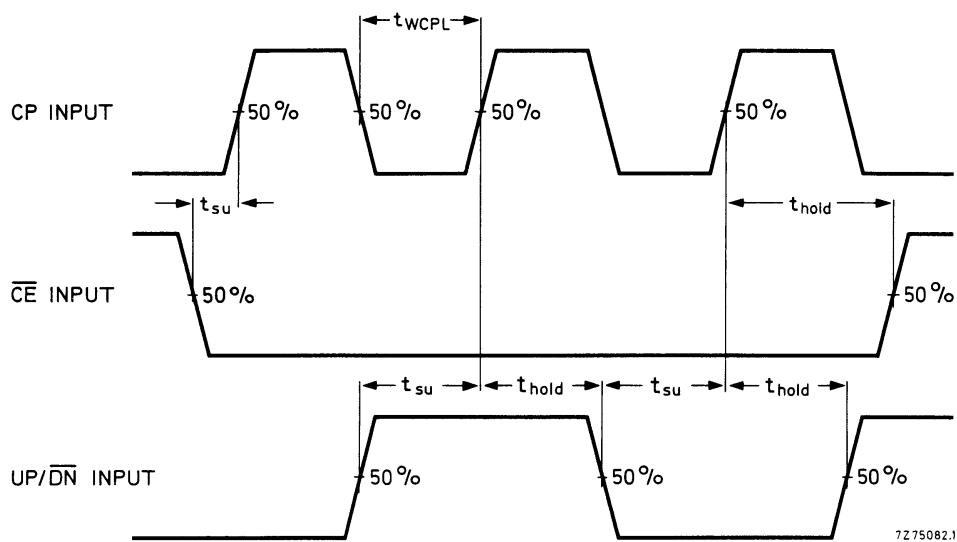
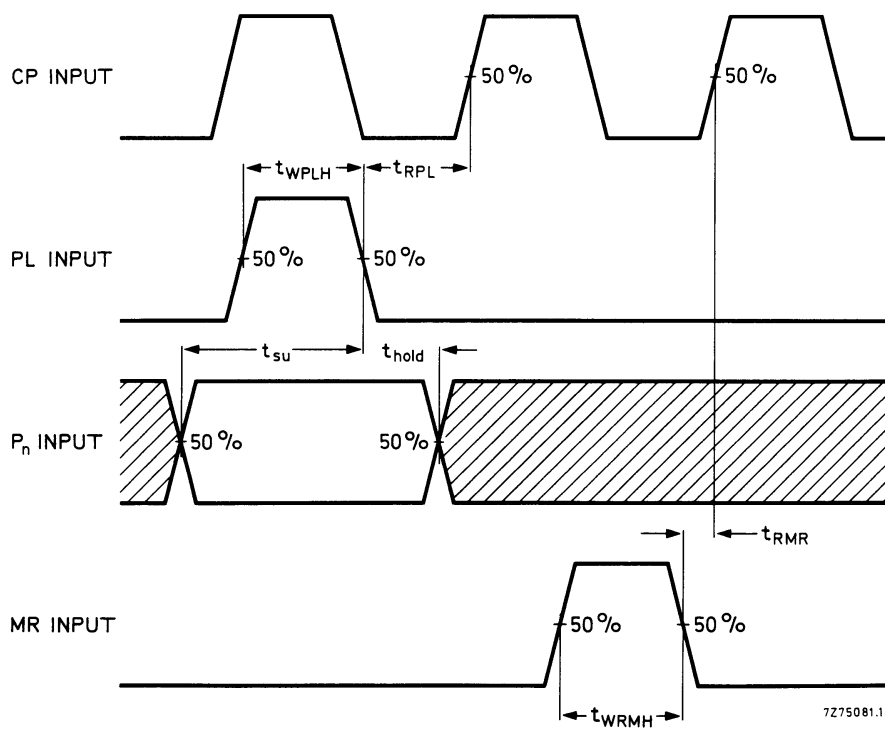
	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Output transition times HIGH to LOW	5	t_{THL}		60	120 ns	10 ns + (1,0 ns/pF) C_L
	10			30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5	t_{TLH}		60	120 ns	10 ns + (1,0 ns/pF) C_L
	10			30	60 ns	9 ns + (0,42 ns/pF) C_L
	15			20	40 ns	6 ns + (0,28 ns/pF) C_L

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum clock pulse width; LOW	5	t _{WCPL}	95	45	ns	see also waveforms Figs 6 and 7
	10		35	20	ns	
	15		25	15	ns	
Minimum PL pulse width; HIGH	5	t _{WPLH}	105	55	ns	
	10		45	25	ns	
	15		35	15	ns	
Minimum MR pulse width; HIGH	5	t _{WMRH}	120	60	ns	
	10		50	25	ns	
	15		40	20	ns	
Recovery time for MR	5	t _{RMR}	130	65	ns	
	10		45	20	ns	
	15		30	15	ns	
Recovery time for PL	5	t _{RPL}	150	75	ns	
	10		50	25	ns	
	15		30	15	ns	
Set-up times P _n → PL UP/ $\overline{\text{DN}}$ → CP $\overline{\text{CE}}$ → CP	5	t _{su}	100	50	ns	
	10		50	25	ns	
	15		40	20	ns	
	5	t _{su}	250	125	ns	
	10		100	50	ns	
	15		75	35	ns	
	5	t _{su}	120	60	ns	
	10		40	20	ns	
	15		25	10	ns	
Hold times P _n → PL UP/ $\overline{\text{DN}}$ → CP $\overline{\text{CE}}$ → CP	5	t _{hold}	10	−40	ns	
	10		5	−20	ns	
	15		0	−20	ns	
	5	t _{hold}	35	−90	ns	
	10		15	−35	ns	
	15		15	−25	ns	
	5	t _{hold}	20	−40	ns	
	10		5	−15	ns	
	15		5	−10	ns	
Maximum clock pulse frequency	5	f _{max}	3	6	MHz	
	10		7	14	MHz	
	15		9	18	MHz	

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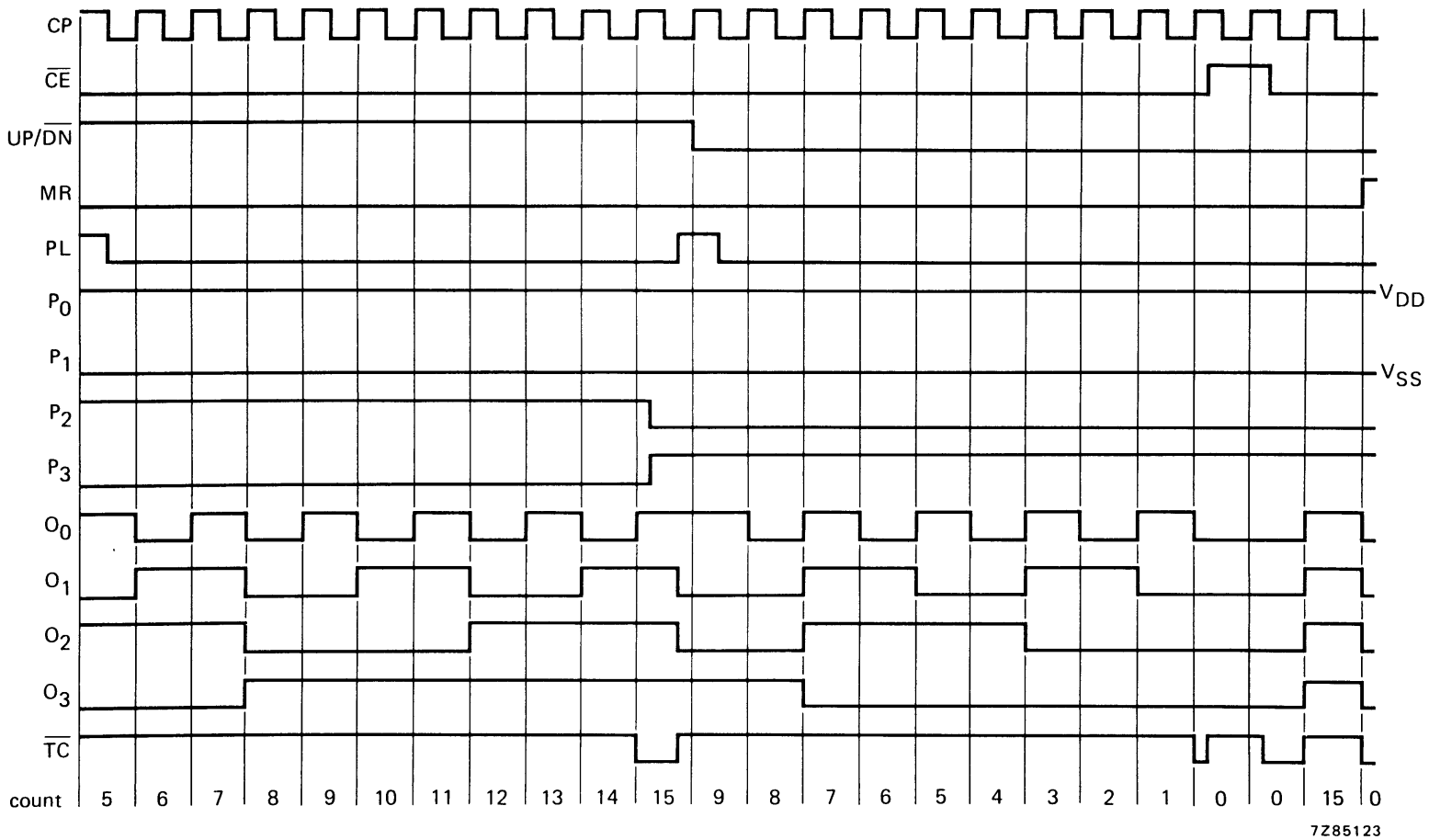


Fig.8 Timing diagram.