

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF40106B

### gates

### Hex inverting Schmitt trigger

Product specification  
File under Integrated Circuits, IC04

January 1995

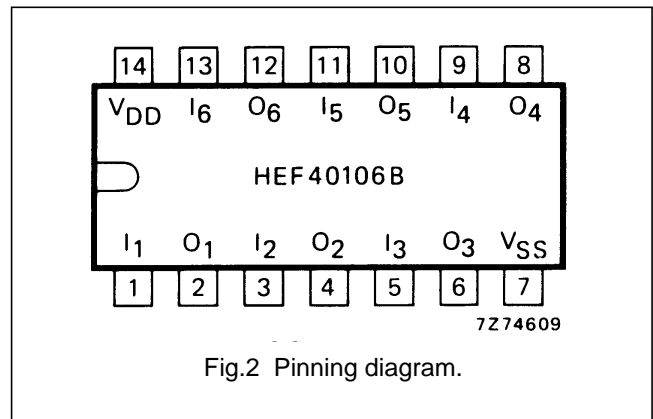
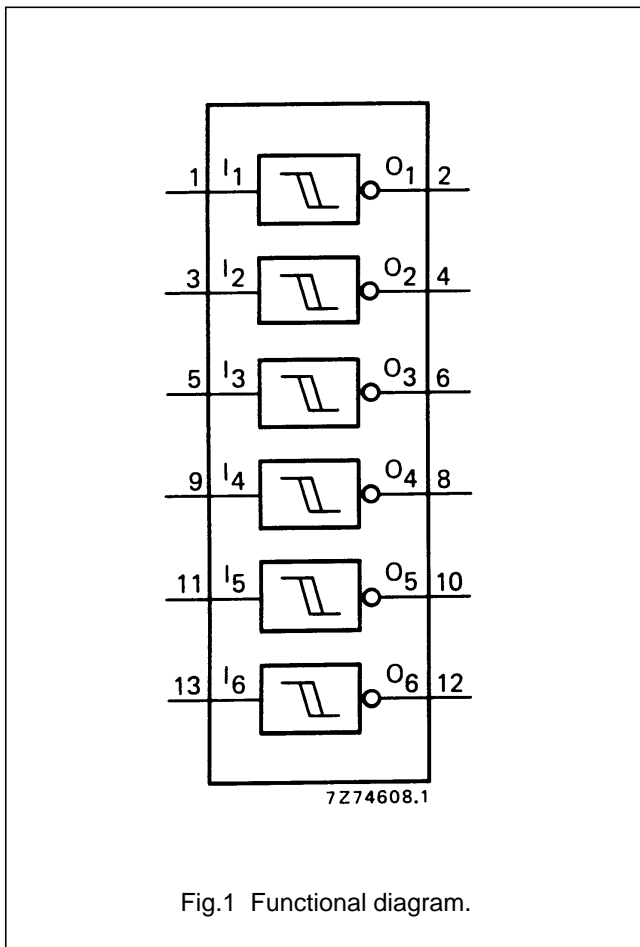
# Hex inverting Schmitt trigger

# HEF40106B gates

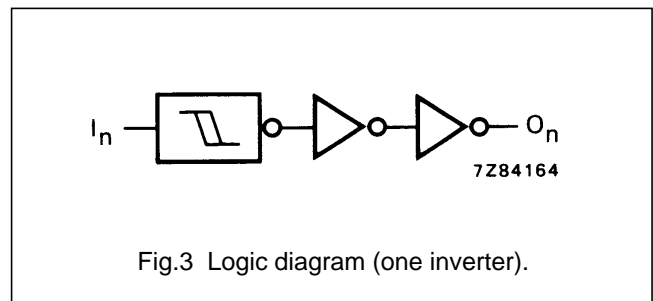
### DESCRIPTION

Each circuit of the HEF40106B functions as an inverter with Schmitt-trigger action. The Schmitt-trigger switches at different points for the positive and negative-going input signals. The difference between the positive-going voltage ( $V_P$ ) and the negative-going voltage ( $V_N$ ) is defined as hysteresis voltage ( $V_H$ ).

This device may be used for enhanced noise immunity or to "square up" slowly changing waveforms.



- HEF40106BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF40106BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF40106BT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America



### FAMILY DATA, I<sub>DD</sub> LIMITS category GATES

See Family Specifications

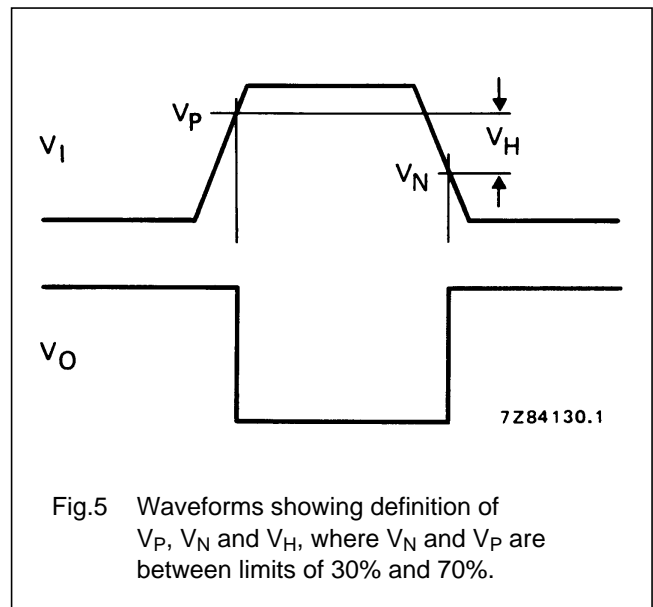
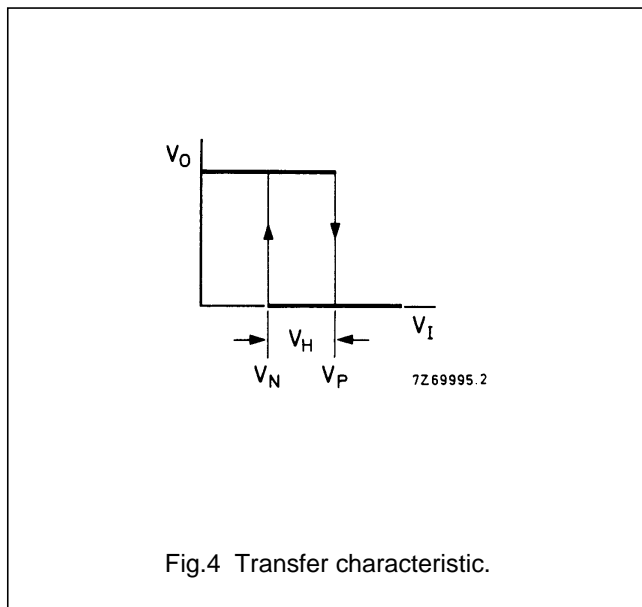
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**DC CHARACTERISTICS**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	
Hysteresis voltage	5	$V_H$	0,5	0,8		V
	10		0,7	1,3		V
	15		0,9	1,8		V
Switching levels positive-going input voltage	5	$V_P$	2	3,0	3,5	V
	10		3,7	5,8	7	V
	15		4,9	8,3	11	V
negative-going input voltage	5	$V_N$	1,5	2,2	3	V
	10		3	4,5	6,3	V
	15		4	6,5	10,1	V



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	$V_{DD}$ V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	90	180	ns	63 ns + (0,55 ns/pF) $C_L$
	10		35	70	ns	24 ns + (0,23 ns/pF)
	15		30	60	ns	22 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5	$t_{PLH}$	75	150	ns	48 ns + (0,55 ns/pF) $C_L$
	10		35	70	ns	24 ns + (0,23 ns/pF) $C_L$
	15		30	60	ns	22 ns + (0,16 ns/pF) $C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120	ns	10 ns + (1,0 ns/pF) $C_L$
	10		30	60	ns	9 ns + (0,42 ns/pF) $C_L$
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$
LOW to HIGH	5	$t_{TLH}$	60	120	ns	10 ns + (1,0 ns/pF) $C_L$
	10		30	60	ns	9 ns + (0,42 ns/pF) $C_L$
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu$ W)	
Dynamic power dissipation per package (P)	5	$2\,300 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$9\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$20\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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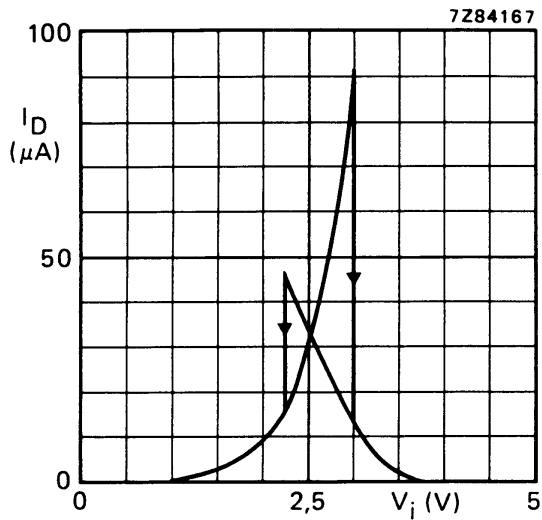


Fig.6 Typical drain current as a function of input voltage;  $V_{DD} = 5 V$ ;  $T_{amb} = 25^\circ C$ .

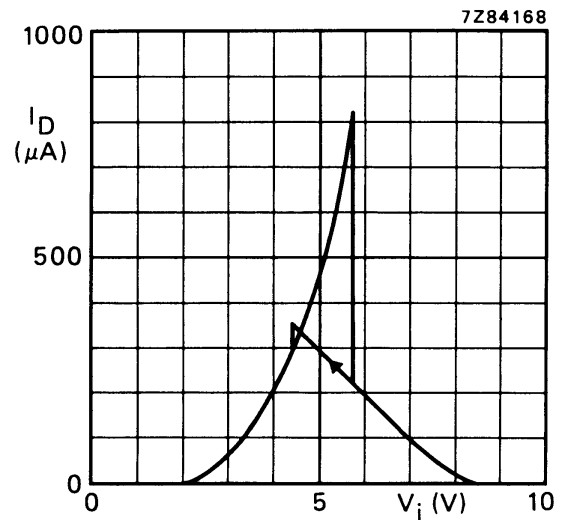


Fig.7 Typical drain current as a function of input voltage;  $V_{DD} = 10 V$ ;  $T_{amb} = 25^\circ C$ .

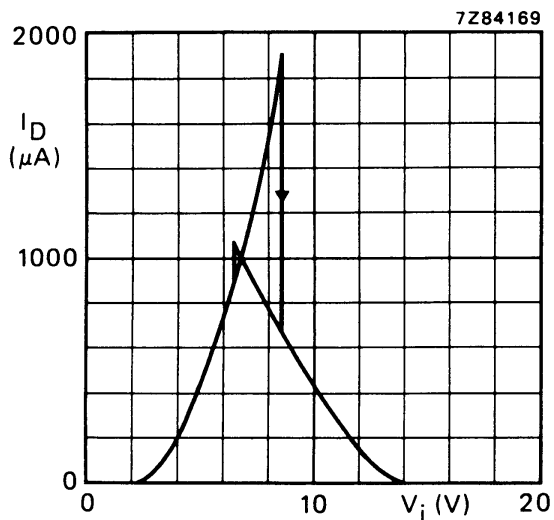


Fig.8 Typical drain current as a function of input voltage;  $V_{DD} = 15 V$ ;  $T_{amb} = 25^\circ C$ .

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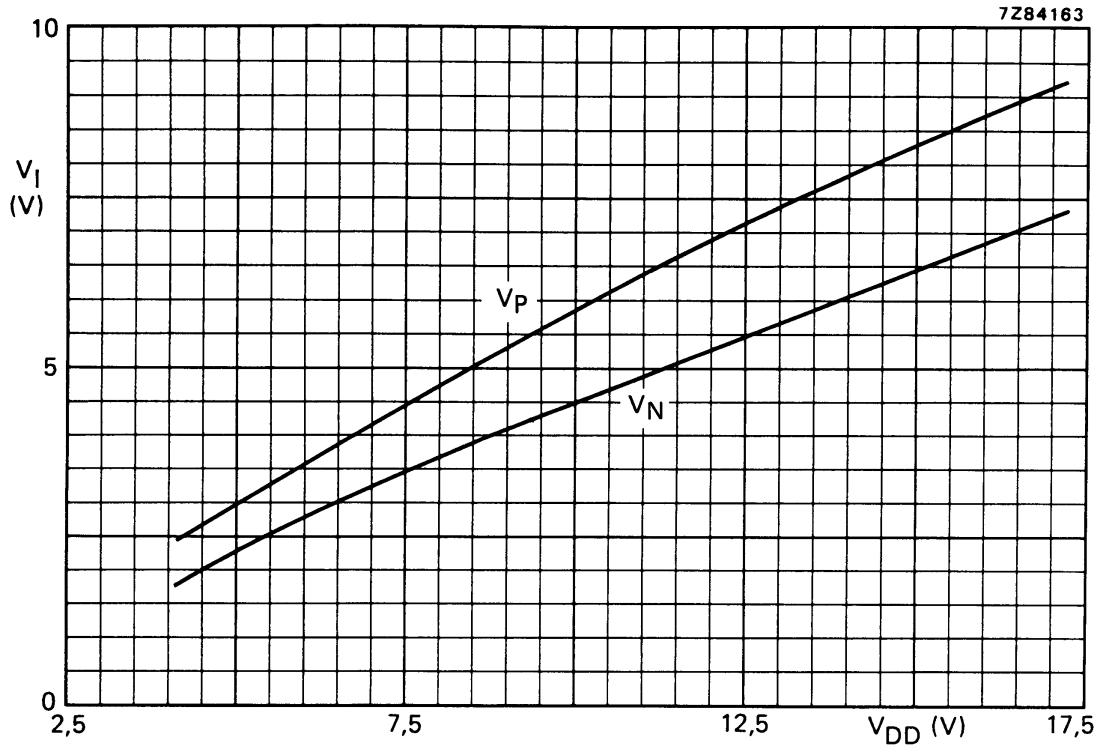


Fig.9 Typical switching levels as a function of supply voltage V<sub>DD</sub>; T<sub>amb</sub> = 25 °C.

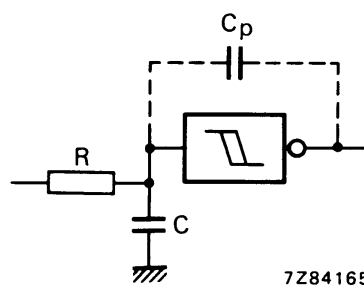


Fig.10 Schmitt trigger driven via a high impedance (R > 1 kΩ).

If a Schmitt trigger is driven via a high impedance (R > 1 kΩ) then it is necessary to incorporate a capacitor C of such value that:  $\frac{C}{C_p} > \frac{V_{DD} - V_{SS}}{V_H}$ , otherwise oscillation can occur on the edges of a pulse.

C<sub>p</sub> is the external parasitic capacitance between input and output; the value depends on the circuit board layout.

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### APPLICATION INFORMATION

Some examples of applications for the HEF40106B are:

- Wave and pulse shapers
- Astable multivibrators
- Monostable multivibrators.

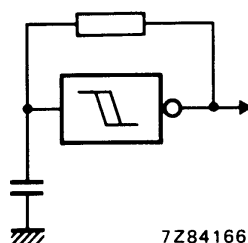


Fig.11 The HEF40106B used as an astable multivibrator.