

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4013B **flip-flops** Dual D-type flip-flop

Product specification
File under Integrated Circuits, IC04

January 1995

Dual D-type flip-flop

HEF4013B flip-flops

DESCRIPTION

The HEF4013B is a dual D-type flip-flop which features independent set direct (S_D), clear direct (C_D), clock inputs (CP) and outputs (O, \bar{O}). Data is accepted when CP is LOW and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the D or CP inputs. The outputs are buffered for best system performance. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

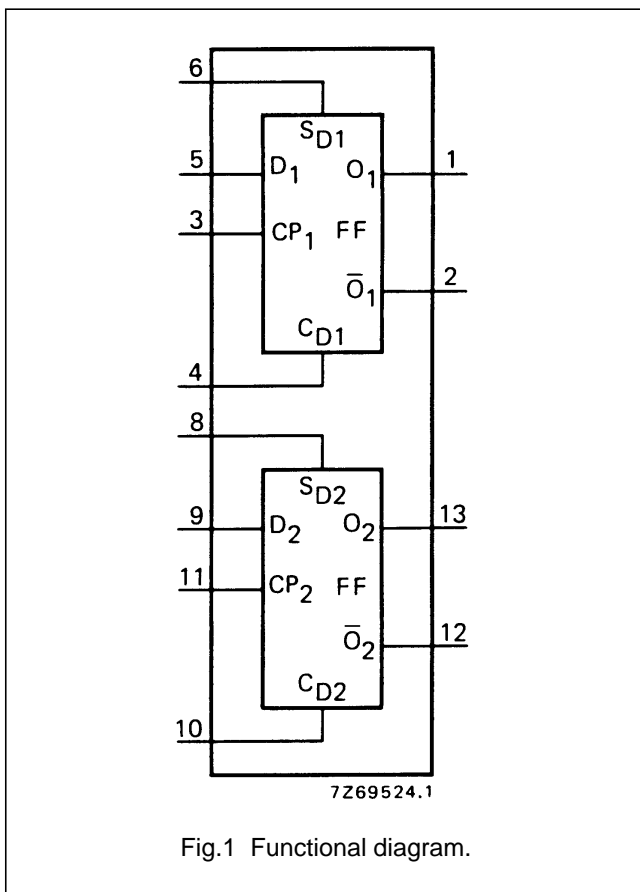


Fig.1 Functional diagram.

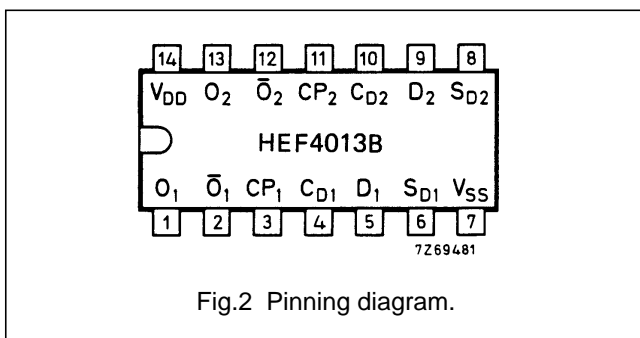


Fig.2 Pinning diagram.

FUNCTION TABLES

INPUTS				OUTPUTS	
S_D	C_D	CP	D	O	\bar{O}
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H

INPUTS				OUTPUTS	
S_D	C_D	CP	D	O_{n+1}	\bar{O}_{n+1}
L	L		L	L	H
L	L		H	H	L

Notes

- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
 = positive-going transition
 O_{n+1} = state after clock positive transition

PINNING

- D data inputs
- CP clock input (L to H edge-triggered)
- S_D asynchronous set-direct input (active HIGH)
- C_D asynchronous clear-direct input (active HIGH)
- O true output
- \bar{O} complement output

HEF4013BP(N): 14-lead DIL; plastic (SOT27-1)

HEF4013BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

HEF4013BT(D): 14-lead SO; plastic (SOT108-1)

(): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category FLIP-FLOPS

See Family Specifications

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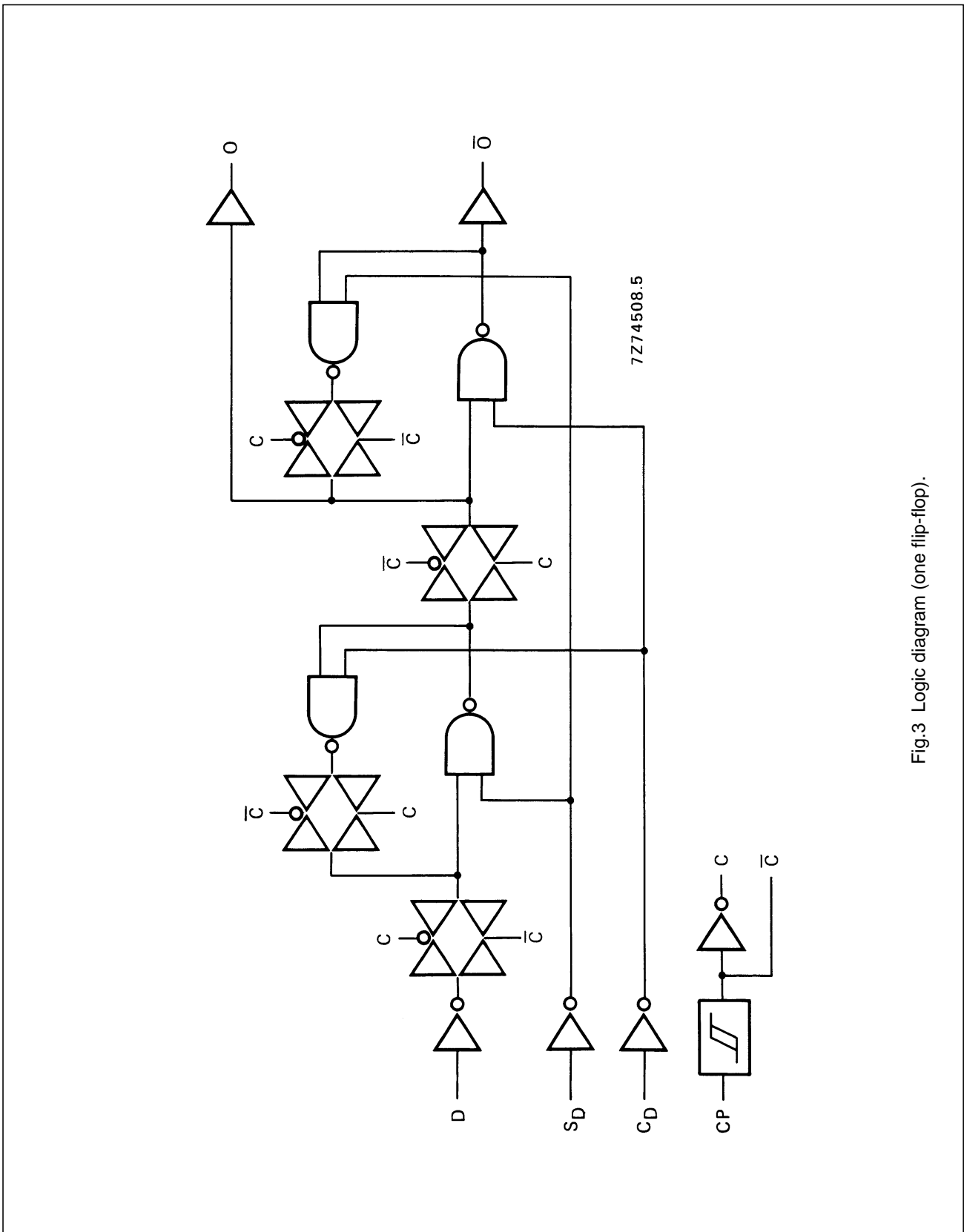


Fig.3 Logic diagram (one flip-flop).

Dual D-type flip-flop

HEF4013B
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	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $CP \rightarrow O, \bar{O}$ HIGH to LOW	5	t_{PHL}		110	220	ns	$83\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			45	90	ns	$34\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}		95	190	ns	$68\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$S_D \rightarrow \bar{O}$ HIGH to LOW	5	t_{PHL}		100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$S_D \rightarrow O$ LOW to HIGH	5	t_{PLH}		75	150	ns	$48\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			35	70	ns	$24\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			25	50	ns	$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
$C_D \rightarrow O$ HIGH to LOW	5	t_{PHL}		100	200	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$C_D \rightarrow \bar{O}$ LOW to HIGH	5	t_{PLH}		60	120	ns	$33\text{ ns} + (0,55\text{ ns/pF}) C_L$
	10			30	60	ns	$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			20	40	ns	$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}		60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
	10			30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

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AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Set-up time D → CP	5	t_{su}	40	20	ns	see also waveforms Figs 4 and 5
	10		25	10	ns	
	15		15	5	ns	
Hold time D → CP	5	t_{hold}	20	0	ns	
	10		20	0	ns	
	15		15	0	ns	
Minimum clock pulse width; LOW	5	t_{WCPL}	60	30	ns	
	10		30	15	ns	
	15		20	10	ns	
Minimum S_D pulse width; HIGH	5	t_{WSDH}	50	25	ns	
	10		24	12	ns	
	15		20	10	ns	
Minimum C_D pulse width; HIGH	5	t_{WCDH}	50	25	ns	
	10		24	12	ns	
	15		20	10	ns	
Recovery time for S_D	5	t_{RSD}	15	-5	ns	
	10		15	0	ns	
	15		15	0	ns	
Recovery time for C_D	5	t_{RCD}	40	25	ns	
	10		25	10	ns	
	15		25	10	ns	
Maximum clock pulse frequency	5	f_{max}	7	14	MHz	
	10		14	28	MHz	
	15		20	40	MHz	

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$850 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = total load cap. (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3\,600 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$9\,000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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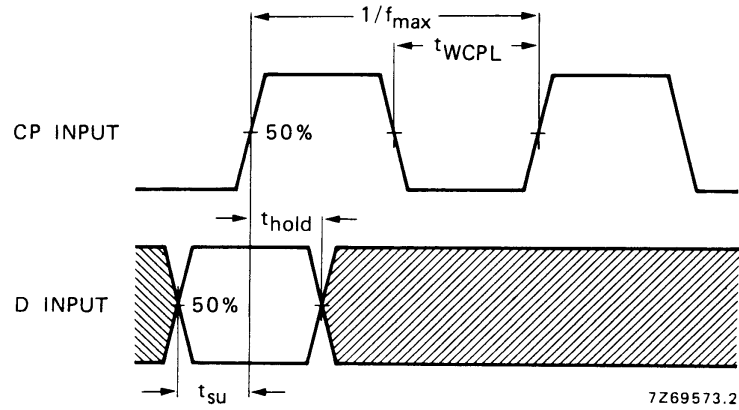


Fig.4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

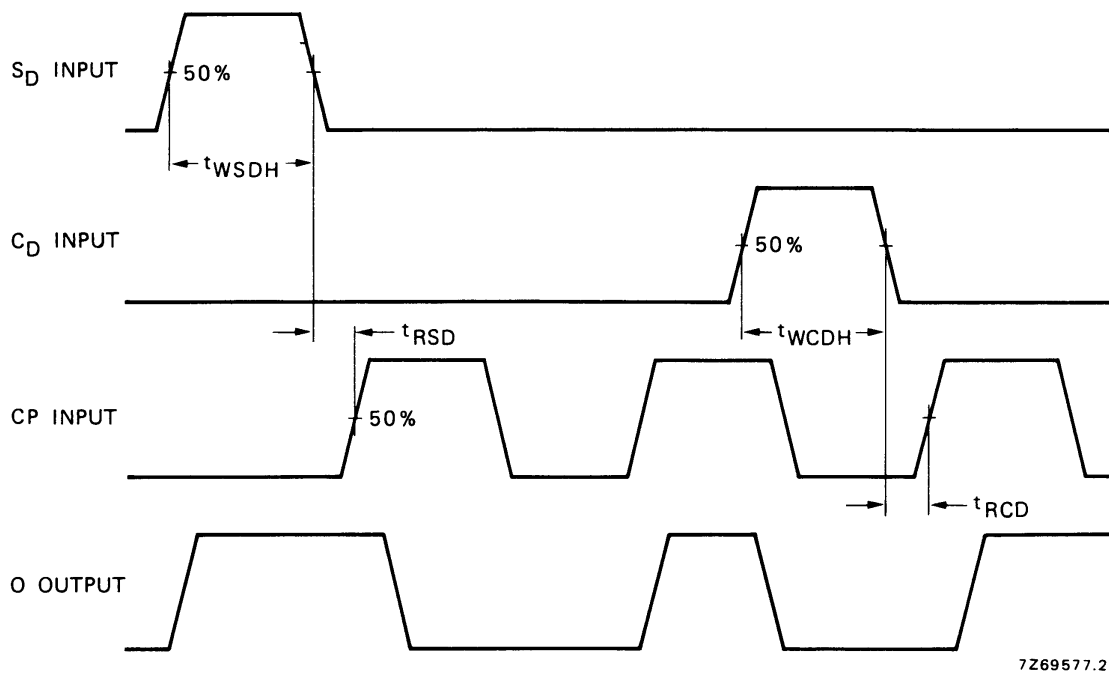


Fig.5 Waveforms showing recovery times for S_D and C_D ; minimum S_D and C_D pulse widths.

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APPLICATION INFORMATION

Some examples of applications for the HEF4013B are:

- Counters/dividers
- Registers
- Toggle flip-flops

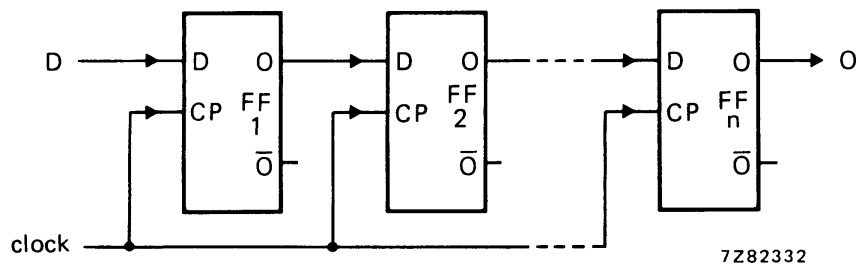


Fig.6 Typical application of the HEF4013B in an n-stage shift register.

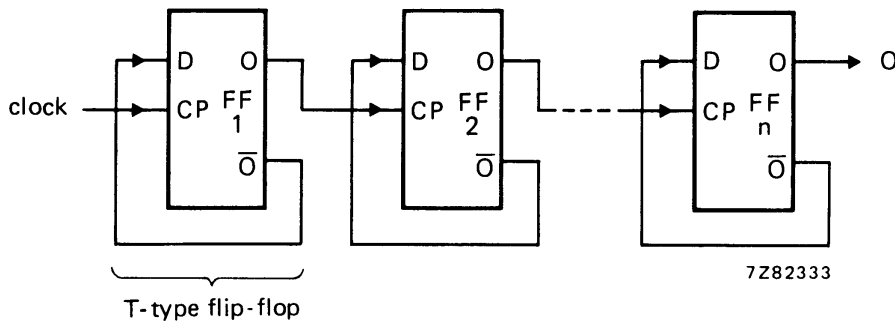


Fig.7 Typical application of the HEF4013B in a binary ripple up-counter; divide-by-2ⁿ.

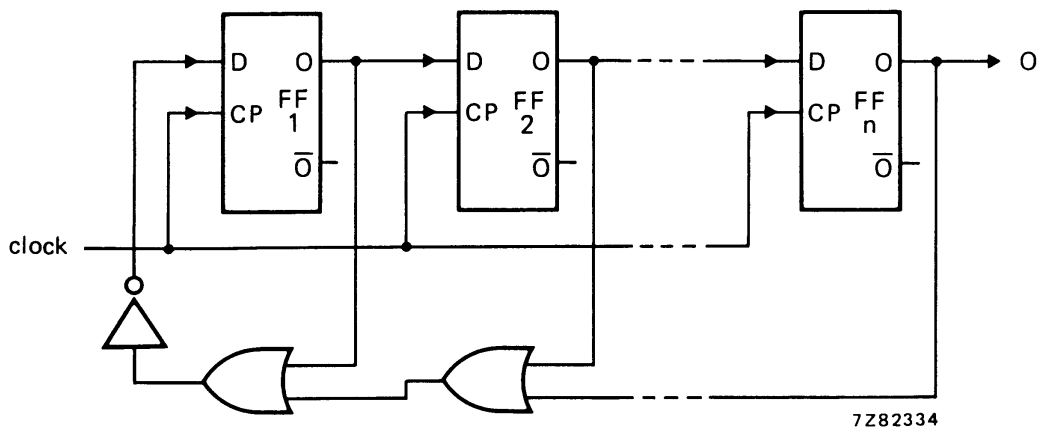


Fig.8 Typical application of the HEF4013B in a modified ring counter; divide-by-(n + 1).