

Balanced modulator/demodulator

MC1496/MC1596

DESCRIPTION

The MC1496 is a monolithic double-balanced modulator/demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of -55 to +125°C. The MC1496 is intended for applications within the range of 0 to +70°C.

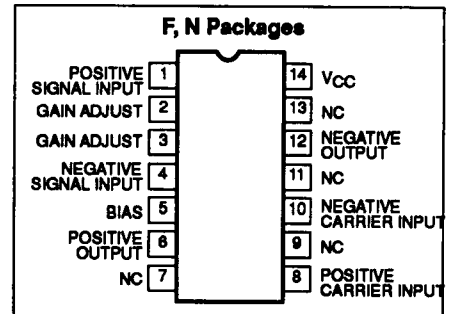
FEATURES

- Excellent carrier suppression
65dB typ @ 0.5MHz
50dB typ @ 10MHz
- Adjustable gain and signal handling
- Balanced inputs and outputs
- High common-mode rejection—85dB typ

APPLICATIONS

- Suppressed carrier and amplitude modulation
- Synchronous detection
- FM detection
- Phase detection
- Sampling
- Single sideband
- Frequency doubling

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Cerdip	0 to +70°C	MC1496F	0581
14-Pin Plastic	0 to +70°C	MC1496N	0405
14-Pin Cerdip	-55 to +125°C	MC1596F	0581
14-Pin Plastic	-55 to +125°C	MC1596N	0405

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
	Applied voltage	30	V
V_8-V_{10}	Differential input signal	± 5.0	V
V_4-V_1	Differential input signal	$(5 \pm I_5 R_0)$	V
V_2-V_1 , V_3-V_4	Input signal	5.0	V
I_5	Bias current	10	mA
P_D	Maximum power dissipation, $T_A=25^\circ\text{C}$ (still-air) ¹ F package N package	1190 1420	mW mW
T_A	Operating temperature range MC1496 MC1596	0 to +70 -55 to +125	°C °C
T_{STG}	Storage temperature range	-65 to +150	°C

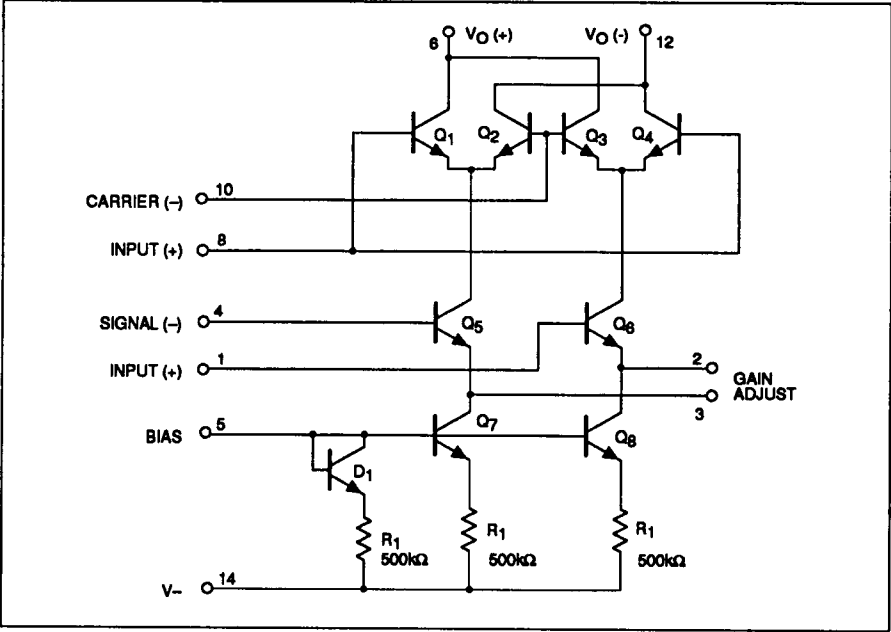
NOTES:

- Derate above 25°C, at the following rates:
F package at 9.5mW/°C
N package at 11.4mW/°C

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EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS

V_{CC}=+12V_{DC}; V_{CC}=-8.0V_{DC}; I_S=1.0mA_{DC}; R_L=3.9kΩ; R_E=1.0kΩ; T_A=25°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
R _{IP} C _{IP}	Single-ended input impedance Parallel input resistance Parallel input capacitance	Signal port, f=5.0MHz		200 2.0			200 2.0		kΩ pF
R _{OP} C _{OP}	Single-ended output impedance Parallel output resistance Parallel output capacitance	f=10MHz		40 5.0			40 5.0		kΩ pF
I _{BS} I _{BC}	Input bias current I _{BS} = I _{BC} =			12 12	25 25		12 12	30 30	μA μA
I _{IOS} I _{IOC}	Input offset current I _{IOS} =I _{I1} -I _{I4} I _{IOC} =I _{I8} -I _{I10}			0.7 0.7	5.0 5.0		0.7 0.7	7.0 7.0	μA μA
T _{CI/O} I _{OO}	Average temperature coefficient of input offset current Output offset current I _{OO} =I _{I6} -I _{I12}			2.0 14	 50		2.0 15	 80	nA/°C μA
T _{C/OO} V _O	Average temperature coefficient of output offset current Common-mode quiescent output voltage (Pin 6 or Pin 12)			90 8.0	 		90 8.0	 	nA/°C V _{DC}
I _{D+} I _{D-}	Power supply current I _{D+} =I _{I6} +I _{I12} I _{D-} =I _{I14}			2.0 3.0	3.0 4.0		2.0 3.0	4.0 5.0	mA _{DC}
P _D	DC power dissipation			33			33		mW

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AC ELECTRICAL CHARACTERISTICS

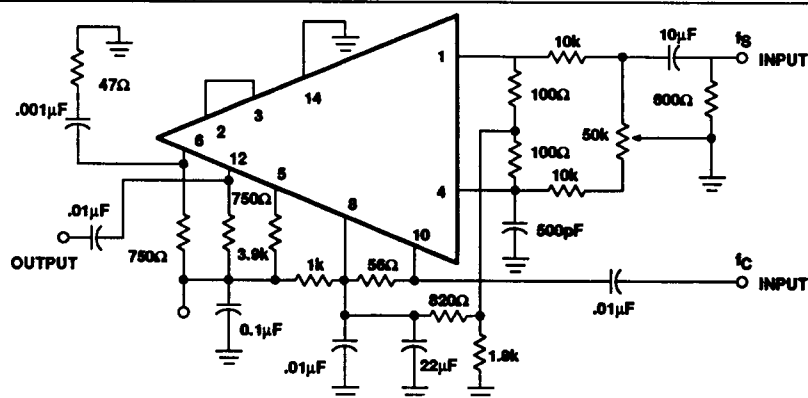
$V_{CC}=+12V_{DC}$; $V_{CC}=-9.0V_{DC}$; $I_S=1.0mA_{DC}$; $R_L=3.9k\Omega$; $R_E=1.0k\Omega$; $T_A=+25^\circ C$ unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CFT}	Carrier feedthrough	$V_C=60mV_{RMS}$ sinewave and offset adjusted to zero							μV_{RMS}
		$f_C=1.0kHz$		40			40		
		$f_C=10MHz$		140			140		mV_{RMS}
		$V_C=300mV_{P-P}$ squarewave: Offset adjusted to zero $f_C=1.0kHz$ Offset not adjusted $f_C=1.0kHz$		0.04 20	0.2 100		0.04 20	0.4 200	
V_{CS}	Carrier suppressions	$f_S=10kHz$, $300mV_{RMS}$ sinewave $f_C=500kHz$, $60mV_{RMS}$ sinewave $f_C=10MHz$, $60mV_{RMS}$ sinewave	50	65 50		40	65 50		dB
BW_{3dB}	Transadmittance bandwidth (Magnitude) ($R_L=50\Omega$)	Carrier input port, $V_C=60mV_{RMS}$ sinewave $f_S=1.0kHz$, $300mV_{RMS}$ sinewave		300			300		MHz
		Signal input port, $V_S=300mV_{RMS}$ sinewave $ V_C = 0.5V_{DC}$		80			80		MHz
A_{VS}	Signal gain	$V_S=100mV_{RMS}$; $f=1.0kHz$ $ V_C = 0.5V_{DC}$	2.5	3.5		2.5	3.5		V/V
CMV A_{CM}	Common-mode input swing Common-mode gain	Signal port, $f_S=1.0kHz$ Signal port, $f_S=1.0kHz$ $ V_C = 0.5V_{DC}$		5.0 -85			5.0 -85		V_{P-P} dB
DV_{OUT}	Differential output voltage swing capability			8.0			8.0		V_{P-P}

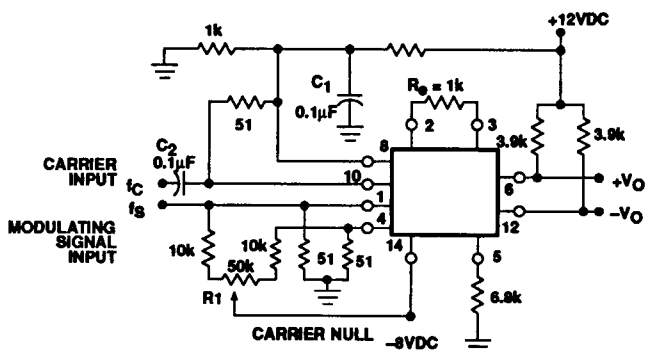
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TEST CIRCUITS



Carrier Rejection and Suppression



Carrier Rejection and Suppression

