

# DATA SHEET

## **MCR106-6** Thyristors logic level

Product specification

July 2001

Thyristors logic level

MCR106-6

GENERAL DESCRIPTION

Passivated, sensitive gate thyristor in a plastic envelope, intended for use in general purpose switching and phase control applications. This device is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

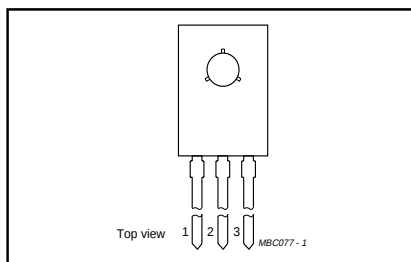
QUICK REFERENCE DATA

| SYMBOL              | PARAMETER                            | MAX. | UNIT |
|---------------------|--------------------------------------|------|------|
| $V_{\text{DRM}}$    | Repetitive peak off-state voltages   | 400  | V    |
| $V_{\text{RRM}}$    |                                      |      |      |
| $I_{\text{T(AV)}}$  | Average on-state current             | 2.5  | A    |
| $I_{\text{T(RMS)}}$ | RMS on-state current                 | 4    | A    |
| $I_{\text{TSM}}$    | Non-repetitive peak on-state current | 38   | A    |

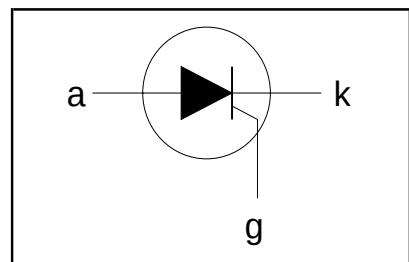
PINNING - SOT32

| PIN | DESCRIPTION |
|-----|-------------|
| 1   | cathode     |
| 2   | anode       |
| 3   | gate        |

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

| SYMBOL                           | PARAMETER                                                    | CONDITIONS                                                                                              | MIN. | MAX.             | UNIT               |
|----------------------------------|--------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|------|------------------|--------------------|
| $V_{\text{DRM}}, V_{\text{RRM}}$ | Repetitive peak off-state voltages                           |                                                                                                         | -    | 400 <sup>1</sup> | V                  |
| $I_{\text{T(AV)}}$               | Average on-state current                                     | half sine wave; $T_{\text{mb}} \leq 113\text{ }^{\circ}\text{C}$                                        | -    | 2.5              | A                  |
| $I_{\text{T(RMS)}}$              | RMS on-state current                                         | all conduction angles                                                                                   | -    | 4                | A                  |
| $I_{\text{TSM}}$                 | Non-repetitive peak on-state current                         | half sine wave; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$ prior to surge                              | -    | 35               | A                  |
|                                  |                                                              | $t = 10\text{ ms}$                                                                                      | -    | 38               | A                  |
| $I^2t$                           | $I^2t$ for fusing                                            | $t = 8.3\text{ ms}$                                                                                     | -    | 6.1              | A <sup>2</sup> s   |
| $di_{\text{T}}/dt$               | Repetitive rate of rise of on-state current after triggering | $t = 10\text{ ms}$                                                                                      | -    | 50               | A/ $\mu\text{s}$   |
| $I_{\text{GM}}$                  | Peak gate current                                            | $I_{\text{TM}} = 10\text{ A}; I_{\text{G}} = 50\text{ mA}; di_{\text{G}}/dt = 50\text{ mA}/\mu\text{s}$ | -    | 2                | A                  |
| $V_{\text{GM}}$                  | Peak gate voltage                                            |                                                                                                         | -    | 5                | V                  |
| $V_{\text{RGM}}$                 | Peak reverse gate voltage                                    |                                                                                                         | -    | 5                | V                  |
| $P_{\text{GM}}$                  | Peak gate power                                              |                                                                                                         | -    | 5                | W                  |
| $P_{\text{G(AV)}}$               | Average gate power                                           | over any 20 ms period                                                                                   | -    | 0.5              | W                  |
| $T_{\text{stg}}$                 | Storage temperature                                          |                                                                                                         | -40  | 150              | $^{\circ}\text{C}$ |
| $T_{\text{j}}$                   | Operating junction temperature                               |                                                                                                         | -    | 125 <sup>2</sup> | $^{\circ}\text{C}$ |

**1** Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ $\mu\text{s}$ .

**2** Note: Operation above 110 $^{\circ}\text{C}$  may require the use of a gate to cathode resistor of 1k $\Omega$  or less.

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## THERMAL RESISTANCES

| SYMBOL         | PARAMETER                                       | CONDITIONS  | MIN. | TYP. | MAX. | UNIT |
|----------------|-------------------------------------------------|-------------|------|------|------|------|
| $R_{th\ j-mb}$ | Thermal resistance<br>junction to mounting base | in free air | -    | -    | 2.5  | K/W  |
| $R_{th\ j-a}$  | Thermal resistance<br>junction to ambient       |             | -    | -    | 95   | K/W  |

## STATIC CHARACTERISTICS

 $T_j = 25\ ^\circ\text{C}$  unless otherwise stated

| SYMBOL     | PARAMETER                 | CONDITIONS                                                                 | MIN. | TYP. | MAX. | UNIT          |
|------------|---------------------------|----------------------------------------------------------------------------|------|------|------|---------------|
| $I_{GT}$   | Gate trigger current      | $V_D = 12\ \text{V}$ ; $I_T = 0.1\ \text{A}$                               | -    | 15   | 200  | $\mu\text{A}$ |
| $I_L$      | Latching current          | $V_D = 12\ \text{V}$ ; $I_{GT} = 0.1\ \text{A}$                            | -    | 0.17 | 10   | mA            |
| $I_H$      | Holding current           | $V_D = 12\ \text{V}$ ; $I_{GT} = 0.1\ \text{A}$                            | -    | 0.10 | 6    | mA            |
| $V_T$      | On-state voltage          | $I_T = 5\ \text{A}$                                                        | -    | 1.23 | 1.8  | V             |
| $V_{GT}$   | Gate trigger voltage      | $V_D = 12\ \text{V}$ ; $I_T = 0.1\ \text{A}$                               | -    | 0.4  | 1.5  | V             |
| $I_D, I_R$ | Off-state leakage current | $V_D = V_{DRM(max)}$ ; $I_T = 0.1\ \text{A}$ ; $T_j = 110\ ^\circ\text{C}$ | 0.1  | 0.2  | -    | V             |
|            |                           | $V_D = V_{DRM(max)}$ ; $V_R = V_{RRM(max)}$ ; $T_j = 125\ ^\circ\text{C}$  | -    | 0.1  | 0.5  | mA            |

## DYNAMIC CHARACTERISTICS

 $T_j = 25\ ^\circ\text{C}$  unless otherwise stated

| SYMBOL    | PARAMETER                                     | CONDITIONS                                                                                                                                                                                                                   | MIN. | TYP. | MAX. | UNIT             |
|-----------|-----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------------------|
| $dV_D/dt$ | Critical rate of rise of<br>off-state voltage | $V_{DM} = 67\% V_{DRM(max)}$ ; $T_j = 125\ ^\circ\text{C}$ ;<br>exponential waveform; $R_{GK} = 100\ \Omega$                                                                                                                 | -    | 50   | -    | V/ $\mu\text{s}$ |
| $t_{gt}$  | Gate controlled turn-on<br>time               | $I_{TM} = 10\ \text{A}$ ; $V_D = V_{DRM(max)}$ ; $I_G = 5\ \text{mA}$ ;<br>$dI_G/dt = 0.2\ \text{A}/\mu\text{s}$                                                                                                             | -    | 2    | -    | $\mu\text{s}$    |
| $t_q$     | Circuit commutated<br>turn-off time           | $V_D = 67\% V_{DRM(max)}$ ; $T_j = 125\ ^\circ\text{C}$ ; $I_{TM} = 8\ \text{A}$ ;<br>$V_R = 10\ \text{V}$ ; $dI_{TM}/dt = 10\ \text{A}/\mu\text{s}$ ;<br>$dV_D/dt = 2\ \text{V}/\mu\text{s}$ ; $R_{GK} = 1\ \text{k}\Omega$ | -    | 100  | -    | $\mu\text{s}$    |

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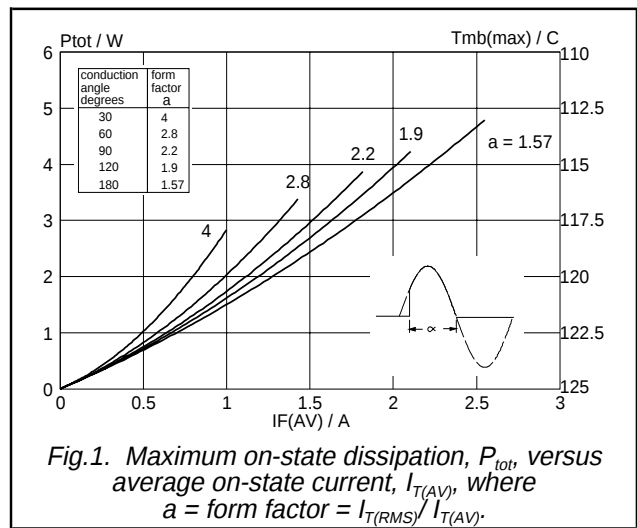


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{T(AV)}$ , where  $a = \text{form factor} = I_{T(RMS)} / I_{T(AV)}$ .

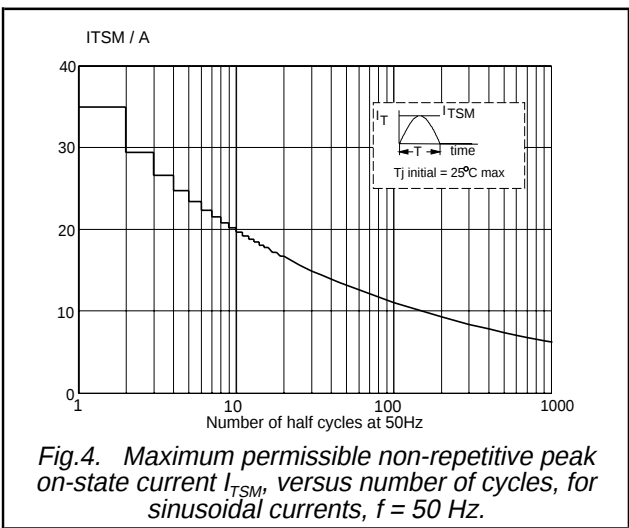


Fig.4. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50$  Hz.

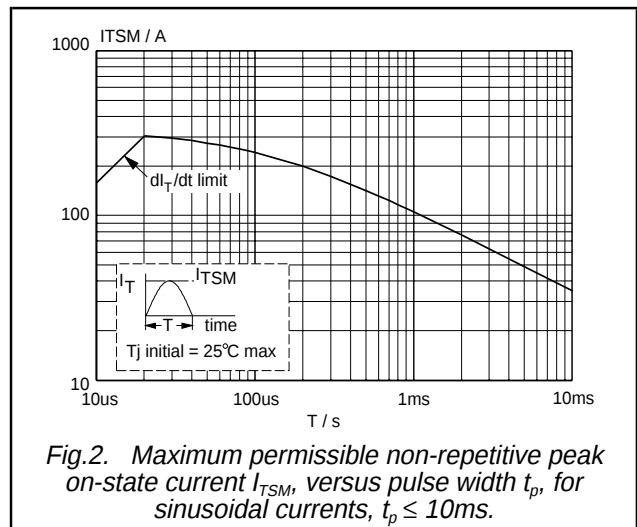


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10$  ms.

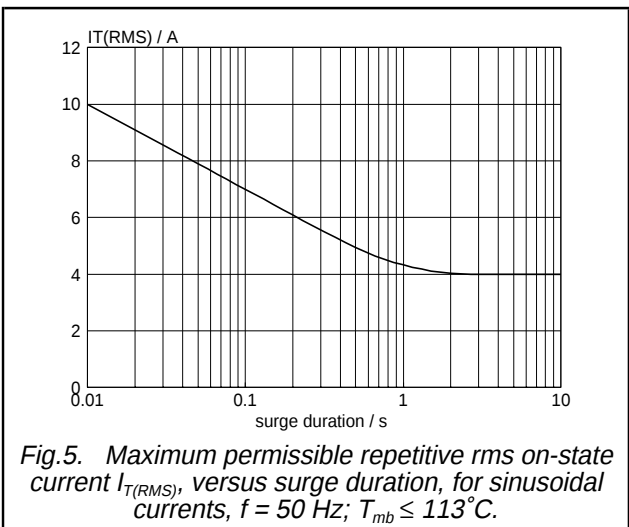


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50$  Hz;  $T_{mb} \leq 113^\circ\text{C}$ .

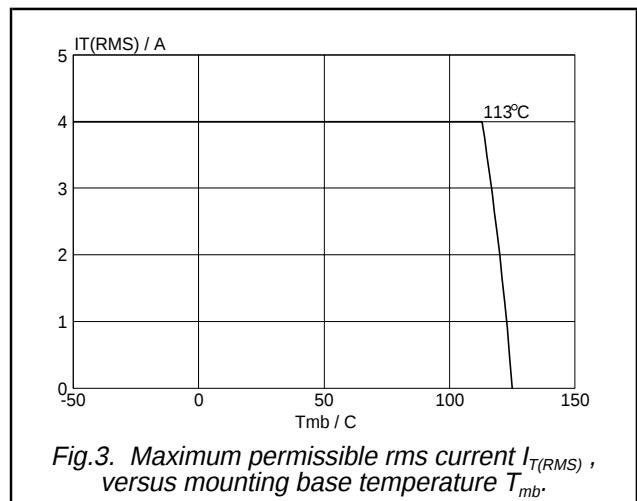


Fig.3. Maximum permissible rms current  $I_{T(RMS)}$ , versus mounting base temperature  $T_{mb}$ .

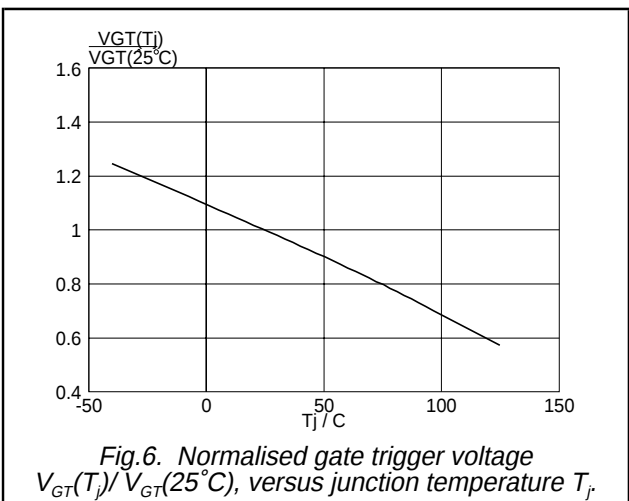


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j) / V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

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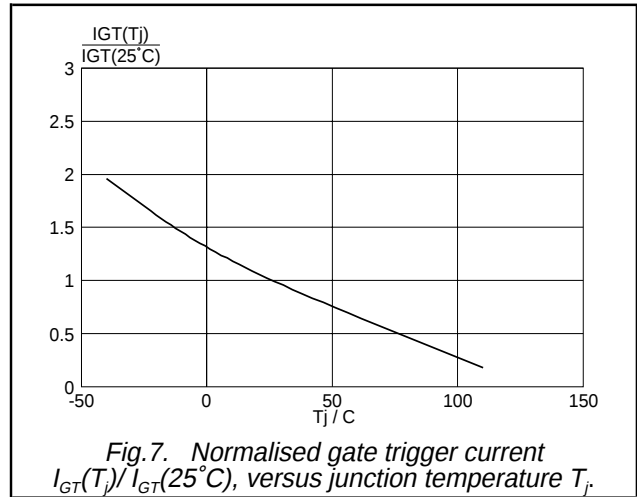


Fig. 7. Normalised gate trigger current  $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

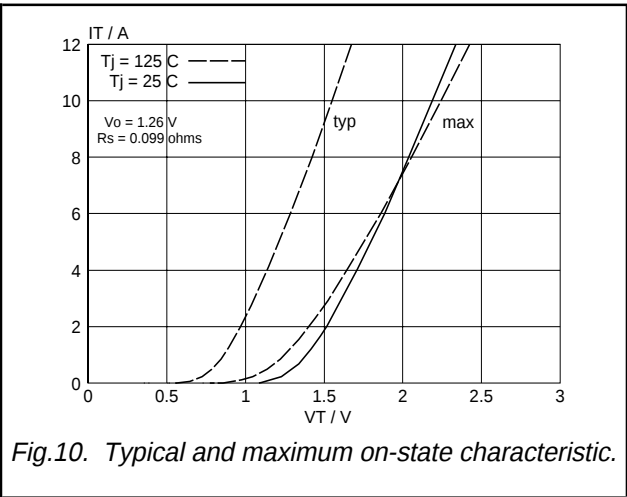


Fig. 10. Typical and maximum on-state characteristic.

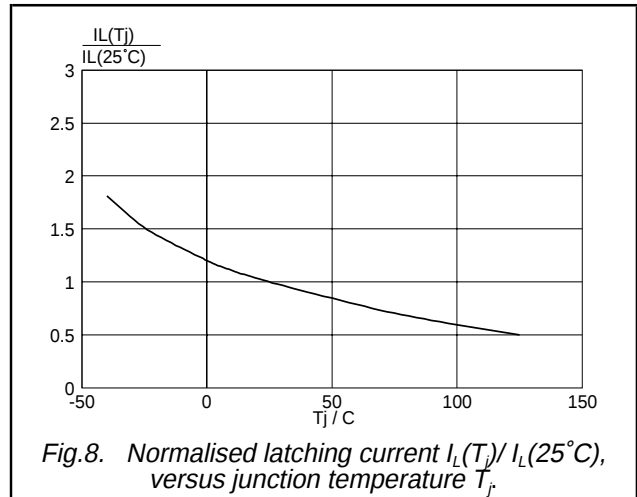


Fig. 8. Normalised latching current  $I_L(T_j)/I_L(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

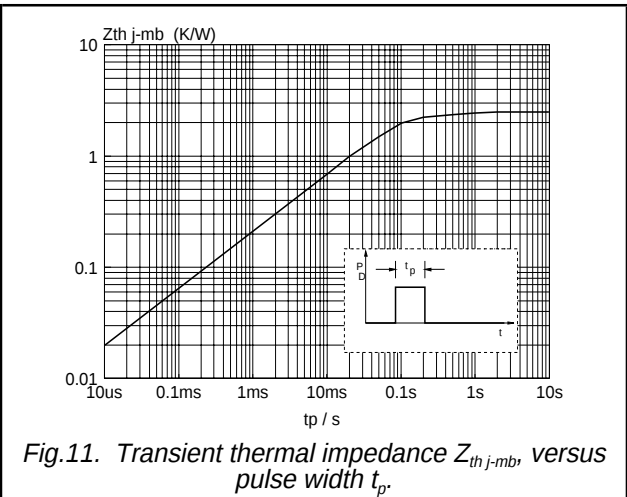


Fig. 11. Transient thermal impedance  $Z_{th\ j-mb}$ , versus pulse width  $t_p$ .

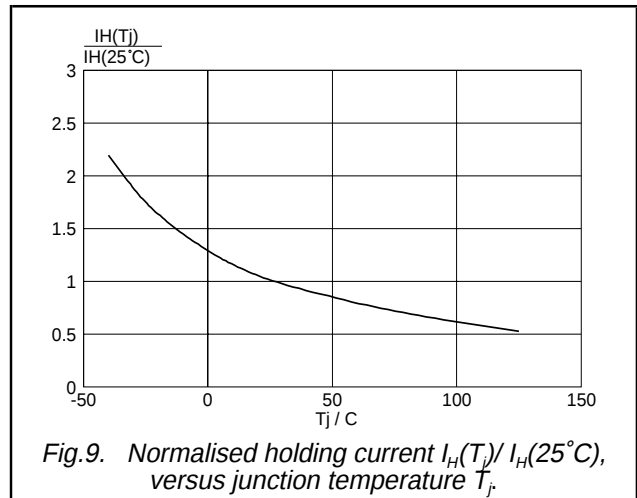


Fig. 9. Normalised holding current  $I_H(T_j)/I_H(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

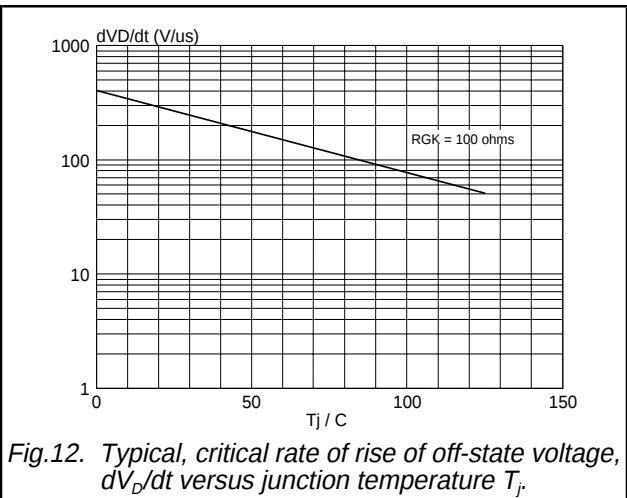


Fig. 12. Typical, critical rate of rise of off-state voltage,  $dV_D/dt$  versus junction temperature  $T_j$ .

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MECHANICAL DATA

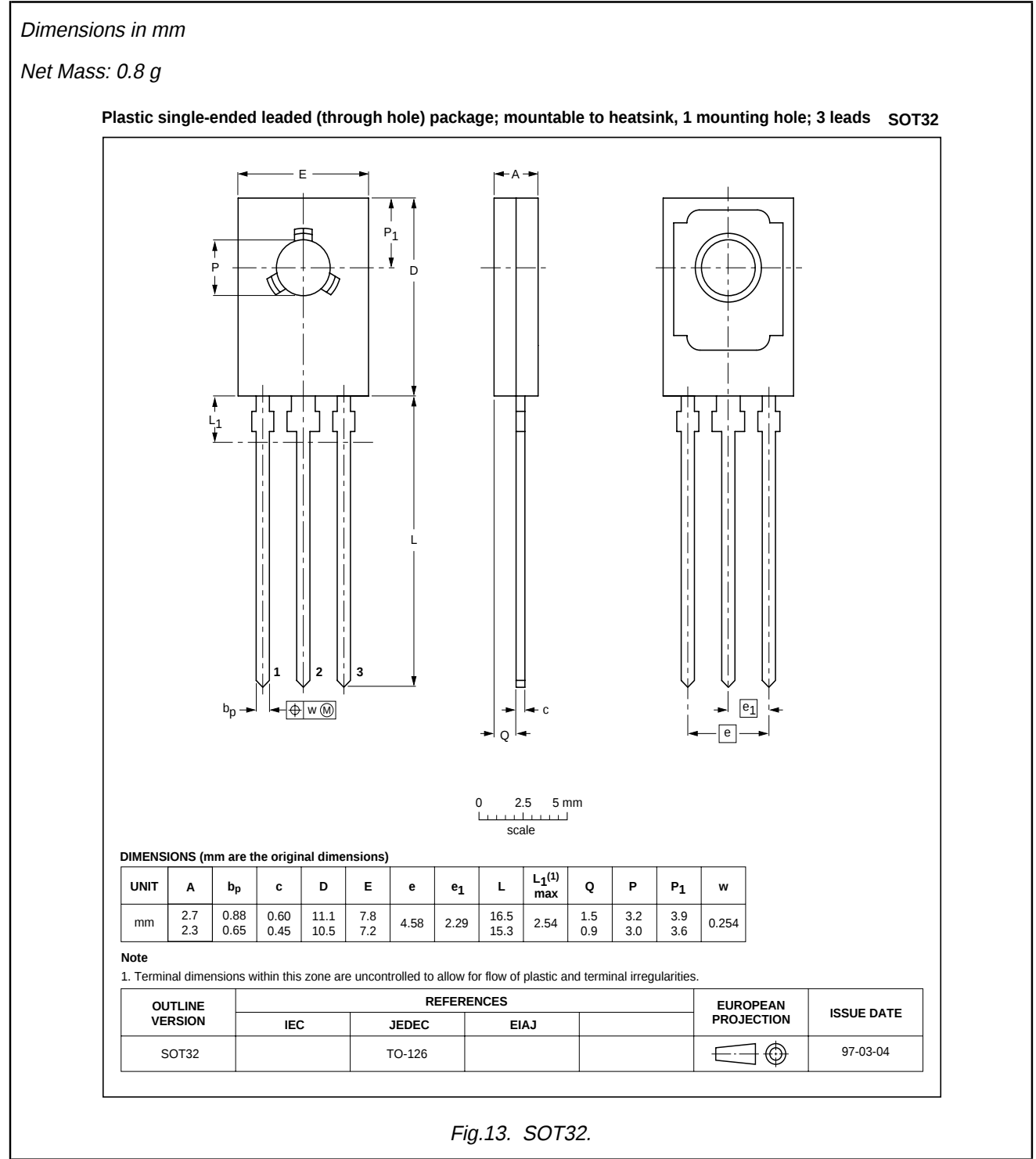


Fig.13. SOT32.

- Notes**
- 1. Refer to mounting instructions for SOT32 envelopes.
  - 2. Epoxy meets UL94 V0 at 1/8".

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## DEFINITIONS

| DATA SHEET STATUS                                                                                                                                                                                                                                                                                                                                                                                                                                          |                             |                                                                                                                                                                                                                                                                                                                       |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DATA SHEET STATUS <sup>3</sup>                                                                                                                                                                                                                                                                                                                                                                                                                             | PRODUCT STATUS <sup>4</sup> | DEFINITIONS                                                                                                                                                                                                                                                                                                           |
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