

DATA SHEET

PDTA114E series

PNP resistor-equipped transistors;

$R1 = 10\text{ k}\Omega$, $R2 = 10\text{ k}\Omega$

Product specification
Supersedes data of 2003 Apr 10

2004 Aug 02

PNP resistor-equipped transistors; R1 = 10 k Ω , R2 = 10 k Ω

PDTA114E series

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	–50	V
I _O	output current (DC)	–	–100	mA
R1	bias resistor	10	–	k Ω
R2	bias resistor	10	–	k Ω

DESCRIPTION

PNP resistor-equipped transistor (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN COMPLEMENT
	PHILIPS	EIAJ		
PDTA114EE	SOT416	SC-75	03	PDTC114EE
PDTA114EEF	SOT490	SC-89	03	PDTC114EEF
PDTA114EK	SOT346	SC-59	03	PDTC114EK
PDTA114EM	SOT883	SC-101	E5	PDTC114EM
PDTA114ES	SOT54 (TO-92)	SC-43	TA114E	PDTC114ES
PDTA114ET	SOT23	–	*03 ⁽¹⁾	PDTC114ET
PDTA114EU	SOT323	SC-70	*03 ⁽¹⁾	PDTC114EU

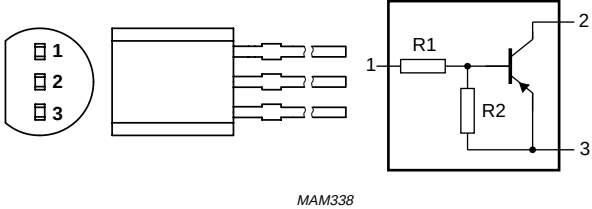
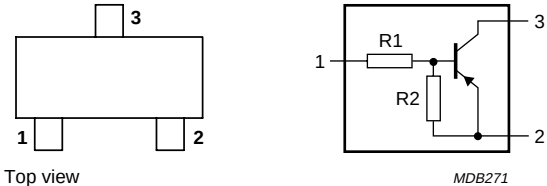
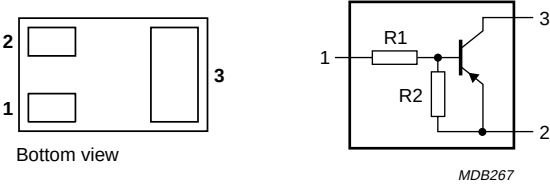
Note

- * = p: Made in Hong Kong.
* = t: Made in Malaysia.
* = W: Made in China.

PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

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SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PDTA114ES		1 2 3	base collector emitter
PDTA114EE PDTA114EEF PDTA114EK PDTA114ET PDTA114EU		1 2 3	base emitter collector
PDTA114EM		1 2 3	base emitter collector

PNP resistor-equipped transistors; R1 = 10 k Ω , R2 = 10 k Ω

PDTA114E series

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	–	–50	V
V _{CEO}	collector-emitter voltage	open base	–	–50	V
V _{EBO}	emitter-base voltage	open collector	–	–10	V
V _I	input voltage				
	positive		–	+10	V
	negative		–	–40	V
I _O	output current (DC)		–	–100	mA
I _{CM}	peak collector current		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C			
	SOT54	note 1	–	500	mW
	SOT23	note 1	–	250	mW
	SOT346	note 1	–	250	mW
	SOT323	note 1	–	200	mW
	SOT416	note 1	–	150	mW
	SOT490	notes 1 and 2	–	250	mW
	SOT883	notes 2 and 3	–	250	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C

Notes

1. Refer to standard mounting conditions.
2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	in free air		
	SOT54	note 1	250	K/W
	SOT23	note 1	500	K/W
	SOT346	note 1	500	K/W
	SOT323	note 1	625	K/W
	SOT416	note 1	833	K/W
	SOT490	notes 1 and 2	500	K/W
	SOT883	notes 2 and 3	500	K/W

Notes

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2. Reflow soldering is the only recommended soldering method.
3. Refer to SOT883 standard mounting conditions; FR4 with 60 μ m copper strip line.

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PDTA114E series

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = -50 V; I _E = 0	–	–	-100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = -30 V; I _B = 0	–	–	-1	μ A
		V _{CE} = -30 V; I _B = 0; T _j = 150 °C	–	–	-50	μ A
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0	–	–	-400	μ A
h _{FE}	DC current gain	V _{CE} = -5 V; I _C = -5 mA	30	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = -10 mA; I _B = -0.5 mA	–	–	-150	mV
V _{i(off)}	input-off voltage	I _C = -100 μ A; V _{CE} = -5 V	–	-1.1	-0.8	V
V _{i(on)}	input-on voltage	I _C = -10 mA; V _{CE} = -0.3 V	-2.5	-1.8	–	V
R1	input resistor		7	10	13	k Ω
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C _c	collector capacitance	I _E = i _e = 0; V _{CB} = -10 V; f = 1 MHz	–	–	3	pF

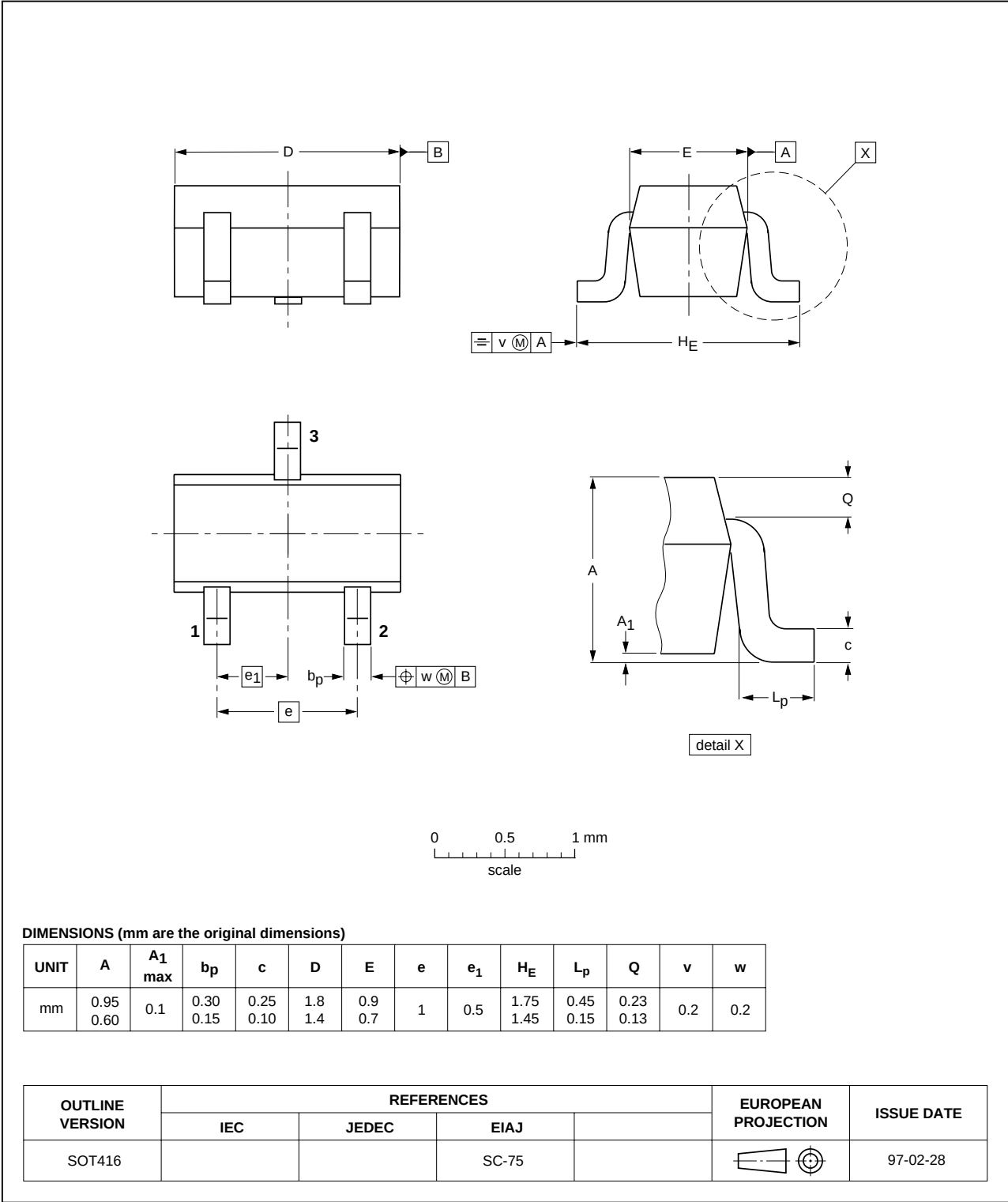
PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

PDTA114E series

PACKAGE OUTLINES

Plastic surface mounted package; 3 leads

SOT416

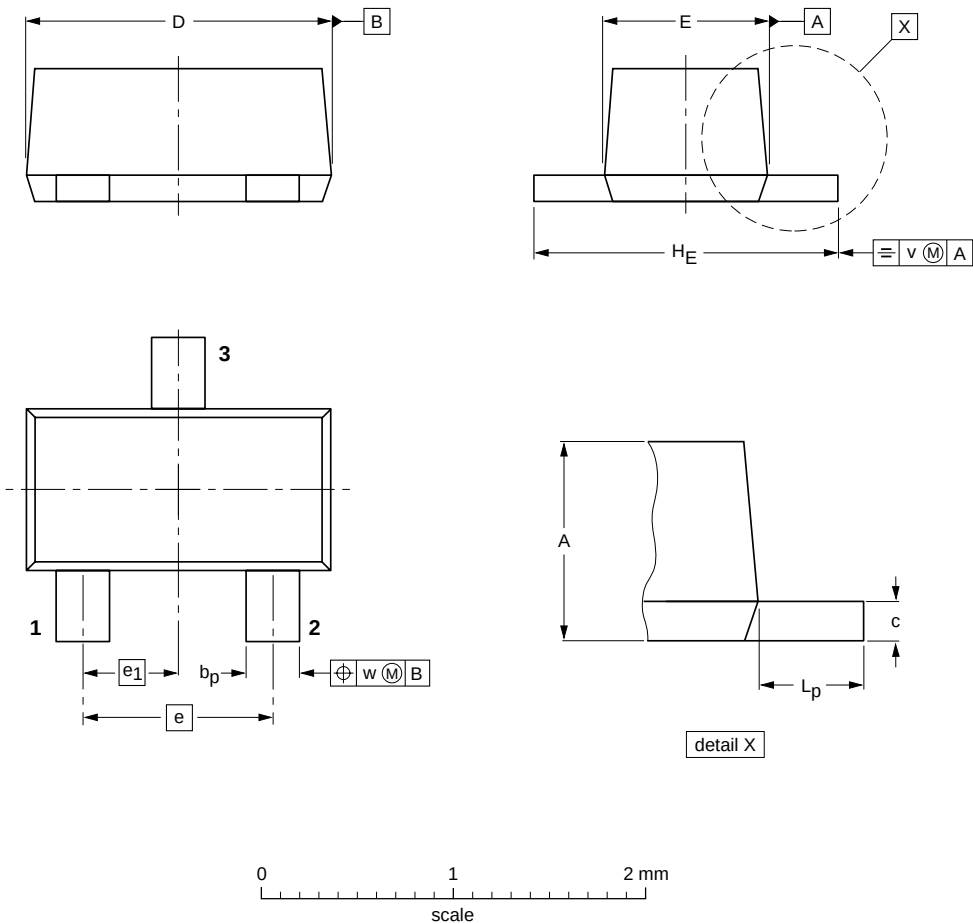


PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

PDTA114E series

Plastic surface mounted package; 3 leads

SOT490



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	H _E	L _p	v	w
mm	0.8 0.6	0.33 0.23	0.2 0.1	1.7 1.5	0.95 0.75	1.0	0.5	1.7 1.5	0.5 0.3	0.1	0.1

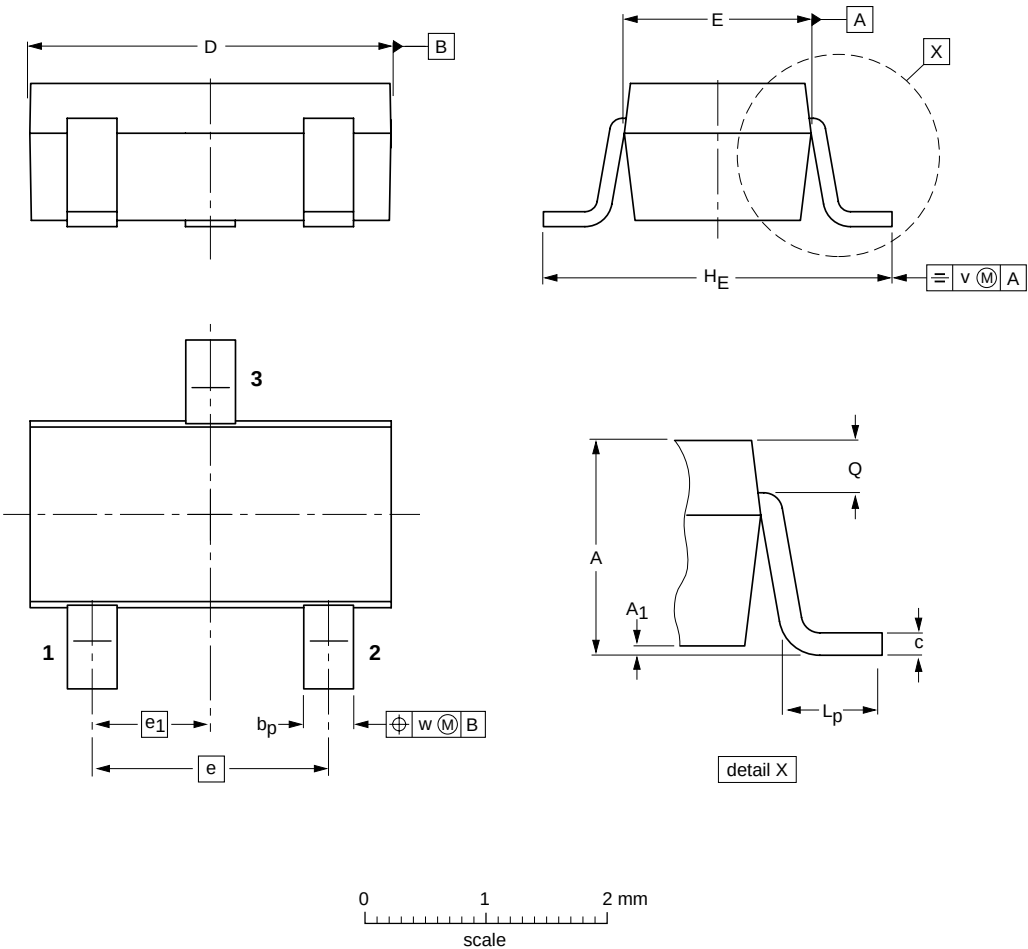
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT490			SC-89			98-10-23

PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

PDTA114E series

Plastic surface mounted package; 3 leads

SOT346



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.3 1.0	0.1 0.013	0.50 0.35	0.26 0.10	3.1 2.7	1.7 1.3	1.9	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2

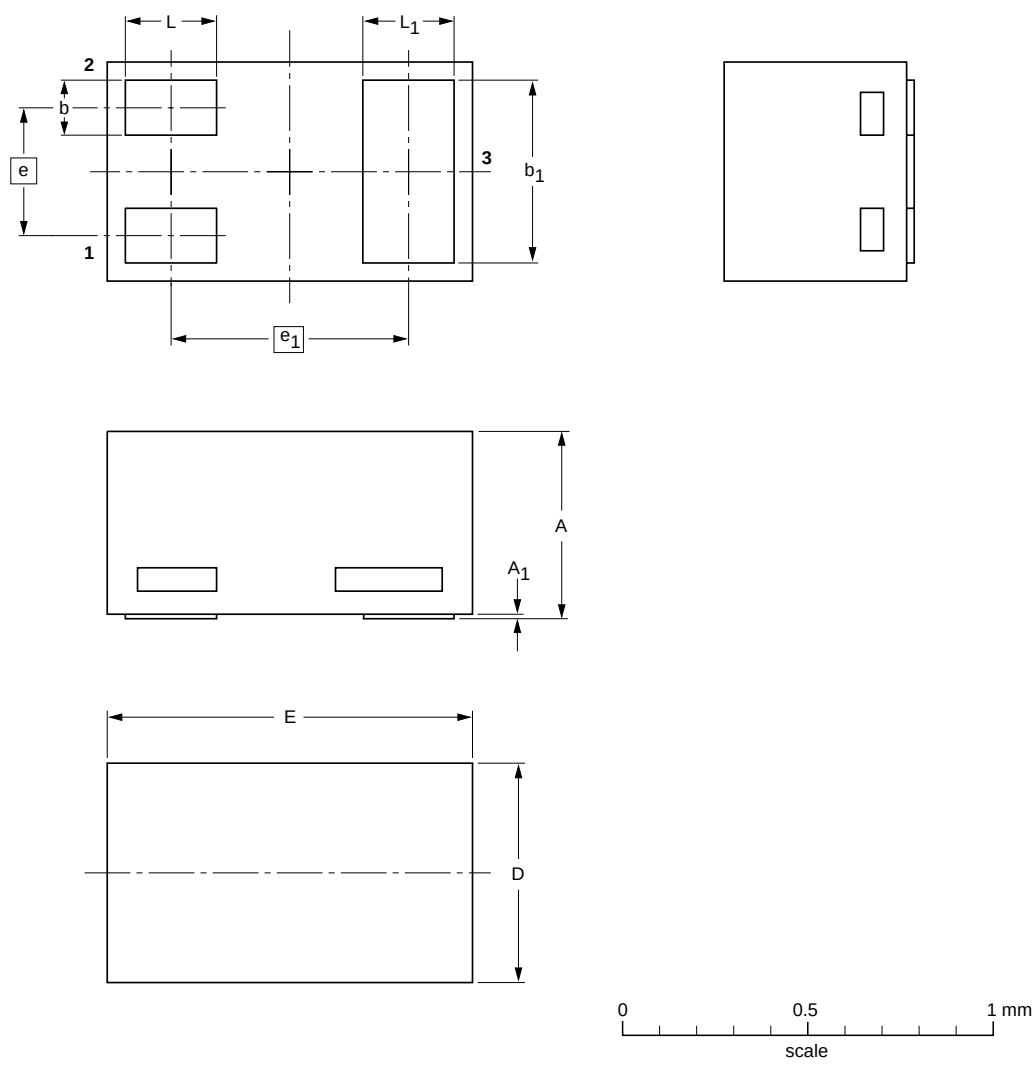
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT346		TO-236	SC-59			98-07-17

PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

PDTA114E series

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾	A ₁ max.	b	b ₁	D	E	e	e ₁	L	L ₁
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note
1. Including plating thickness

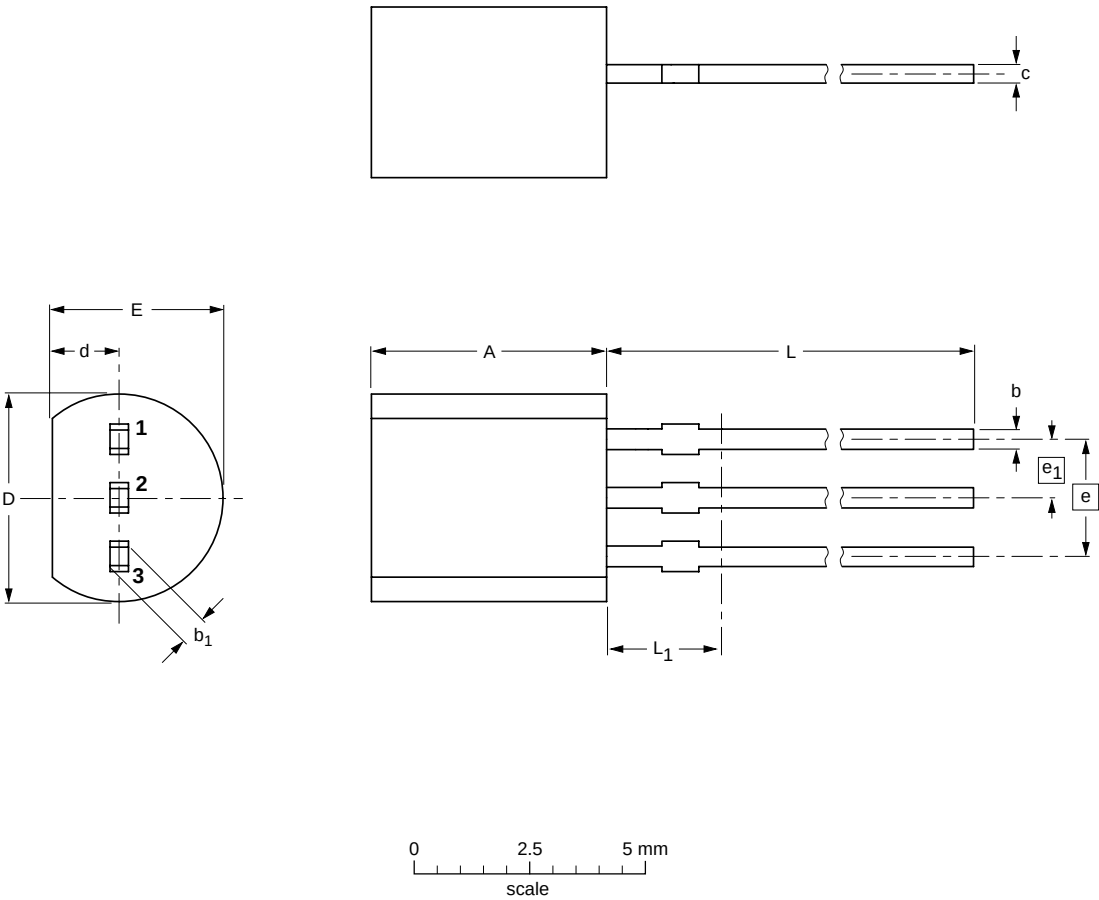
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT883			SC-101			03-02-05 03-04-03

PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

PDTA114E series

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

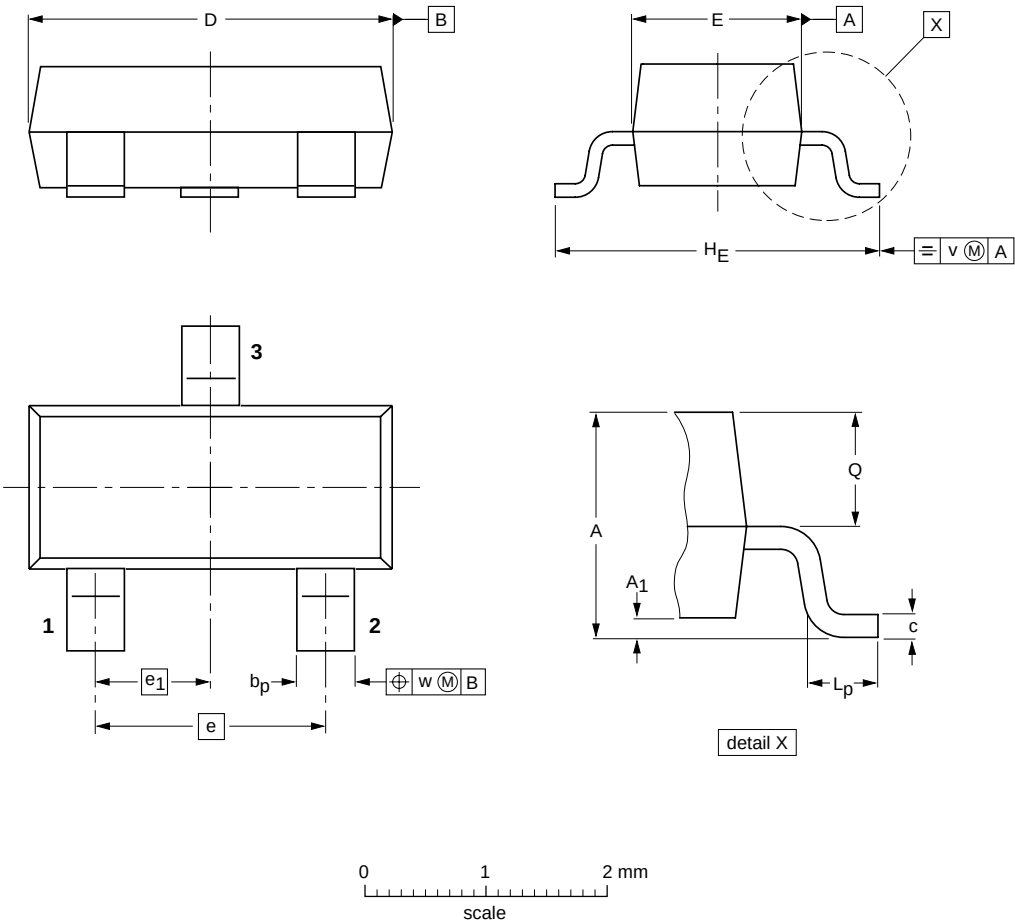
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	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			-97-02-28 04-06-28

PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

PDTA114E series

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max.	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

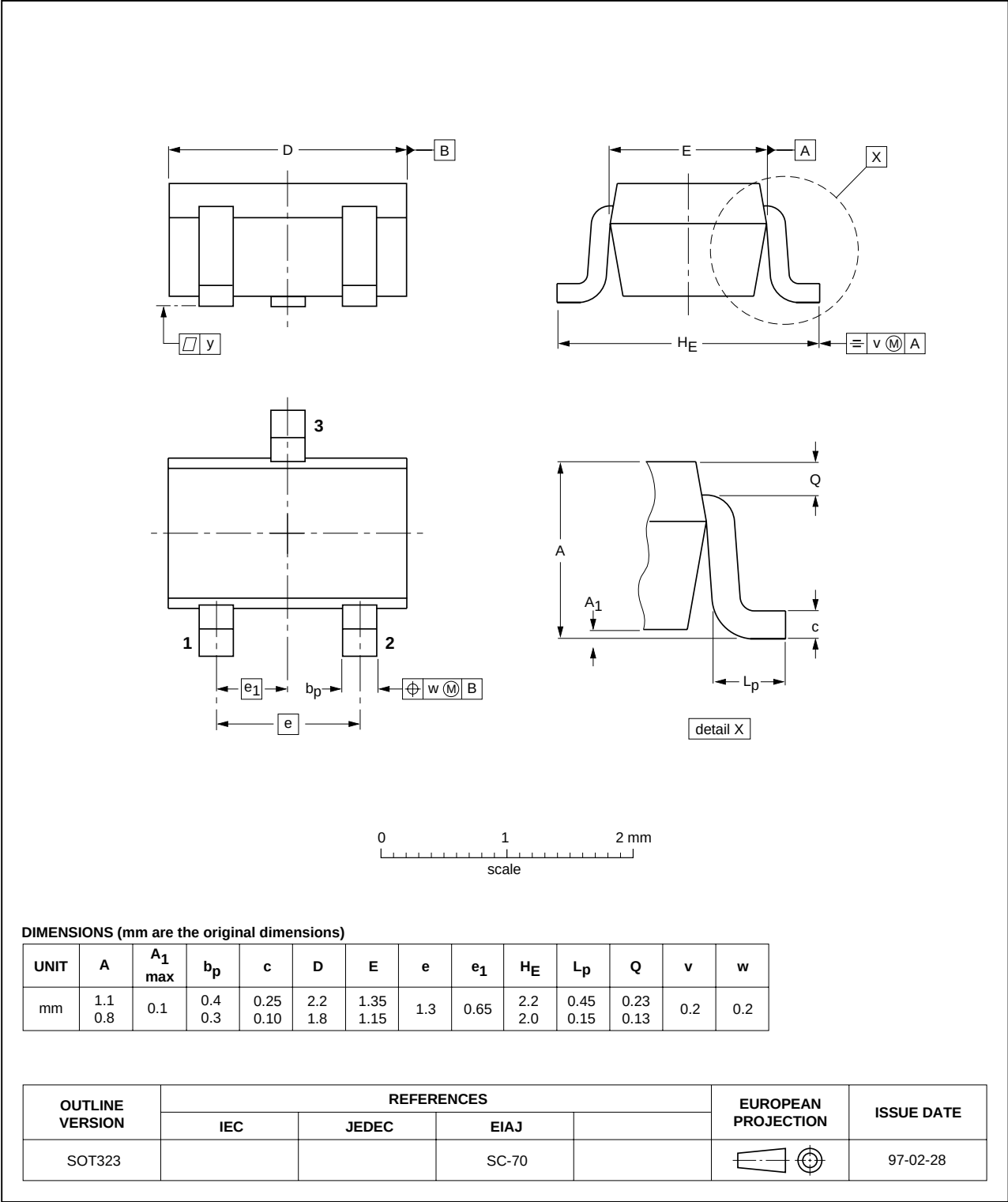
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23		TO-236AB				97-02-28 99-09-13

PNP resistor-equipped transistors;
R1 = 10 kΩ, R2 = 10 kΩ

PDTA114E series

Plastic surface mounted package; 3 leads

SOT323



PNP resistor-equipped transistors; R1 = 10 kΩ, R2 = 10 kΩ

PDTA114E series

DATA SHEET STATUS

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