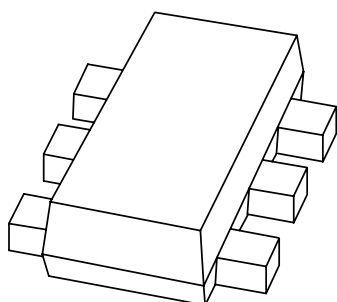


DATA SHEET



PEMB3

PNP resistor-equipped double
transistor $R1 = 4.7 \text{ k}\Omega$, $R2 = \text{open}$

Preliminary specification

2001 Sep 14

PNP resistor-equipped double transistor

R1 = 4.7 kΩ, R2 = open

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FEATURES

- 300 mW total power dissipation
- Very small 1.6 mm × 1.2 mm × 0.55 mm ultra thin package
- Excellent coplanarity due to straight leads
- Reduces number of components as replacement of two SC-75/SC-89 packaged transistors
- Reduces required board space
- Reduces pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

DESCRIPTION

PNP resistor-equipped double transistor in a SOT666 plastic package.

MARKING

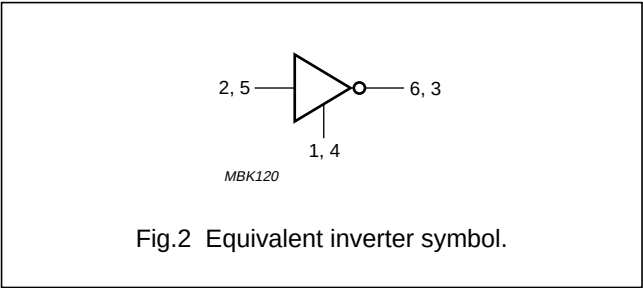
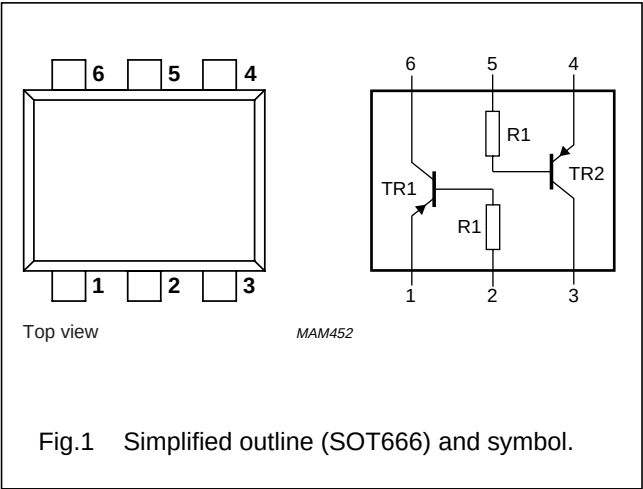
TYPE NUMBER	MARKING CODE
PEMB3	Z3

PINNING

PIN	DESCRIPTION	
1, 4	emitter	TR1; TR2
2, 5	base	TR1; TR2
6, 3	collector	TR1; TR2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{CEO}	collector-emitter voltage	−50	V
I _{CM}	peak collector current	−100	mA
TR1	PNP	−	−
TR2	PNP	−	−
R1	bias resistor	4.7	kΩ



PNP resistor-equipped double transistor

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
V _{CBO}	collector-base voltage	open emitter	–	–50	V
V _{CEO}	collector-emitter voltage	open base	–	–50	V
V _{EBO}	emitter-base voltage	open collector	–	–10	V
V _I	input voltage				
	positive		–	+10	V
	negative		–	–40	V
I _O	output current (DC)		–	–100	mA
I _{CM}	peak collector current		–	–100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	300	mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

PNP resistor-equipped double transistor

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CHARACTERISTICST_{amb} = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor						
I _{CBO}	collector cut-off current	I _E = 0; V _{CB} = -50 V	–	–	-100	nA
I _{CEO}	collector cut-off current	I _B = 0; V _{CE} = -50 V	–	–	-1	μ A
		I _B = 0; V _{CE} = -30 V; T _j = 150 °C	–	–	-50	μ A
I _{EBO}	emitter cut-off current	I _C = 0; V _{EB} = -5 V	–	–	-100	nA
h _{FE}	DC current gain	I _C = -1 mA; V _{CE} = -5 V	200	–	–	
V _{CEsat}	collector-emitter saturation voltage	I _C = -5 mA; I _B = -0.25 mA	–	–	-100	mV
R1	input resistor		3.3	4.7	6.1	k Ω
C _c	collector capacitance	I _E = i _e = 0; V _{CB} = -10 V; f = 1 MHz	–	–	3	pF

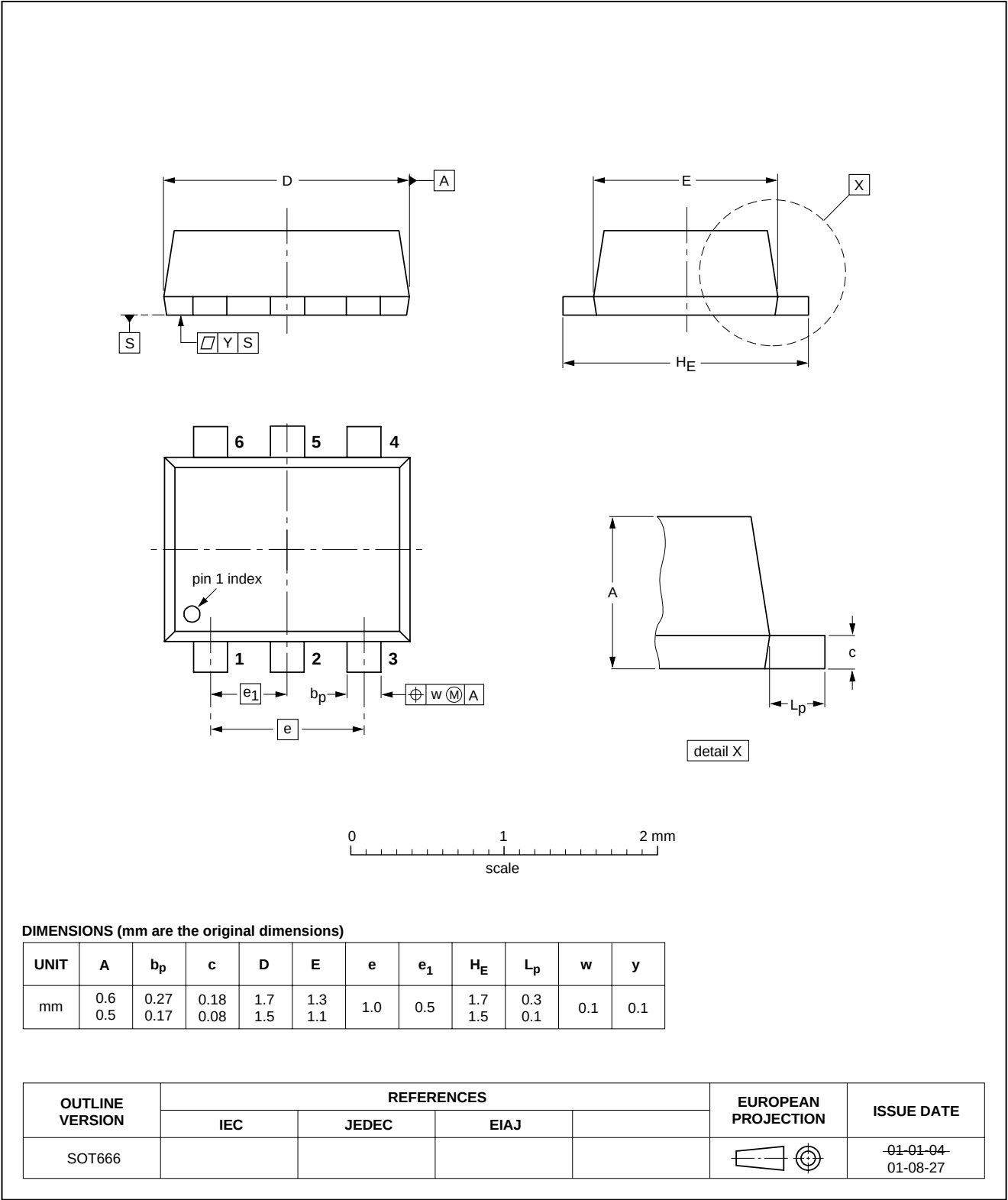
PNP resistor-equipped double transistor
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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



PNP resistor-equipped double transistor

R1 = 4.7 k Ω , R2 = open

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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NOTES

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